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Diagnostic Tests for Pre-Bond TSV Defects

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***Abstract*— Pre-bond testing and defect identification of through silicon via (TSV) is extremely important for yield assurance of 3D stacked devices. Based on a recently published pre-bond TSV probing technique, this paper proposes an ILP (integer linear programming) model to generate near-optimal set of sessions for pre-bond TSV test. The sessions generated by our model identify defective TSVs in a TSV network with the same capability as that of other available heuristic methods, but with consistently reduced test time. The ILP model is shown to reduce the pre-bond TSV test time by 38.2% for pinpointing up to two faulty TSVs in an 11-TSV network. Reducing pre-bond TSV test time helps reduce the manufacturing cost of 3D stacked devices. This ILP model has low complexity and an example demonstration using a commercial solver takes less than 40 seconds.**

***Keywords:* 3D stacked integrated circuits, pre-bond TSV testing, through silicon via (TSV) defects.**

I. Introduction

Through silicon vias (TSVs) act as media to transport power supply and signals among stacks of a 3D stacked integrated circuit (IC). The testing of TSVs is important as a single irreparable TSV can cause an entire stack to fail. TSVs can be tested before die bonding (pre-bond) or after die bonding (post-bond). Pre-bond TSV test targets defects arising in wafer manufacturing, such as a void within a TSV, a complete break in a TSV, a pinhole creating a leakage path between TSV and substrate, etc. Pre-bond TSV testing is important as it helps identify defective dies early in the process and avoid situations where one single bad die causes entire 3D stack to be discarded. It is also necessary in providing known good die (KGD) information for die-to-die or die-to-wafer fabrication process. Even for wafer-on-wafer stacking, pre-bond TSV test helps in better wafer matching and thus improves the yield [14], [17], [20], [21]. Post-bond TSV test targets the defects that arise during the assembly process. These defects can be caused by TSV misalignment, mechanical stress, thermal issues, etc. Recent work [3] identifies eleven kinds of TSV defects, of which six occur before bonding.

The post-bond TSV test has been extensively studied [8], [9], [13]. After bonding TSVs are basically treated as wires. Post-bond TSV testing can also be easily conducted by employing the developing IEEE P1838 standard [8], [9], [12]. The pre-bond TSV testing is challenging mainly because before-bonding a TSV is single ended, i.e., one of its ends is not connected to any circuitry. For pre-bond TSV test, we can test on a still thick wafer. In that case, the TSVs are deeply buried in the wafer substrate without any test access. This requires special per-bond DFT circuit (e.g., BIST) to test TSVs with only single-sided access. Several built-in self-test (BIST) techniques have been proposed for buried TSVs, such as, the use of a voltage division circuit to measure the leakage resistance of TSVs and detect pinhole defects [5], or a DRAM and ROM-like test to determine the RC time constant and resistance of blind TSVs and open-sleeve TSVs, respectively [4]. Ring Oscillators have been widely used to characterize the propagation delay of TSVs and thus diagnose possible resistive open or leakage defects [6], [19]. All BIST approaches require dedicated circuit to be added for each individual TSV, and the area overhead is huge since there can be tens of thousands of TSVs on a chip [7]. Moreover, the BIST circuits themselves suffer from process variation, which may render them totally useless. An alternative is to test thinned wafers where TSV tips are exposed. This requires special facilities to probe thinned wafers (about 50 µm thick) without damaging them. However, the relatively large pitch (40 µm) of current probing technology [16], [18] prohibits individual TSV probing with a realistic pitch of 10 µm [7].

A pre-bond TSV probing method has been recently proposed [11] where several TSVs are contacted by a single probe needle defining a *TSV network*. The number T of TSVs within a network is typically less than 20 and depends on the relative diameter of the probe needle and the pitch of TSVs [7], [10], [12], [16], [18]. TSV parametric test can be conducted by adding an active driver in the probe needle and forming a charge sharing circuit between single (or multiple) TSV(s) and the probe needle. This probing method offers robustness to process variation, requires less hardware overhead, provides accurate measurement of TSV resistance, and has many more benefits as explained in the original proposal [10], [11], [12]. A possible concern in the utilization of this technique is that a lack of perfect planarity of TSV tips may prevent a large probe needle from making simultaneous electrical contact with all TSVs in a network. However, benefits of the probing method serve as a driving force for both foundry and test equipment manufacturer to work together and find a solution.

For this test procedure [11], a heuristic method [10] generates a series of test sessions that can uniquely locate a given number of faulty TSVs within a network. This heuristic method has been shown to reduce the test time compared to that of testing each TSV individually. However, the improvement is far from being optimal.

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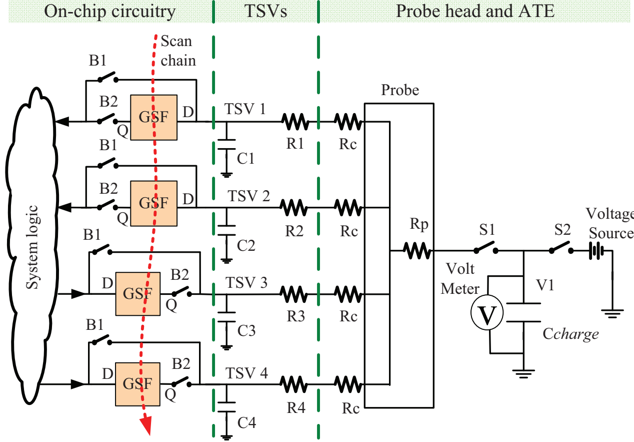

Fig. 1: Circuit model for pre-bond TSV probing.

We address the problem of test session generation for pre-bond TSV probing with a focus on minimizing the identification time of faulty TSVs. The proposed integer linear programming (ILP) method for session generation reduces test time compared to that of the heuristic method [10]. To the best of our knowledge, this is the first work on using ILP for generating pre-bond TSV test sessions.

II. Preliminaries and Motivation

Since most pre-bond TSV defects are resistive in nature [3], pinpointing the resistive defects is very important. Considering the relative sizes of typical test probes and TSVs, an earlier proposal [11] used a large probe needle with an active driver to contact multiple TSVs at a time.

Figure 1 shows a circuit model of the test set up for a four-TSV network [11], [12]. TSV i is represented by its resistance R_i and capacitance C_i. R_c is the contact resistance between the TSV and probe. A gated scan flip-flop (GSF) is inserted between TSV i and the system logic in accordance with the developing IEEE P1838 standard [8], [9], [12]. All GSFs can be loaded up or read out through a boundary scan mechanism. In the normal mode, a "bypass" signal makes all GSFs transparent by opening switch B2 and closing switch B1. In Figure 1, TSVs 1 and 2 are receiving TSVs and TSVs 3 and 4 are sending TSVs. A receiving TSV receives signal from the other die and drives the on-chip logic while a sending TSV is driven by the on-chip logic and sends a signal to the other die. A GSF in scan mode drives a receiving TSV during pre-bond TSV probing when both B1 and B2 switches are closed. A GSF drives a sending TSV when B1 is opened and B2 is closed.

Pre-bond TSV resistance measurement starts by scanning in all GSFs with "1." C_{charge} and all TSVs are then discharged through the probe needle. By configuring the switches of a GSF, a charge sharing circuit is constructed between that GSF and C_{charge} through its corresponding TSV. The charging rate of C_{charge} is compared to a calibrated curve of a good TSV to determine the resistance of the TSV under test. Parallel TSV test can also be conducted by configuring multiple GSFs at a time. Now, C_{charge} is charged faster and the measurement terminates quicker. However, the number of TSVs tested in parallel cannot exceed some "r" due to minimum measurement *resolution constraint* [11], [12]. The measurement resolution is the minimum change in TSV resistance that can be detected by the technique and it is adversely affected by the number of TSVs tested in parallel. In this work maximum value of r is constrained to 4, same as [15]. We call the TSVs tested in parallel within the same TSV network a *test session*. *Session size* q is defined as the number of TSVs within a session. In this probing technique, any faulty TSV within a session will cause the session test to fail but we cannot tell which TSV(s) is (are) faulty. On the other hand, a good parallel test implies that all TSVs within the session are fault-free. The above discharging and charging process continues until either all TSVs are identified as good or a certain number of defective TSV resistances are found within the network.

TABLE I: Capacitor charging time of parallel TSV test [15].

Number of TSVs tested in parallel (q)	Charging time $t(q)$ (µs)
1	0.80
2	0.53
3	0.42
4	0.38

SPICE simulation of a TSV probe setup was done using the predictive technology model (PTM) [2] for 45nm technology [10], [11], [12], [15]. The capacitance charging time as a function of *session size* is recorded in Table I. Note that the number of TSVs tested in parallel, i.e., *session size* q cannot exceed r. Also, *test time of a session* in this work only refers to the time to charge the capacitor C_{charge}, same as in [10]. It is related to the session size as shown in column 2 of Table I.

Intuitively, to pinpoint each defective TSV within a TSV network we can test one TSV at a time with highest resolution. However such high resolution may be unnecessary. Besides, the single-TSV session takes longer test time as shown in Table I. Instead of identifying all faulty TSVs, only up to a certain number of faulty TSVs need to be pinpointed in a network. The maximum number m of faulty TSVs to be identied within a TSV network equals to the number of redundant TSVs in that TSV network. If the number of faulty TSVs exceeds m, then not all faulty TSVs in the network can be repaired and the chip may be discarded.

Significant test time saving is possible if we test TSVs in parallel but retain the capability of identifying up to m faulty TSVs and guarantee that the size of each session does not exceed the resolution constraint r. Reference [10] proposes a heuristic to generate such test sessions. However, the results are far from being optimal due to the greedy nature of the heuristic employed. For example, to pinpoint one faulty TSV

in a 6-TSV network with minimum resolution constraint of $r = 4$, the heuristic based sessions [10] are {1,2,3,4}, {1,5,6}, {2,5}, {3,6}, {4}. The total time of these sessions is 2.66 µs according to Table I which is not optimal. The optimal sessions for this case would be {1,2,3}, {1,4,5}, {2,4,6}, {3,5,6}, which reduces the test time by 9.7%. This example motivates us to find a way to generate optimal set of test sessions with minimum test time.

III. ILP MODEL FOR TEST SESSION GENERATION WITH SPECIFIED IDENTIFICATION CAPABILITY

We propose an integer linear programming (ILP) model to find near-optimal set of test sessions. The problem is formulated as follow.

Problem 1. Given the test time $t(q)$ for test session size q, $q \in [1, r]$, and the maximum number m of faulty TSVs within a T-TSV network, determine a series of test sessions (each of size less than r) so that up to m faulty TSVs can be uniquely identified and the total test time is minimized.

A sufficient condition to solve Problem 1 is stated below.

Condition 1. If each TSV (TSV_i) is put in $m + 1$ test sessions, $S_1, S_2, \cdots, S_{m+1}$, and the intersection of any two out of these $m + 1$ sessions contain only TSV_i, i.e., $S_j \bigcap S_k = TSV_i$ for $j \neq k \in [1, m + 1]$, then up to m faulty TSVs within the network can be uniquely identified.

We refer to those $m+1$ sessions satisfying Condition 1 as $m + 1$ unique test sessions for TSV_i. A unique test session for TSV_i is defined as a session whose intersection with any other session containing TSV_i consists of only TSV_i. We prove the sufficiency of Condition 1 by first stating the following theorem.

Theorem 1. Given that there are no more than m faulty TSVs within a network. If a good TSV, TSV_i, belongs to $m+1$ unique test sessions, then we can find at least one out of these $m + 1$ sessions consisting only of good TSVs.

We prove Theorem 1 by contraposition.

Proof of Theorem 1. Given that there are up to m faulty TSVs within a network. Suppose each unique test session for TSV_i contains at least one faulty TSV. Because of the "unique" identity of these $m + 1$ sessions, the faulty TSVs within each session should be different. We conclude that there will be at least $m + 1$ faulty TSVs within the network, which is obviously a contradiction to the given condition that says there are at most m faulty TSVs. In other words, at least one unique session for TSV_i would contain only good TSVs.

Next, we prove Condition 1 is a sufficient condition for solving Problem 1.

Proof of sufficiency. According to Theorem 1, Condition 1 will guarantee that for any good TSV, say TSV_i, there will be at least one unique session, say session S_j, consisting only of good TSVs. The test result of S_j would suggest that all TSVs within S_j are fault-free. Thus, we uniquely identify TSV_i as a good TSV. If all good TSVs are identified, then all defective TSVs would be known too.

Proof of non-necessity. The non-necessity of Condition 1 is proved by considering a simple example. In sequential testing, all TSVs can be uniquely identified but each TSV resides in only one session.

The ILP model proposed next is based on Condition 1. We first summarize all general constraints for the model:

1) **C1.** Each TSV should reside in at least $m+1$ sessions.
2) **C2.** The size of a test session ranges anywhere from 0 (empty session) to r.
3) **C3.** We suppose any non-empty session is a unique session for any TSV within it.

An upper bound N_{up} on total number of sessions can be calculated as,

$$N_{up} = \left\lceil \frac{t(1)}{t(r)} \cdot T \right\rceil \tag{1}$$

where r is resolution constraint, $t(1)$ and $t(r)$ are test times for sessions with sizes 1 and r, respectively. If the number N of total sessions is larger than N_{up}, then even if all sessions have size r the total test time will still be larger than that of sequential testing. This upper bound constrains the maximum number of sessions produced by the ILP model that follows.

A binary variable x_{ij} ($1 \leq i \leq T, 1 \leq j \leq N_{up}$) is defined as follows:

$$x_{ij} = \begin{cases} 1 & \text{if } TSV_i \text{ is assigned to session } S_j \\ 0 & \text{otherwise} \end{cases} \tag{2}$$

From **C1**, we have

$$\sum_{j=1}^{N_{up}} x_{ij} \geq m + 1 \tag{3}$$

We define an integer variable L_j, which denotes the size of session S_j,

$$L_j = \sum_{i=1}^{T} x_{ij} \tag{4}$$

From **C2**, we have

$$0 \leq L_j \leq r \tag{5}$$

From **C3**, if $\exists\ x_{ij} \cdot x_{ik} = 1$ for any i and any $j \neq k \in [1, N_{up}]$, then $\sum_{i=1}^{T} x_{ij} \cdot x_{ik} = 1$. **C3** also implies that the intersection of any two different sessions S_j and S_k should contain no more than a single TSV, thus,

$$\left| S_j \bigcap S_k \right| = \sum_{i=1}^{T} x_{ij} \cdot x_{ik} \leq 1 \tag{6}$$

Constraint (6) is obviously nonlinear. To linearize it, we further introduce a binary variable $z_{ijk} = x_{ij} \cdot x_{ik}$ and two more linear constraints:

$$x_{ij} + x_{ik} - z_{ijk} \leq 1 \tag{7}$$

$$x_{ij} + x_{ik} - 2 \cdot z_{ijk} \geq 0 \tag{8}$$

According to these constraints if $x_{ij} = 0$, then $z_{ijk} \leq \frac{x_{ik}}{2}$. Since both x_{ik} and z_{ijk} are binary variables, z_{ijk} must be 0. If $x_{ij} = 1$, $x_{ik} \leq z_{ijk} \leq 0.5 + 0.5x_{ik}$, and we conclude, $z_{ijk} = x_{ik}$. Thus, constraints (7) and (8) guarantee $z_{ijk} = x_{ij} \cdot x_{ik}$. With z_{ijk}, constraint (6) becomes,

$$\sum_{i=1}^{T} z_{ijk} \leq 1 \tag{9}$$

The objective of the ILP model is to minimize the total test time of all sessions:

$$\text{Minimize} \sum_{j=1}^{N_{up}} t(L_j) \tag{10}$$

Both L_j and $t(L_j)$ are variables, we need to linearize the objective function so that any commercial ILP solver can be used. A new binary variable δ_{jq} ($1 \leq j \leq N_{up}$, $0 \leq q \leq r$) is introduced:

$$\delta_{jq} = \begin{cases} 1 & \text{if session } S_j \text{ contains } q \text{ TSVs} \\ 0 & \text{otherwise} \end{cases} \tag{11}$$

Therefore, $t(L_j) = \sum_{q=0}^{r} \delta_{jq} \cdot t(q)$. In addition, two following constraints should be included in the model:

$$L_j = \sum_{q=0}^{r} q \cdot \delta_{jq} \tag{12}$$

which indicates that a session can have 0 to r TSVs, and

$$\sum_{q=0}^{r} \delta_{jq} = 1 \tag{13}$$

indicating that the size of a session should be unique. For every session S_j, there will be exactly one value of q for which $\delta_{jq} = 1$. Therefore, δ_{jq} determines the size of S_j. We can rewrite the objective function as

$$\text{Minimize} \sum_{j=1}^{N_{up}} \sum_{q=0}^{r} \delta_{jq} \cdot t(q) \tag{14}$$

The testing time for different session size $t(q)$ is a constant obtained from SPICE simulation as shown in Table I. Thus, the objective function is linearized.

The complete ILP model is summarized in Figure 2. The number of variables and number of constraints determine the complexity of the model as $O(N_{up}^2 T)$. For the example of Section II, the ILP model produces 4 optimal test sessions in less than 3 seconds. Note that a globally optimal set of sessions is not guaranteed by this ILP model since the model is based on Condition 1, which is a non-necessary condition for solving Problem 1.

Obviously, the sessions generated by the ILP model guarantee that all TSVs can be identified if the total number of faulty TSVs in a TSV network does not exceed m. If there are more than m faulty TSVs within a network, then

Objective:

$$\text{Minimize} \quad \sum_{j=1}^{N_{up}} \sum_{q=0}^{r} \delta_{jq} \cdot t(q)$$

Subject to:

1) $x_{ij} + x_{ik} - z_{ijk} \leq 1; \quad \forall i \in [1, T], \forall j \neq k \in [1, N_{up}]$

2) $x_{ij} + x_{ik} - 2z_{ijk} \geq 0; \quad \forall i \in [1, T], \forall j \neq k \in [1, N_{up}]$

3) $\sum_{i=1}^{T} z_{ijk} \leq 1; \ \forall j \neq k \in [1, N_{up}]$

4) $L_j = \sum_{i=1}^{T} x_{ij}; \ \forall j \in [1, N_{up}]$

5) $0 \leq L_j \leq r; \ \forall j \in [1, N_{up}]$

6) $\sum_{j=1}^{N_{up}} x_{ij} \geq m+1; \ \forall i \in [1, T]$

7) $L_j = \sum_{q=0}^{r} \delta_{jq} \cdot q; \ \forall j \in [1, N_{up}]$

8) $\sum_{q=0}^{r} \delta_{jq} = 1; \ \forall j \in [1, N_{up}]$

Fig. 2: ILP model for finding near-optimal test sessions with specified identification capability.

with the use of sessions produced by the ILP model two possible situations may occur. First, not all TSVs can be uniquely identified as either good or bad. Second, all TSVs are identified but the number of faulty TSVs is larger than m. In both situations, we conclude that there are more than m faulty TSVs within the network and the chip not repairable. Therefore, the sessions provided by the ILP model can always help make the right decision to either replace the identified bad TSVs or discard the chip as having too many faulty TSVs within a local silicon area.

IV. Experimental results

We compare the total test time and total number of sessions for the proposed ILP model, the heuristic method [10], and sequential TSV testing. The *relative test time ratio* in this section refers to the ratio of the test time to the time of sequential TSV testing. We only show cases where relative test time ratio is smaller than 100%. Thus, for the cases not shown, sequential test of each TSV is more time-efficient than the other two methods. The ILP model is solved using a commercial solver named CPLEX from IBM [1]. In all situations, the solver outputs the results in less than 40 seconds.

Figure 3 shows the relative test time ratio for both ILP model and heuristic method considering various resolution constraints $r \in [2, 4]$ and values of $m \in [1, 4]$ in a 20-TSV network. Note that the test time from ILP model is always less than that from the heuristic method. The percentage shown with each pair of bars is the relative test time improvement of ILP model over heuristic. As can be seen from Figure 3, for a given r, the relative test time ratio for both methods increases as m increases since pinpointing larger number of defective TSVs requires more sessions and takes longer time. For the same m, larger r offers smaller test time ratio because then a session can hold more

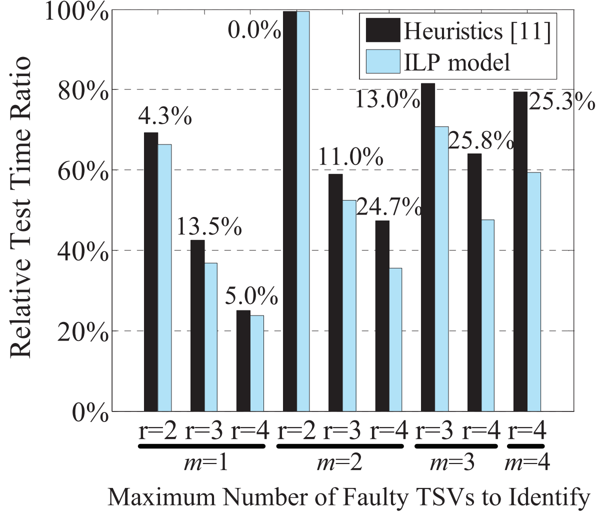

Fig. 3: Test time comparison between ILP model and heuristic method [10] for a 20-TSV network.

TSVs with less test time. Moreover, the total number of sessions generally decreases for larger r. Also, note that ILP model always helps reduce test time further compared to the heuristic method and the improvement generally increases as m increases. Thus, for small m the heuristic may behave well but as m increases the quality of the heuristic method deviate farther away from the optimal result. The largest improvement of ILP model over heuristic method reaches 25.8% which happens when $T = 20$, $m = 3$ and $r = 4$.

Figure 4 examines the impact of the number T of TSVs within a network on the relative test time ratio. We simulate 4 networks of different sizes with $m \in [1, 4]$ and r fixed at 3. As can be seen the ILP model reduces test time further compared to the heuristic method regardless of the value of T. This relative improvement can be as large as 38.2% shown on top of the pair of bars corresponding to $T = 11$, $m = 2$. It is interesting to observe that the relative test time ratio of ILP model remains consistent across different values of T for a given m. While for the heuristic method, the test time ratio varies a lot for different network sizes. For example, when $m = 2$, the relative test time ratio from the heuristic method for an 11-TSV network is much larger than those for other networks. The unstable performance of the heuristic method is mainly due to its greedy nature of generating test sessions. These observations suggest that the proposed ILP model is more robust across variations of TSV network parameters and thus could eliminate the need for redesign and optimization of each individual TSV network on chip as required in the heuristic method [10].

We show the total number of test sessions generated by the two methods for 4 different networks in Figure 5 where r is fixed at 4 and $m \in [1, 4]$. The percentage on top of each pair of bars represents the relative reduction in the number of sessions from ILP model over heuristic method. As expected, generally a smaller number of sessions is produced for smaller m. For a larger TSV network, it is possible to reduce test time with number of test sessions larger than the total number of TSVs (i.e., T). As can be seen, the ILP model sometimes produced the same number of sessions as the heuristic. However, our experimental results demonstrate that though the number of sessions produced by both methods may be the same, the sessions themselves are different. Sessions produced by ILP model are guaranteed to be more time-efficient. For example, for $T = 8, m = 1, r = 4$ and $T = 8, m = 2, r = 4$, the ILP model produced same number of sessions as the heuristic but with test time reduced by 5.8% and 12.5%, respectively. In most cases, ILP model helps reduce total number of sessions compared to the heuristic. For example, for $T = 16, m = 4, r = 4$, 4 out of 24 sessions were eliminated representing a 16.7% relative reduction.

V. Conclusion

An ILP based model is proposed to generate near-optimal set of test sessions for pre-bond TSV testing. Extensive experiments demonstrate that the ILP model always reduces pre-bond TSV identification time compared to that of a previous heuristic method. Moreover, the test time reduction of the ILP model remain consistent for various TSV networks, and thus eliminates the need for separately designing and optimizing each TSV network as required in the previous work. The proposed ILP model is expected to significantly reduce pre-bond TSV test cost in real silicon. Our model

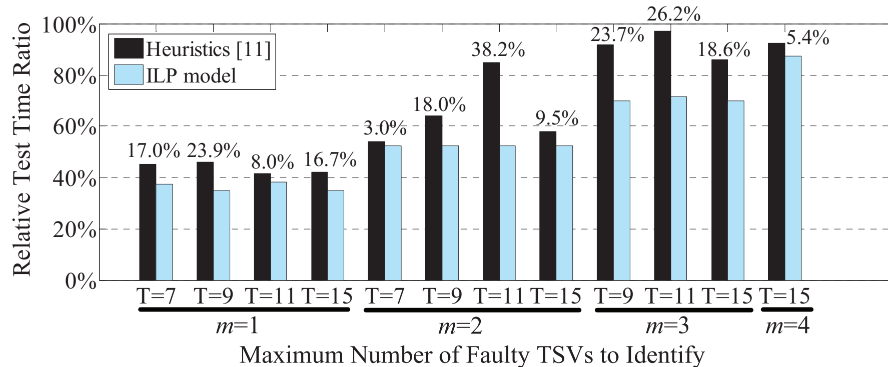

Fig. 4: Test time comparison between ILP model and heuristic method [10] for resolution constraint $r = 3$.

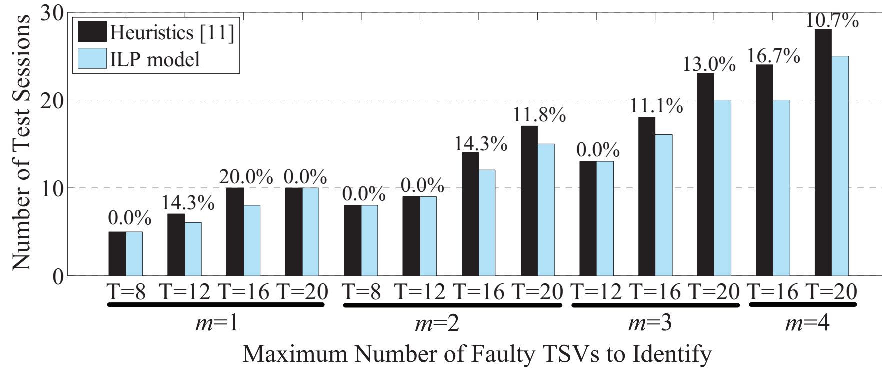

Fig. 5: Comparison of number of sessions from ILP model and heuristic method [10] for resolution constraint $r = 4$.

is based on a sufficient but non-necessary condition for test session generation, which still leaves room for future explorations, such as, possibly finding a necessary and sufficient condition to generate globally optimal set of sessions.

The proposed technique is applicable to TSV redundancy architecture where any identified faulty TSV can be replaced by any redundant TSV in the same network. Another possible limitation of the technique is that sharing of redundant TSVs among TSV networks is not considered. This needs further examination.

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