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Editorial

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The topics discussed in this issue are verification and validation, software testing, hardware security, radio frequency noise measurement and wafer-level testing. The first paper here comes from the IEEE 24th Latin American Test Symposium (LATS), Veracruz, Mexico, 21–24 March, 2023.

The first three articles discuss verification and validation. In the first paper, a circuit graph partitioning followed by a probabilistic procedure translate bit faults into signal errors. Further analysis leads to a clustered probability binomial reliability (CPBR) model that allows estimation of correctness rate of the primary output signals. Authors are Goudet, Sureau, Breuil, Treviño, Naviner, Daveau, and Roche from LTCI, Télécom Paris, Institut Polytechnique de Paris, Palaiseau, France and Technology Design Platforms, STMicroelectronics, Crolles, France.

The second article is authored by Georgoulopoulos, Mamali, and Hatzopoulos from Aristotle University of Thessaloniki, Thessaloniki, Greece. They present a method to verify mixed-signal circuit designs using System Verilog.

The third article is contributed by Rashid, Gauhar, and Hasan from National University of Sciences and Technology (NUST), Islamabad, Pakistan and Abed and Ahmad from Kuwait University Kuwait. They observe that floating point arithmetic hardware units can produce errors in the processing of conditions like overflow, truncation, and similar. The paper examines the correctness of such units using, unum, a universal number representation format and a theorem proving system.

The fourth article addresses the problem of optimizing software test cases by examining the impact of tests for function, performance, security, and reliability on software quality. The presented solution relies on entropy-based optimization and machine intelligence. Authors are Tamizharasi and Ezhumalai from R. M. D. Engineering College, Kavarapettai, Thiruvallur, Tamil Nadu, India.

The fifth article develops a genetic algorithm to derive tests for detecting Trojans that are otherwise difficult to detect because they are placed on low-activity signals. Contributors are Chakraborty and Sen from National Institute of Technology, Durgapur, India, Ghosh from Pennsylvania State University, USA, and Mondal from Asansol Engineering College, India.

The sixth article designs a low noise radio frequency (RF) source for an X-band pulsed Doppler radar. A phase locked loop (PLL) stabilizes the RF oscillator. The paper then details a random vibration (RV) test for phase noise measurement that is relevant to the application. Authors are Kumar from Bharat Electronics Limited, Bengaluru, Karnataka, India and Ghosh from National Institute of Technology, Patna, Bihar, India.

The seventh article presents a cost optimization procedure for wafer-level tests. Reducing tests causes test escapes but increasing them to prevent escapes may cause yield loss. Thus, an optimal tradeoff is required. The paper accomplishes this goal by using a random forest predictor trained with data from randomly selected dies, and another parameter known as bad neighbor ratio (BNR). A 42% reduction in testing cost is observed. This work is reported by Pan, Liang, Li, Qu, Huang, Yi and Lu from Hefei University of Technology, Hefei, China.

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