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# Diagnosis of Analog and Digital Circuit Faults Using Exponential Deep Learning Neural Network

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**Abstract**
With advanced technology, the latest Very Large Scale Integration (VLSI) circuit designs are manufactured. In advanced technology-centered circuits, new design-specific, as well as feature-sensitive failure mechanisms are on the rise; those failures are named faults. These faults could make the circuit behave abnormally and could be of any kind. Therefore, locating as well as detecting these faults becomes essential for the circuit's analysis and enhancement. The challenges are not fully solved even though the prevailing models gave several ideas for detecting faults. A novel methodology for Fault Diagnosis (FD) with Fault Location Identification (FLI) and optimal VLSI circuit design recovery was proposed in this methodology to tackle these issues. The signals with the frequency response are collected initially in the proposed methodology. The proposed Kendall Ensemble Empirical Mode Decomposition (KEEMD) algorithm, which decomposes the signal, is utilized to pre-process the obtained signals. Subsequently, the features like mean, Standard Deviation (SD), kurtosis, skewness, Relative Entropy (RE), and minimum and maximum values are retrieved as of the decomposed signal. For the circuit FD, the extracted features are provided as input to the Exponential Deep Learning Neural Network (EDLNN). Next, the fault locations are identified as of the diagnosed fault. The Interpolated Aquila Optimizer (IAO) algorithm optimally recovered the fault circuit subsequent to the identification. Centered on performance measures, the proposed scheme's performance is analyzed with existent models in experiential analysis. It is concluded that better results were attained by the proposed schemes than the prevailing models.

**Keywords** Very Large Scale Integration (VLSI) · Kendall Ensemble Empirical Mode Decomposition (KEEMD) · Exponential Deep Learning Neural Network (EDLNN) · Interpolated Aquila Optimizer (IAO) · Optimal circuit recovery

## 1 Introduction

For elevating the reliability of diverse systems like aircraft apparatus, biomedical devices, and satellites operating in remote harsh environmental conditions, designing circuits with the ability to detect and correct faults is vital [31]. If any of these applications have faults, the entire system's functionality could be destroyed. With the technology's advancement, Integrated Circuits (IC) complexity is elevated. The IC's size reduction is caused by technological innovation. By this, the design is made compact along with more susceptible to transient faults [12]. Hard faults and soft faults are the '2' faults classifications. Analog circuits occasionally have hard defects that include open circuits and short circuits. Soft faults, which represent the deterioration of circuit component properties, triggered many analog circuit defects [19]. Open or short faults are classified as catastrophic faults. A parametric fault or soft fault is a deviance of a circuit component values as of its nominal value [20]. Thus, the severely required strategy is fault detection. Typically, fault Feature Extraction (FE) and fault pattern classification are the two steps involved in the traditional data-driven FD. It is well understood that FE is a significant

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step. By encompassing time-domain analysis methodologies, frequency-domain analysis methodologies, time–frequency analysis methodologies, along with information entropy approaches, numerous FE algorithms have been created [32]. A severe testing process is conducted in a few manufacturing units. For instance, to validate whether every chip is free of manufacturing defects, production tests are executed at the VLSI manufacturing procedure's end. Testing an IC externally utilizing Automatic Test Equipment (ATE) becomes highly complicated with the advancement of recent design along with packaging technologies in VLSI [9]. A highly efficient low-cost solution was provided by the Design for Testability (DFT) techniques [27]. However, the testing of fault condition detection needs an advanced approach. The circuit is recovered after that. The design's sensitive areas are essential to be detected before recovering the circuit as of the faulty condition using these techniques. It has a high probability of getting altered into an error along with affecting the circuit's normal operation if a fault is identified in a sensitive area. Unessential overheads like computational overheads together with costs will be eliminated during elevating the circuit's reliability by recognizing sensitive areas along with exploiting suitable fault-tolerant methodologies [4]. Market pressure of modern VLSI chips was generated by the elevation in logic density, speed, along with time, so it is necessary for the manufacturers to raise the yields. A vital step in separating similar defective net locations is FD, therefore defect identification and elimination could be executed [33]. For instance, intelligence technologies encompassing expert system schemes, fuzzy theory, Artificial Neural Networks (ANN), as well as Support Vector Machines (SVM) were applied by experts to construct multi-classification models for FD [28]. But, the problems were not entirely solved yet. So, a novel approach centered on fault and fault location detection with optimal VLSI circuit design was proposed in this scheme. Some examples of fault types in digital and analog signals are given as follows,

***Digital Faults***

**Stuck-at Fault:** A digital signal line is stuck at a particular logic level (0 or 1).
**Bridging Fault:** Two or more signal lines are short-circuited, causing unintended signal coupling.
**Transition Fault:** A fault that affects the timing of signal transitions, resulting in incorrect data propagation.
**Gate-Level Fault:** A fault that occurs within a logic gate, causing incorrect gate behavior or output.

***Analog Faults***

**Gain Fault:** A fault in an analog amplifier that causes an incorrect gain factor.
**Offset Fault:** A fault that introduces an unwanted DC offset in an analog circuit, resulting in biased outputs.
**Nonlinearity Fault:** A fault that causes the response of an analog circuit to deviate from its ideal linear behavior.
**Frequency Response Fault:** A fault that alters the frequency response of an analog circuit, causing distortion or attenuation.

### 1.1 Problem Definition

Improvement is still needed to solve the FD and FLI issues even though many ideas were provided by the prevailing research methodologies. The prevailing scheme's issues are enlisted as,

- Owing to the circuit structure's complexity and variability, there is a lack of reliable and practical fault modeling methods for circuits.
- The circuit component's parameter values are unremitting.
- The tolerance and nonlinear nature issue's impact cannot be negligible.
- The limitations for actual circuits were test points.
- Some discrete simulation data, that affect the system's performance, were utilized for testing in most of the prevailing research models.
- The test pattern generation procedure followed by the prevailing research methodologies requires a huge storage capacity for recording total test responses for all faults.

In order to resolve these shortcomings, the proposed method developed a novel approach based on fault and fault location detection with optimal VLSI circuit design. The main motive of the proposed methodology is to address both fault detection and fault diagnosis in VLSI circuits. The signals collected from the circuit undergo pre-processing using the KEEMD algorithm, and features are extracted from the decomposed signals. These features are then used as input for fault diagnosis, where an EDLNN is employed to determine the presence of faults, and then the locations, where the faults are present, are identified. Finally, the IAO algorithm is utilized to optimize the recovery of the faulty circuit based on the identified fault locations.

Thus, the efficient FD and FLI approach with an optimal VLSI circuit recovery system was proposed with better accuracy and diminished complexity by pondering all the above-addressed drawbacks.

The presented research is structured as, in section 2, the related existing research methodologies are explained, the proposed research methodologies are illustrated in section 3, in section 4, the experimental analysis is given, and in section 5, the paper is concluded along with future enhancement.

## 2 Related Work

Sanyal et al. [23] suggested a model that identified equivalent faults in analog circuits. Anamalgamation of Direct Current (DC) operating point analysis along with Alternating Current (AC) analysis of the Circuit Under Test (CUT) was utilized in this combination. In the course of post-silicon testing, the faults were detected by this approach. The approach's effectiveness in identifying equivalent faults was exposed in this study. Higher fault coverage was attained in this approach with noticeably abated computation. High fault coverage was achieved by utilizing the Fault Classification (FC) along with input signal synthesis. This classification significantly covered most of the detectable faults. However, more time was taken for bigger circuits.

Nirmalraj et al. [18] presented a technique to distinctively recognize any single stuck-at faults location along with fault type. When analogized with prevailing models, the number of test configurations was significantly diminished by the Walsh code methodology. A series of ISCAS'89 benchmark circuits implemented in distinct Field Programmable Gate Array (FPGA) families executed the method's extensive testing. The simulation outcomes suggested that fault detection and diagnosis required a maximal number of configurations. It was noted that the total number of test configurations was abated by the methodology. Since the methodology was analyzed with less number of circuits, the approach was not reliable.

IshraqulHuq et al. [10] recommended '2' Single-Ended Ring Oscillator (SERO)-centered Transistor Stuckon (TSON) FD models for Complimentary Metal–Oxide–Semiconductor (CMOS) circuits. In methods 1 and 2, the SERO was utilized as a current-controlled and voltage-controlled oscillator, respectively; thereby abating the detection block's circuit head. The outcomes exhibited that TSON faults in the CMOS circuit were successfully detected by both methods centered on the SERO's oscillatory behavior. Performance issues were raised if the approach utilized the Built-In Current Sensors (BICS).

Gao et al. [6] implemented a Reed–Solomon Erasure Codes (RS-EC) decoder on an FPGA. Grounded on partial re-encoding for the faults in the RS-EC decoder's user memory, a fault detection and location scheme was presented. The analysis exposed that most faults were detected by this scheme with tiny missing and false detection probability. The experiential outcomes suggest that the decoder tolerated more than 90% of faults in user memory. Consequently, all the faults were accurately located by the fault location scheme.

Srimani et al. [29] presented a testing technique for identifyingparametric faults in analog circuits grounded on the 'Kolmogorov–Smirnov' (K–S) test. When the circuit's input was a random analog signal, the time-domain signal processing approach was the method, which analogized statistical similarity regarding the 'Empirical Cumulative Distribution Function' (ECDF) of the circuit's outputs. The functional metric's tolerances were mapped to the CUT's components by the Multivariate Adaptive Regression Splines' (MARS) scheme. A good agreement with the simulated outcomes was exhibited by the experiential outcomes. The system's performance was affected since the K-S test was more sensitive to deviations near the distribution center rather than at the tails.

Kuen-Jong Lee et al. [14] recommended a diagnosis pattern generation procedure to identify equivalent Transition Faults (TF) efficiently. It also engendered a very compacted diagnosis pattern to differentiate non-equivalent TF. Two major methods were comprised in this procedure to obtain very compact diagnosis patterns. Owing to Automatic Test Pattern Generator (ATPG) backtracking limit, those two methods handled very few fault pairs. The experiential outcomes suggest that this was the first work for differentiating all diverse TF along with identifying all equivalent TF for ISCAS'89 and IWLS'05 benchmark circuits. Grounded on the TF model, some inaccuracy was caused by the approach's effect in any diagnosis model.

Vinod Kumar Khera et al. [11] recommended a heuristic approach to abate the test vector count. It was executed during VLSI testing of standard ISCAS circuits. The test vector's numbers requisite for testing were augmented with the dwindling die-space along with elevating circuitry on a single IC. The circuit's total testing cost was directly affected by the number of test vectors. Here, retrieving child test vectors along with merging them diminished the test vectors. The test vector count was diminished by this scheme, which was tested by single stuck-at-fault models successfully. The scheme's effectiveness was illustrated by the obtained outcomes.

Takahashi et al. [30] suggested a magnetic field emitted as of Large Scale Integration (LSI) to assess the on-chip Power Supply Network (PSN) grounded on up-to-date estimation. From the magnetic field measurement outcomes, the actual current flowing in the network was estimated in this method. It also facilitated us to detect design faults like VIA/wire disconnections and/or current concentration in a non-invasive and low-cost way. Utilizing an electromagnetic field simulator, the experiential outcomes suggest that the current flow in the supply network was accurately predicted by the model. Dedicated on-chip current sources for signal injection into the PSN were needed by the Design Under Test (DUT) in the presented scheme, which was the major drawback that may end in non-negligible hardware overhead.

Gaber et al. [5] introduced a fault detection model for extracting features along with FD as of large-sized digital circuits grounded on Deep Learning (DL). Engendering Test patterns utilizing ATALANTA software, feature reduction employing Stacked Sparse Autoencoder (SSAE), and classification for FD were the '3' phases comprised in this model. For the unsupervised learning phase, test vectors were

employed in SSAE as training data. By altering the SSAE network's architecture along with sparsity constraint, the FE's performance was tested. The experiential outcomes revealed that maximal fault coverage of 99.2% utilizing the ATALANTA tool was delivered by employing ISCAS'85. Better outcomes were provided by SSAE only if the data was bulky. Here, the outcome was not reliable as the system was trained by the research methodology with fewer data.

Rahaman et al. [21] presented a technique under the Missing Gate Fault (MGF) model for FD along with fault location in a reversible combinational circuit. Initially, a universal test set of length that detects whole Partial MGF (PMGF), all Single MGF (SMGF), and all detectable Repeated-Gate Faults (RGF) were derived in a reversible combinational circuit, which was with the Controlled-Not (k-CNOT) gates. Here, hardware overhead was elevated in this method, not requiring ATPG. A technique was presented under the SMGF scheme for locating the faulty gate.

Luo et al. [15] suggested an FPGA-centered analog FD system by implementing 2D information fusion, two-port network analysis, together with interval math theory. Initially, Since the embedded algorithms were executed in parallel on FPGA, higher processing speed along with smart circuit size were provided by it. Secondly, good compatibility was exhibited by the hardware structure with other diagnostic algorithms. Finally, flexibility was enhanced by the equipped Ethernet interface for remote monitoring as well as controlling. The experiential outcomes acquired as of '2' realistic example circuits signified that the competitive performance in both diagnosis accuracy and time-effectiveness, with about 96% accuracy within 60 ms computational time, was attained by methodology. It was computationally complex.

Mondal et al. [17] developed FD along with a localization scheme for the prevailing MGF models in Reversible Circuits (RC). Here, Test vectors (T) were computed initially followed by engendering a unique test set (U) by executing an algorithm. The faults of any type prevailing in the circuit could be detected by applying them after engendering the test set (U). For all sorts of MGF namely SMGF, PMGF, and MMGF, this approach was successfully tested. The testing policies were executed over a wide spectrum of benchmarks to verify the functional correctness of the scheme along with cross-checking the experiential findings. With the prevailing works, the attained outcomes were analogized and enhancements were reported.

Hari M. Gaur et al. [7] presented a redundant logic-grounded framework for designing fault-tolerant RC. The scheme was grounded on the testable circuits' development that generates an error signal in the course of any fault existence, which was further employed to realize fault-tolerant circuits. Corresponding double and tri-modular redundant fault-tolerant circuits were implemented to perform the experiments on benchmark circuit sets. With the efficient prevailing approaches, comparisons were provided. The presented approach elevated the test overheads.

Hari Mohan Gaur et al. [8] propounded an effective design for a testability scheme for the stuck-at FD in RC by utilizing the Toffoli and Fredkin gates' properties. When analogized to the prevailing work in the area that evidences its effectiveness towards the diminish in hardware cost with diminished degradation in speed, a set of benchmark circuits was acquired for experimentation where the presented framework attained a diminish of up to 25:0% in gate cost and 35:8% in quantum cost. For the presented approach, quantum delay, testing, and design complexity were high.

Arabi et al. [3] recommended a multiclass Adaptive Neuro-Fuzzy Inference System (ANFIS) classifier for FC in analog IC. Analog circuits' FD suffering from inaccurate FC was assisted by this approach along with diminishing the computational burden. A high level of efficiency was revealed by the obtained outcomes with an accuracy average attaining a higher level. When analogized with both the ANN framework and the Fractional Fourier Transform (FRFT) methodology grounded on a statistical property, better performance was exhibited by the approach regarding FC accuracy. Owing to the complex structure and gradient learning, the suggested ANFIS required a high computational cost.

## 3 Proposed Fault and Fault Location Diagnosis with Optimal VLSI Circuit Recovery System

A fault is pondered as an error that causes unfavourable effects and is an abnormal state at the system level or device. If the system or device cannot resume a stable operational state, it is said to be faulty. FD system is therefore required. A novel method for fault FD was proposed by this research scheme, which also pondered fault location identification to recover the mild and medium fault circuits. Frequency response collection with signal, pre-processing by KEEMD, FE, FD by EDLNN, FLI, and the ideal VLSI circuit recovery system by IAO are the proposed methodologies' six phases. Figure 1 shows the proposed methodologies' block diagram.

### 3.1 Frequency Response Collection

Grounded on the circuit's nature and operator frequencies, the circuit's frequency response is acquired in the first stage by sweeping a fixed input signal with a defined frequency range. Thus, the circuit's signal is defined as,

$$\begin{aligned} &S_s = \{r_1, r_2, r_3, ....., r_n\}, \quad (or) \\ &S_s = r_i, i = 1, 2, 3, ....., n \end{aligned} \tag{1}$$

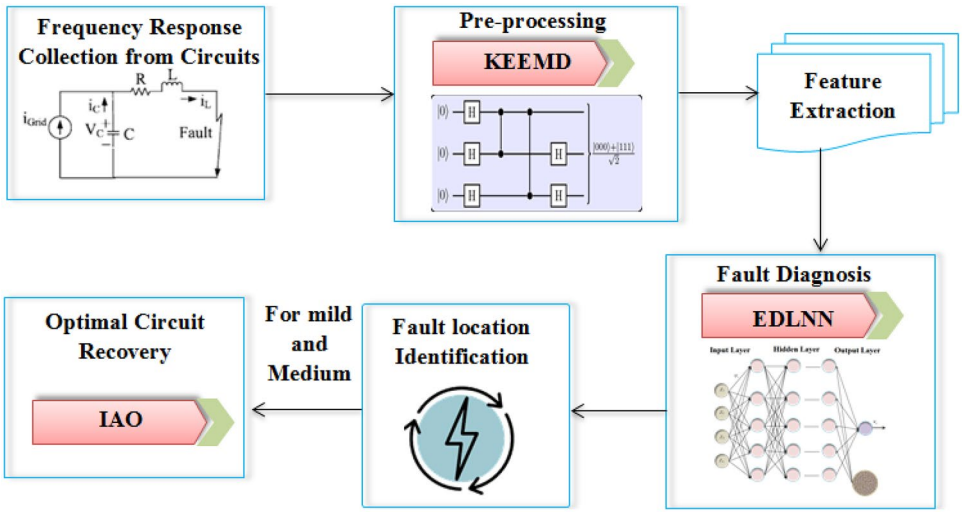


**Fig. 1** Block diagram for the proposed research methodology

where, the circuit's signal set with frequency level is defined by $S_s$, and the n-number of signals is indicated by $r_n$.

### 3.2 Pre-Processing

The mode fusing issue of EMD was addressed by the Ensemble Empirical Mode Decomposition (EEMD), which is an enhancement of EMD. To create the Intrinsic Mode Functions (IMFs), the EMD's ensembles are combined with the white noise of finite amplitude. The added noise dissipates equally in the entire time–frequency plane; thereby the problem of mode mixing is resolved. The EEMD algorithm is employed to decompose the input circuit signals into IMFs' components. A better result was provided by the EEMD, but the random addition of the white noise's amplitude leading to additional trials is the issue, which exacerbates the mode mixing issue. The Kendall rank correlation between all the input signals is computed in this model to tackle this issue. Later, the better value is added as white noise. This sort of process minimizes the number of trials along with improving the EEMD algorithm's performance. The modification is therefore known as the Kendall EEMD (KEEMD). The proposed algorithm's steps are given as follows,

**Step 1:** Initially, the white noise time series, which is computed by the Kendall rank correlation $\mu_n(t)$ is utilized for generating new time series that is given as an input signal $r_i(t)$,

$$T_n(t) = r_i(t) + \mu_n(t) \tag{2}$$

where, $n = 1, 2, ...., N$ with $N^{th}$ ensemble number.

**Step 2:** By utilizing EMD,the acquired signal is decomposed into IMFs as:

$$T_n(t) = \sum_{p=1}^{L_q} h_{pq} + u_{L_q} \tag{3}$$

where, the $q^{th}$ trial's $p^{th}$ IMF is denoted as $h_{pq}$, the residue of $q^{th}$ trial is notated as $u_{L_q}$, and $q^{th}$ the trial's IMFs number is denoted as $L_q$.

**Step 3:** For $H$ trials, steps (2) and (1) are repeated. A distinct white noise series is summed in each trial to the input signal.

**Step 4:** By averaging the decomposition's corresponding IMFs, the decomposed signal's final outcome is computed that is denoted as $h_p(t)$:

$$h_p(t) = \frac{\left(\sum_{q=1}^{H} h_{pq}\right)}{H}, \; p = 1, 2, ....., K \tag{4}$$

where, the minimum number of IMFs among all the trials is signified as $K$.

### 3.3 Feature Extraction

The features are retrieved from the decomposed signals after pre-processing. Kurtosis, skewness, RE, mean, SD, minimum, and maximum values are the features extracted here.

**Relative Entropy ($\chi_1$):** The distance measured betwixt two probability distributions on a random variable is named RE. It is also known as the Kullback–Leibler divergence. The RE's derivation is given as,

$$\chi_1 = \sum l(x) \log \frac{l(x)}{m(x)} \tag{5}$$

where, the RE value is defined as $\chi_1$, and the two probability distribution on the random variable is indicated as $l(x)$ and $m(x)$.

**Mean** ($\chi_2$)**:** The arithmetic average is the decomposed signal's mean values. The mean calculation is given as,

$$\chi_2 = \frac{1}{z}\sum h_p \tag{6}$$

where, the mean value is represented as $\chi_2$, and the total number of acquired decomposed values is defined as $z$.

**Standard Deviation** ($\chi_3$)**:** The SD for the IMF components is defined as,

$$\chi_3 = \sqrt{\frac{\sum \left(h_p - \chi_2\right)^2}{z-1}} \tag{7}$$

**Skewness** ($\chi_4$)**:** The symmetry or asymmetry in the Distribution Function (DF) is identified by a standard named Skewness. It is measured as zero if the DF is symmetrical. The skewness measure is positive for higher values along with negative for lower values if the DF is asymmetrical. This is defined as,

$$\chi_4 = \frac{\chi_2}{\chi_3^3} \tag{8}$$

**Kurtosis** ($\chi_5$)**:** The curve's sharpness at maximal value is recognized by a standard named Kurtosis, which defines the normal distribution as,

$$\chi_5 = \frac{\chi_2}{\chi_3^4} \tag{9}$$

**Min and Max:** The minimum $\chi_6$ and maximum values $\chi_7$ are selected as of the decomposed values.

### 3.4 Diagnosis of Fault

Using an EDLNN, the fault is identified in this section by the features gathered. A special type of Machine learning algorithm is Artificial Neural Networks (ANNs). In order to identify a novel pattern, nonlinear statistical models called ANNs exhibit a complex relationship betwixt inputs and outputs. The Input Layer (IL), the Hidden Layer (HL), and the Output Layer (OL) are the three layers comprised in ANN. But, in a traditional neural network, the weights connecting the neurons are initialized with random values. However, selecting the perfect random weight values can be time-consuming, and the selected values may not always be reliable. To address this issue, the research methodology proposes a weight adjustment approach using exponential values for the neurons. The exponential values for the neurons are summed up, and the resulting sum is divided by the total number of neurons in the hidden layer. This process helps calculate the weight values in a more systematic manner. Thus, the proposed EDLNN differs from the existing technique in terms of adding a weight adjustment approach. Figure 2 gives the proposed EDLNN structure.

The input features are primarily accepted by the input layer. Information as of the outside world is provided to the network by this layer. In this layer, no computation is executed, only the input features are forwarded to the subsequent layer. HL, which is also known as an intermediate layer, is the succeeding layer where the computations are eventuated. It acts as an intermediate layer between the input and OL and its calculation is provided as,

$$ID_i = bias + \sum_{i=1}^{n} \chi_i . \psi_i \tag{10}$$

where, *bias* refers to an additional parameter that is added to each neuron in the network. The bias term allows the neural network to shift the activation function's curve, enabling the network to learn and represent more complex patterns and relationships betwixt inputs and outputs. During the training process, the network adjusts both the weights and biases to minimize the error betwixt predicted outputs and the desired outputs. The biases, similar to weights, are updated through an optimization algorithm, such as gradient descent, to improve the network's performance. The HL is denoted as $ID_i$, $\chi_i$ signifies the input data, and the particular layer's weight value is denoted as $\varepsilon_i$. The layer's weight value is computed as follows,

$$\psi_i = \sum \frac{e^{on_i}}{n} \tag{11}$$

where, the neuron's exponential value is symbolized as $e^{on_i}$. By summing all the input values weights ($n$), the output unit is computed to attain the neuron's values in the OL.

$$v_i = bias + \sum_{i=1}^{n} ID_i . \psi_i \tag{12}$$

where, the output unit is indicated as $v_i$, and the loss functio ($SS$) is computed utilizing the Eq. (13),

$$SS = (G_t - v_i) \tag{13}$$

where, the NN's target output is signified as $G_t$. The threshold that is set for the loss function is the minimum value. A further trial is executed if the loss function doesn't meet the threshold value. As the research methodology utilized the weight value by pondering the layer's neurons, more trials are not required. By utilizing the computed features as of the input signal collections, the circuit is diagnosed as the fault circuit (or) normal circuit by the proposed EDLNN.

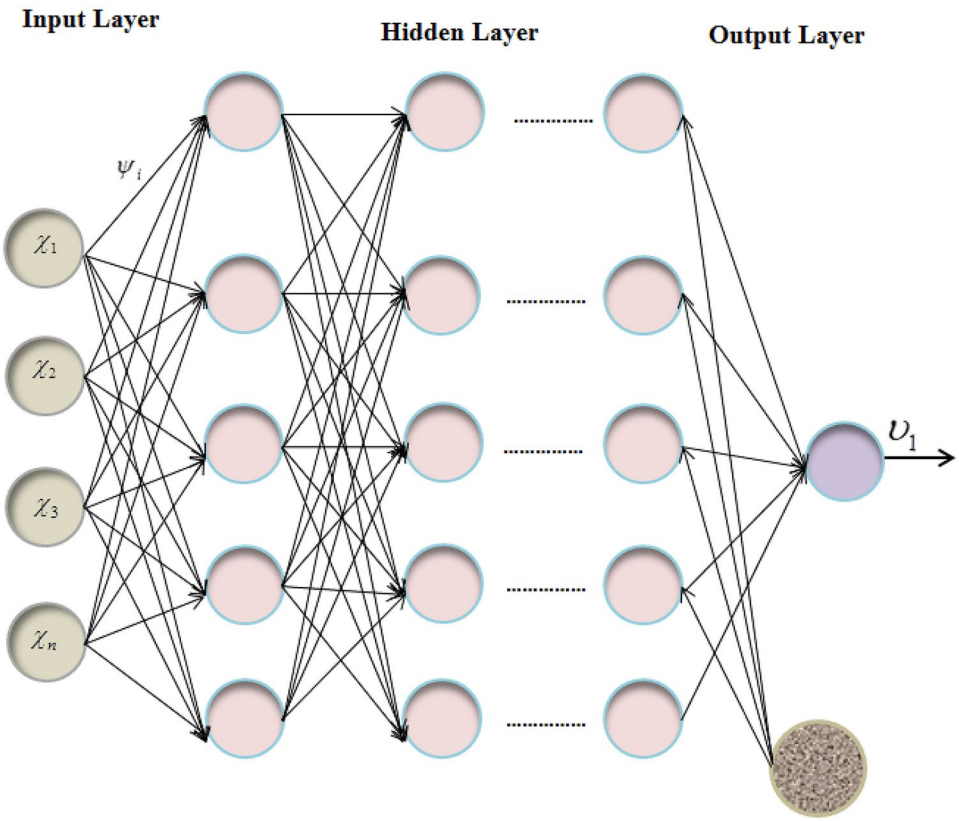


**Fig. 2** Structure of the EDLNN algorithm

### 3.5 Fault Location Detection

Later, less frequency response is pondered as of the signal to detect the fault location if the circuit has a fault. The sensitive area is computed as,

$$F_l = \frac{N_{lf}}{O_{lf}} \tag{14}$$

where, the fault location is signified as $F_l$, the number of fewer frequency responses is symbolized as $N_{lf}$, and the total number of fewer frequency responses is signified as $O_{lf}$. Finally, the fault's effectiveness is identified as of the probability of area. The fault is identified as severe if the probability of area is high. The fault is moderate if the probability is medium. If the probability is low then it is identified as mild.

### 3.6 Optimal VLSI Circuit Recovery

A VLSI Circuit recovery system aims to detect and diagnose faults in both digital and analog circuits. By recovering the faulty VLSI circuit using an optimal design, the reliability of the circuit is significantly enhanced. The faults that caused the circuit to malfunction are rectified, leading to a more stable and reliable operation. Thus, the circuit is recovered using the optimal design if the fault is moderate and mild; otherwise, the circuit is separated. Here, the Interpolated Aquila Optimizer (IAO) is employed to recover the circuit. Here, the VLSI circuit's recovery components are optimized; also, the reduction of delay, wire length, and area are deemed as fitness functions. The optimum global issues are solved by a swarm intelligence–centered approach named AO. Aquila's prey-hunting capability is the inspiration of a population-centered optimization technique, which is named AO. Its local exploitation capabilities are inadequate even though it has significant global exploration capabilities. Therefore, the interpolation process is utilized by this methodology in the expanded exploitation updation process. Four hunting strategies were utilized by them. They also have the capacity to switch between them. The population (i.e., VLSI components) ($y$) is initially initialized for the candidate solution, which is provided as follows,

$$Y = \begin{bmatrix} y_{1,1} & \cdots & y_{1,D} \\ \cdot & & \\ \cdot & & \\ y_{N_p,1} & \cdots & y_{N_p,D} \end{bmatrix} \tag{15}$$

Then, the population ($Y$) is generated randomly by utilizing (16),

$$Y_{k,1} = \gamma\left(U_b - L_b\right) + L_b,\ k = 1, 2, ...., N_{p,1} = 1, 2, ...., D \tag{16}$$

where, the random value is indicated as $\gamma$, the upper bound value is represented as $U_b$, the lower bound value is modelled as $L_b$, the total population size is signified as $N_p$, and the number of decision variables is signified as $D$.

**Expanded exploration:** The prey's location might be recognized by the Aquila, which also flies widely exploring the prey:

$$Y_k(t+1) = Y_e(t) \times \left(1 - \frac{t}{M_t}\right) + Y_m(t) - Y_e(t) * \eta \tag{17}$$

where, the $k^{th}$ individual's position is denoted by $Y_k(t+1)$ at $t+1$ iteration, the optimal location at the current iteration is signified as $Y_e(t)$, the random number in Gaussian distribution is denoted as $\eta$ within an interval of 0 and 1, the maximal permitted iteration number is specified as $M_t$, and all individuals' mean positions are notated as $Y_m(t)$ at the current iteration:

$$Y_m(t) = \frac{1}{N_p}\sum_{k=1}^{N_p} Y_k(t) \tag{18}$$

**Narrowed Exploration:** The prominent hunting method utilized for Aquila is this.Itattacks the prey by utilizing the short gliding after descending within the chosen area along with flying around the prey. The formula for a position update is illustrated as:

$$Y_k(t+1) = Y_e(t) \times \mu + Y_p(t) + (q - p) \times \eta \tag{19}$$

Here, $\eta$ is the random number, the Aquila's random position is depicted as $Y_p(t)$ along with the levy flights are defined as $\mu$ that could be computed as:

$$\mu = c \times \frac{m \times \sigma}{|n|^{\frac{1}{\delta}}} \tag{20}$$

where, a constant parameter is expressed as $c$ and $\delta$, random numbers between 0 and 1 are illustrated as $m, n$, and $\sigma$ is computed as follows:

$$\sigma = \frac{\Gamma(1+\delta) \times \sin\left(\frac{\pi\delta}{2}\right)}{\Gamma\left(\frac{1+\delta}{2}\right) \times \delta \times 2^{\frac{\delta-1}{2}}} \tag{21}$$

The spiral shape in the search is presented by utilizing the $qq$ and $pp$ in the narrowed exploration, which is calculated as follows:

$$pp = \eta \times \sin(\theta) \tag{22}$$

$$qq = \eta \times \cos(\theta) \tag{23}$$

$$\eta = \gamma + V \times D_1 \tag{24}$$

$$\theta = -\varpi \times D_1 + \frac{3\pi}{2} \tag{25}$$

where, the constant number is denoted as $V$ and the fixed constant number is notated as $\varpi$.

**Expanded exploitation:** When they fail to identify the target during the exploitation process, Aquila might reinitialize them. Then, they update their positions with the following equation:

$$Y_i(t+1) = \beta \times \left[\left(Y_e(t)\right)_{nw} + \frac{\left(Y_e(t)\right)_{nw+1} - \left(Y_e(t)\right)_{nw}}{\left(Y_m(t)\right)_{nw+1} - \left(Y_m(t)\right)_{nw}}\right] + \tau \times \left[\left(U_b - L_b\right) \times \gamma + L_b\right] \tag{26}$$

Here, two fixed numbers are symbolized as $\beta$ and, $\tau$ the new best location is indicated as $\left(Y_e(t)\right)_{nw}$, and another one best location is defined as $\left(Y_e(t)\right)_{nw+1}$. Thus, the interpolation process is defined as the new location consideration phase.

**Narrowed exploitation:** It has walking and grabbing prey behavior. Here, the prey is chased by Aquila in the light of its escape trajectory along with attacking the prey on the ground. This behavior mathematical representation is given as follows:

$$Y_i(t+1) = Q_f \times Y_e(t) - \left(T_1 \times Y(t) \times \gamma\right) - T_2 \times \mu + \gamma \times T_1 \tag{27}$$

where, the quality factor is specified as $Q_f$, which is computed as,

$$Q_f = t^{\frac{2\gamma-1}{(1-M_t)^2}} \tag{28}$$

The variations of motion are indicated as $T_1$ and $T_2$, which are derived as follows,

$$T_1 = 2\gamma - 1 \tag{29}$$

$$T_2 = 2\left(1 - \frac{t}{M_t}\right) \tag{30}$$

The VLSI circuit was optimally recovered by utilizing this algorithm. Figure 3 depicts the proposed algorithm's pseudo code. The algorithm's fitness function along with the updation procedure is provided here.

## 4 Result and Discussion

The proposed FD and FLI's performance is analyzed with the prevailing models. In the MATLAB Simulink platform, the proposed research methodology is implemented. By the

**Fig. 3** Pseudocode for IAO algorithm

**Input:** Components of the circuit design
**Output:** Optimal circuit

**Begin**

**Initialize** population $Y_{k,1}$, iteration $t$ and maximum iteration $M_t$

**Calculate** fitness function

**Set** iteration $t = 1$

**While** $(t \le M_t)$ **do**

**Recognize** the location of the prey by ,

$$Y_k(t+1) = Y_e(t) \times \left(1 - \frac{t}{M_t}\right) + Y_m(t) - Y_e(t) * \eta$$

**Update** position by the help of random position $Y_p(t)$

**Update** the position in expanded exploitation by using interpolation procedure, $(Y_e(t))_{mv} + \frac{(Y_e(t))_{mv+1} - (Y_e(t))_{mv}}{(Y_m(t))_{mv+1} - (Y_m(t))_{mv}}$

**Attack** the prey at narrowed exploitation using eq. (27)

**End while**

**Calculate** fitness

**Set** $t = t + 1$

**Return** optimal components for circuit design

**End**

benchmark circuits like ITC'99, IWLS'05, etc., the system's performance is analyzed.

**ITC'99 dataset:**The ITC'99 benchmark dataset includes various industrial-scale circuits used for testing and evaluation purposes. It comprises a set of circuit designs from different application domains, such as microprocessors, memory circuits, and digital signal processors. These circuits are typically representatives of real-world VLSI designs [34].

**IWLS'05 dataset:**The IWLS'05 benchmark dataset is focused on logic synthesis and optimization problems. It consists of a set of combinational logic circuits with different sizes and complexities. These circuits are primarily used for evaluating logic synthesis and optimization algorithms [35].

Both datasets provide circuit-wise information, including circuit netlists, gate-level descriptions, and associated fault models. Additionally, they often come with predefined sets of test patterns and fault coverage information, which was used for evaluating the performance of FDandFLI techniques.

**Implementation details** The proposed methodology for FD and FLI in VLSI circuits can be implemented using MATLAB R2022a and Simulink. The implementation can leverage the processing capabilities of an Intel Core i5 processor running at a speed of 3.30 GHz. The operating system used for the implementation is Windows 10, and the system has 8 GB of RAM.

### 4.1 Performance Analysis of Fault Diagnosis

Here, the proposed EDLNN's performance is analyzed with the prevailing DL Neural Network (DLNN) [24], Convolutional Neural Network (CNN) [22], Recurrent Neural Network (RNN) [2], and ANN [16].

Grounded on FD, Table 1 illustrates the proposed and prevailing research model's performance analysis. Precision, recall, F-measure, along with accuracy are the performance measures analyzed in this table. For any machine learning process, the vital metrics are accuracy and precision. A system is identified as a good system if those vital metrics' values are good. Grounded on the measures, superior performance was attained by the proposed methodology than the existent schemes. Contrarily, when analogized with the proposed and other existent algorithms, the worst performance was obtained by the ANN algorithm. Thus, the table concludes that the enhancements

**Table 1** Demonstrate the performance of the proposed and existing methodologies

| Measures | Proposed EDLNN | DLNN | CNN | RNN | ANN |
|---|---|---|---|---|---|
| Precision | 97.2 | 89.36 | 85 | 79.89 | 77.6 |
| Recall | 97.6 | 89 | 88.6 | 82 | 76.95 |
| F-Measure | 97.3 | 89.17 | 86.76 | 80.9 | 77.27 |
| Accuracy | 99.21 | 92 | 86.35 | 81 | 75.5 |

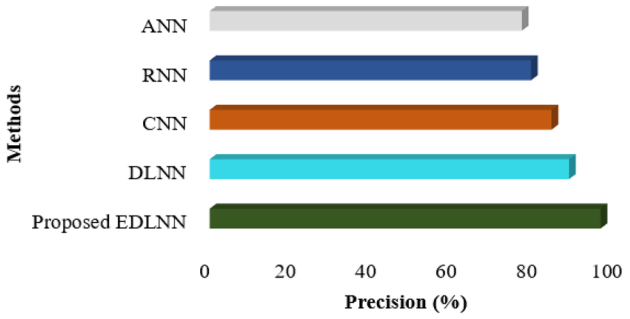


**Fig. 4** Pictorial representation of precision analysis

centered on the proposed research attain superior performance than the prevailing schemes.

Figure 4 displays a pictorial representation of the proposed EDLNN and the existing method's precision analysis. The ratio of precisely detected positive signals to the total predicted positive signals is named precision. A higher precision value of 97.2% was achieved by the proposed EDLNN than the prevailing methods. But, 89.36%, 85%, 79.89%, and 77.6% were the precision values for DLNN, CNN, RNN, and ANN, respectively. Here, lower values were obtained by the prevailing models than the proposed scheme. The analysis concludes that the proposed EDLNN-centered FD is better than the prevailing methodologies.

The proposed EDLNN's recall analysis with the existent DLNN, CNN, RNN, and ANN is displayed in Fig. 5. The measure of the number of positive classes correctly predicted by the classifier over all the positive classes in the data is named recall. A higher recall of 97.6% was achieved by the proposed system than the other models. A higher performance of 89% was attained by the DLNN, which is greater than the prevailing models but not higher than the proposed one because the proposed methodology attains 9.66% higher than the prevailing DLNN. It is concluded from the analysis that higher outcomes than the prevailing models were attained by the proposed EDLNN-centered FD approach, which proves the enhancement's goodness Fig. 6.

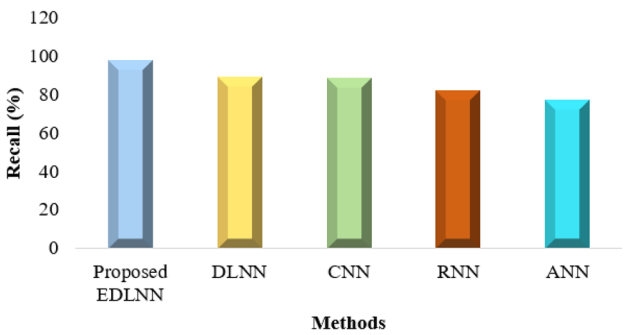


**Fig. 5** Recall Analysis

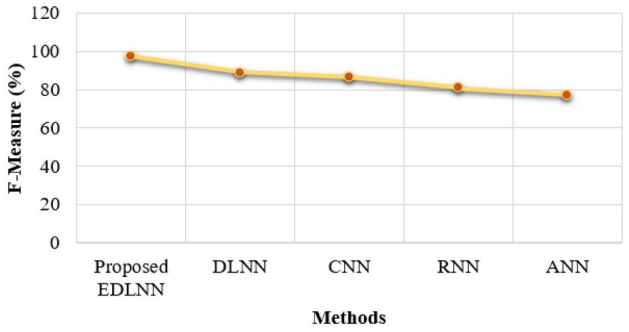


**Fig. 6** Graphical analysis of the F-Measure measure of the proposed and existing methodologies

The F-measure analysis for the proposed EDLNN-based FD system's graphical plot is analyzed with the prevailing algorithm-based FD. The harmonic mean of precision and recall corresponded with the F-measure. By this definition of the F-Measure metric centered on the precision as well as recall metric, high performance is achieved by the proposed EDLNN. So, this F-measure-based analysis doesn't require any description. When contrasted with the prevailing algorithms, a higher F-measure value of 97.3% was attained by the proposed EDLNN. But, the prevailing algorithms show an F-measure value of 89.17%, 86.76%, 80.9%, and 77.27%. Thus, a superior outcome was provided by the proposed methodology's performance for FD.

Figure 7 displays the graphical plot for the analysis of the proposed EDLNN-based FD process with the prevailing algorithm. The most intuitive performance measure named accuracy is the ratio of correctly predicted signals to the circuit's total signals. The main metric for any kind of system is accuracy. The proposed scheme is signified as the best model for FD if the accuracy is high. The proposed methodology attained an accuracy of 99.21%, which is higher than the prevailing schemes. Whereas the prevailing schemes like DLNN, CNN, RNN, and ANN achieved 92%, 86.35%, 81%, and 75.5% of accuracy, respectively.

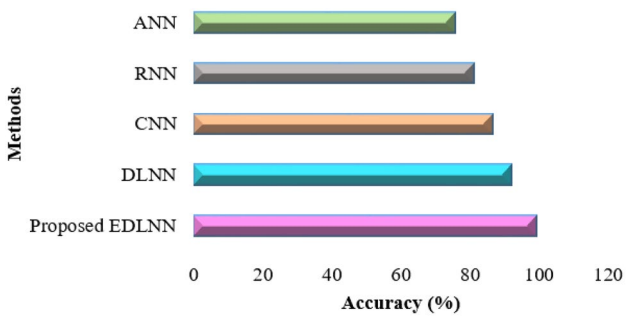


**Fig. 7** Pictorial plot for the proposed EDLNN with the existing methods based fault diagnosis process

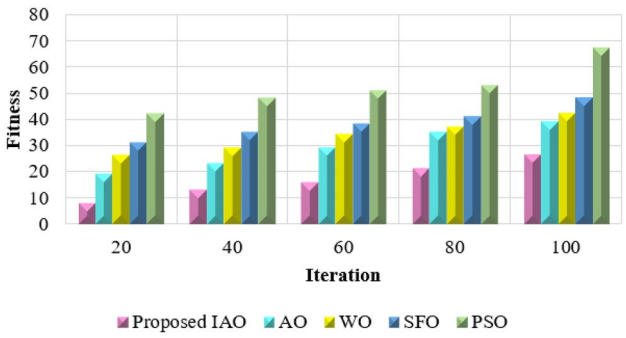


**Fig. 8** Fitness Vs iteration analysis

Here, the proposed model is 7.83% more than the prevailing DLNN algorithm. Finally, the accuracy's pictorial representation proves that a better FD is obtained by the EDLNN algorithm.

### 4.2 Performance Analysis of Optimal Circuit Recovery

Based on fitness vs iteration analysis, the proposed IAO's performance is analyzed with the existent Aquila Optimizer (AO) [13], Whale Optimization (WO) [25], Sailfish Optimization (SO) [26], and Particle Swarm Optimization (PSO) algorithm [1] in this section.

The proposed IAO's fitness vs iteration is analyzed with the prevailing algorithm-centered optimal VLSI circuit recovery design system and is displayed in Fig. 8. The vital fitness in the research methodology is minimization. The analysis suggests that a superior outcome was attained by the proposed scheme than the existent AO, WO, SFO, and PSO algorithms. As a result, the analysis shows that the proposed algorithm-based optimal VLSI circuit recovery is superior to the prevailing research technique.

The layer details of the proposed EDLNN are given in Table 2.

**Discussion:** The proposed method used an enhanced preprocessing step that improved the quality of the input data and consequently led to more accurate FD and FLI. Likewise, the extraction of important features provides the informative characteristics of the faults present in the VLSI circuits. These extracted features contributed to improved accuracy in fault diagnosis. The EDLNN is used as the fault diagnosis model. The EDLNN efficiently captured complex fault dependencies, resulting in improved performance in FLI. Finally, the IAO algorithm effectively restored the fault circuit to its optimal state, leading to improved circuit behavior and overall performance.

**Table 2** The layer details and its values considered for the proposed EDLNN

| | | |
|---|---|---|
| 1 | Learning Rate | 0.001 |
| 2 | Number of Input Layers | 4 |
| 3 | Number of Hidden layers | 8 |
| 4 | Number of Output layers: | 2 |
| 5 | Number of Neurons per Layer: | 120 |
| 6 | Batch Size: | 10 |

## 5 Conclusion

In any form, a fault in the circuit could be present. Crossing or leaving a net disconnected during manufacture can result in a defective circuit. In this study, the proposed EDLNN method is utilized to diagnose the fault along with identifying the fault location. The IAO algorithm is then utilized to restore the circuit with the aid of identified location. The proposed scheme's performance is analyzed with the benchmark circuits here. Regarding accuracy, precision, F-measure, along with recall, the proposed EDLNN's performance is analyzed with existent DLNN, CNN, DLNN, RNN, and ANN algorithms in the performance analysis. The proposed EDLNN attains an accuracy, precision, recall, as well as F-measure of 99.21%, 97.2%, 97.6%, as well as 97.3%, respectively, which is higher than the existent schemes. Therefore, superior outcomes were attained by the proposed methodology-based fault detection and location identification, which is also well suited for VLSI circuits. The proposed scheme could be enhanced in the future by recovering the severe fault circuits and also with advanced models.

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**Availability of Data and Materials** Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

## Declarations

**Ethical Approval** This article does not contain any studies with human participants or animals performed by any of the authors.

**Consent of Publication** Not applicable.

**Conflict of Interest** The authors declare that they have no conflict of interest.

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