Journal of Electronic Testing (2023) 39:207–225
https://doi.org/10.1007/s10836-023-06051-0

Multiple Retest Systems for Screening High-Quality Chips

Chung-Huang Yeh[1] · **Jwu E. Chen**[1]

Received: 13 August 2022 / Accepted: 6 February 2023 / Published online: 20 February 2023

Abstract
In this study, we develop a digital integrated circuit testing model (DITM) based on a statistical simulation method to evaluate the test quality and yield of integrated circuit products. This model can be used to quantify the characteristics of the device under test (DUT) and simulate the effect of the test guardband (TGB) on test results during testing. The complexity and functionality of integrated circuits have continued to increase over the past two decades. Moreover, the development in speed of automated test equipment (ATE), e.g., OTA or overall timing accuracy, according to the ITRS report, lags behind the progress of semiconductor manufacturing. Hence, using existing instruments and tools to select zero-defect products would be a considerable challenge for suppliers due to the slow development of the testing technology. We propose a new scheme of using multiple retest systems (MRSs) to improve the yield while maintaining the desired quality to address the product quality requirements of consumers. We also use a set of parameters from IRDS 2021 (International Roadmap for Devices and Systems 2021) to estimate the future test yield (Y_t) and test quality through DITM calculations. MRS results showed that the test yield (Y_t) can be improved while achieving the expected quality. MRSs not only improve the performance of the tester but also demonstrate effective performance in the yield improvement of high-quality products. This approach enables high-quality, high-yield chip delivery, and significantly increases the overall profit of the company.

Keywords Zero defect · Guardband test · Test specification · Defect level · Test quality

1 Introduction

This paper quantifies the process of wafer fabrication and testing assuming that the characteristics of wafer products are normally distributed and applies the digital integrated circuit test model (DITM) [1–4] to estimate the test yield (Y_t) and quality of integrated circuit (IC) products. The rate of progress in future manufacturing is unpredictable. Therefore, we use current manufacturing techniques and the electrical characteristics of existing products to estimate the distribution trend of future product yields.

The ultimate goal of semiconductor manufacturing is to produce zero-defect [5–9] and high-quality IC products. In particular, the automotive electronics industry, which has high safety requirements, has extremely strict quality requirements. A key indicator of general semiconductor quality uses defects per million to express the failure rate of semiconductor components. However, the defect metric was changed from parts per million (PPM) to parts per billion for some critical parts. Improving the quality of products can reduce abnormal electronic components and improve driving safety. Most current test methods fail to meet the yield and quality needs of the automotive electronics market; thus, suppliers must reevaluate their test plans to find additional cost-effective alternatives to current test methods [10–19]. For example, Teslence Technology Co. Ltd. developed a new test method [10] and applied it to the test production line of ASE Technology Holding Co. Ltd., the world's largest wafer test factory, to improve the test yield (Y_t) of chip products. In addition, the American Automotive Electronics Council (AEC) established the AEC-Q001 [7] specification, which uses the part average testing method to eliminate problematic parts, increase product reliability, and improve the quality of components.

The testing capability has failed to compete with the process capability; thus, if no breakthrough development in the testing method of the chips emerges in the future, then the

Responsible Editor: E. Amyeen

✉ Chung-Huang Yeh
yehsony@gmail.com

Jwu E. Chen
jwu.e.chen@gmail.com

[1] Department of Electrical Engineering, National Central University, No. 300, Jhongda Rd., Jhongli City, Taoyuan County 32001, Taiwan (R.O.C.)

test yield (Y_t) will be increasingly worse due to the inaccuracy of the VLSI tester [20–22]. To solve this problem, we propose an effective multiple retest system (MRS) that utilizes moving guardband testing to improve test yield (Y_t) and test quality (DL, defect level), thus realizing the high-quality zero-defect goals required for avionics and biomedical electronics through cost estimation and effective retesting.

We use data from the 2021 International Roadmap for Devices and Systems (IRDS) [23] table and the DITM model to estimate future yield trends and apply the test–retest method to chip testing (zero defect) with strict quality requirements (biomedical and automotive electronics). Under the feedback of cost calculation, the occurrence of killing errors (α) and missing errors (β) is minimized to reduce unnecessary waste production and decrease testing costs. The improvement of the test yield (Y_t) increases the number of sold chips, which not only improves the chip sale profits of the company but also allows the selling of additional high-quality chips. Therefore, a shortage of materials in the electronics industry has been encountered considering the impact of global semiconductors caused by the COVID-19 epidemic. The retest method not only improves the performance of semiconductor test equipment but also enhances the test yield (Y_t) and increases the global supply of semiconductor chips.

2 Manufacturing and Testing Errors of Semiconductor Wafers

The development sequence of an IC is changed from a design concept in the design house to circuit design. Wafer fabrication is then conducted at the wafer foundry and the IC is finally sent to the test house for analysis (Fig. 1). Chemical concentration, etching, and mask errors [20, 21] in the wafer foundry manufacturing process result in the loss of manufacturing yield (Y_m). In addition to environmental factors in the foundry manufacturing process, tester accuracy, and test methods during test house testing can affect yield and quality.

In the process of IC development and manufacturing (Fig. 2), assuming that we have manufactured N number of chips, the chips can be divided into good and bad parts according to the formulation parameters of the design specification (DS). The manufacturing yield (Y_m) after chip foundry manufacturing can be expressed as $Y_m = G/N$. This yield is then sent to the testing house for analysis. The test specifications (TS) provided by the manufacturer can be divided into two types: pass (P) and failure (F) parameters. If the testing process is perfect, then the ATE tester can classify products into good and bad, which respectively pass and fail the test. In this case, the test yield (Y_t) and the manufacturing yield (Y_m) will be the same. Test errors are caused by instrument errors or measurement uncertainty, causing killing errors (α) and missing errors (β). Missing errors (the number of bad chips that pass the test) can lead to product returns and affect the image of the company. Killing errors (the number of good chips that fail tests) increase product cost and yield loss and reduce corporate revenue margins.

2.1 Calculation of Chip Manufacturing Yield (y_m)

In general traditional statistical analysis, the normal distribution is a theoretical pattern and distribution type that is often used because of its accuracy. Let N (x; μ, σ) denote the probability density function of a normal distribution for a random variable X with mean μ and standard deviation σ. The probability density function of the normal distribution is expressed as

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{1}{2}\left(\frac{X-\mu}{\sigma}\right)^2} dx \tag{1}$$

After hundreds of semiconductor manufacturing procedures, the chip delay time has a probability distribution rather than a fixed value due to uncertain changes in the process. Herein, we assume that the delay time of the device

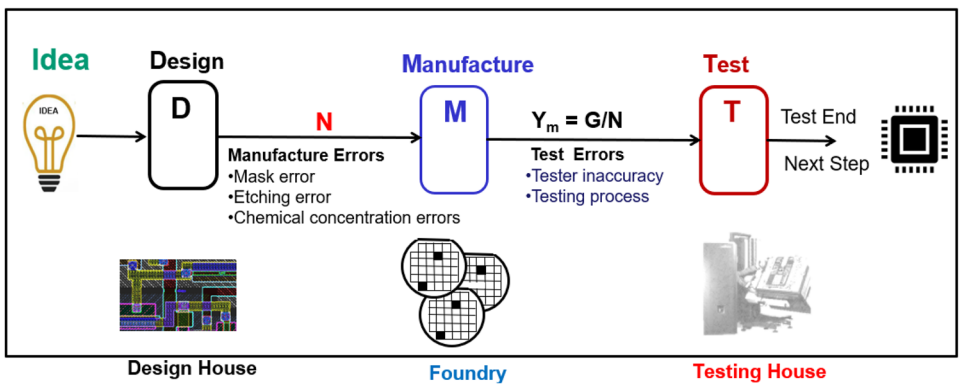

Fig. 1 Process and test errors in the IC manufacturing process

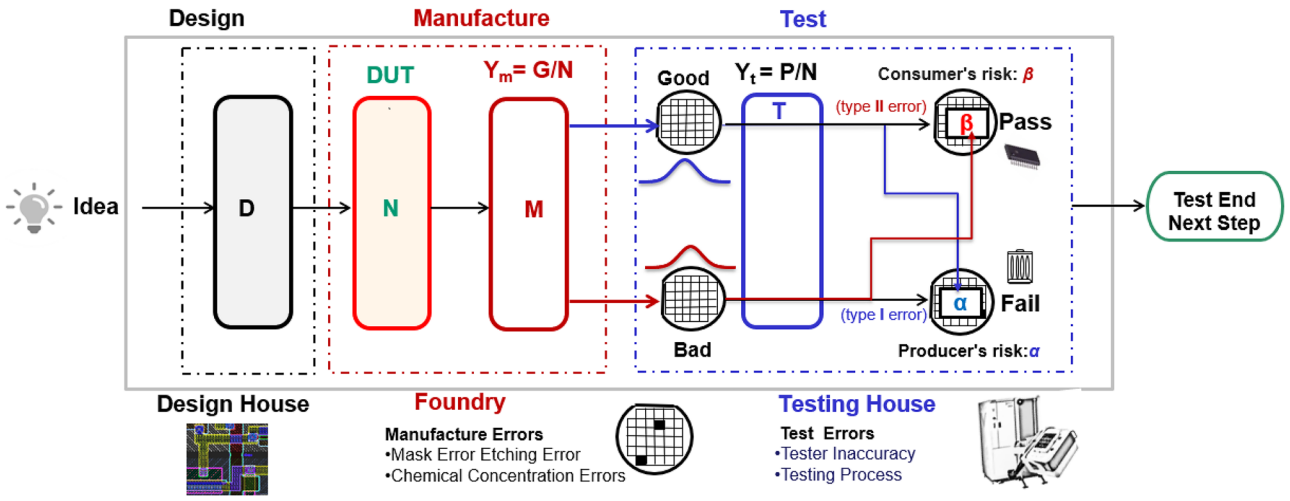

Fig. 2 Test flow and errors for semiconductor ICs

under test (DUT) is normal, that is, Chip (x) = N (x; μ_M, σ_M), mean μ_M and standard deviation σ_M. The Y_m (manufacturing Yield) is the probability of the area under the normal curve between the coordinates $x = -\infty$ and x = DS, that is, $P[-\infty < X < DS]$. We find

$$\begin{aligned} Y_m &= \text{Manufacturing Yield} \\ &= \int_{-\infty}^{DS} \text{Chip}(x)dx \\ &= \int_{-\infty}^{DS} \frac{1}{\sqrt{2\pi}\sigma_M} e^{-\frac{1}{2}\left(\frac{X-\mu_M}{\sigma_M}\right)^2} dx \\ &= \int_{-\infty}^{\frac{DS-\mu_M}{\sigma_M}} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}(x)^2} dx. \end{aligned} \tag{2}$$

Taking the chip circuit as an example, the design house establishes a CPU (central processing unit) with a DS of 0.858 GHz (DS = 1165 ps) and electrical characteristics, including mean μ_M = 1000 ps (picoseconds) and standard deviation σ_M = 100 ps. The chip delay time distribution can be represented by chip X ~ N (x; μ_M = 1000 ps and σ_M = 100 ps). Figure 3 shows the normal distribution of the chip delay time. The horizontal and vertical axes represent the time parameter of circuit characteristics and the probability density of time, respectively. According to the calculation of formula (2), 95% manufacturing yield (true yield) can be obtained $Y_m = P[\text{Good}] = P[X < DS] = 95\%$.

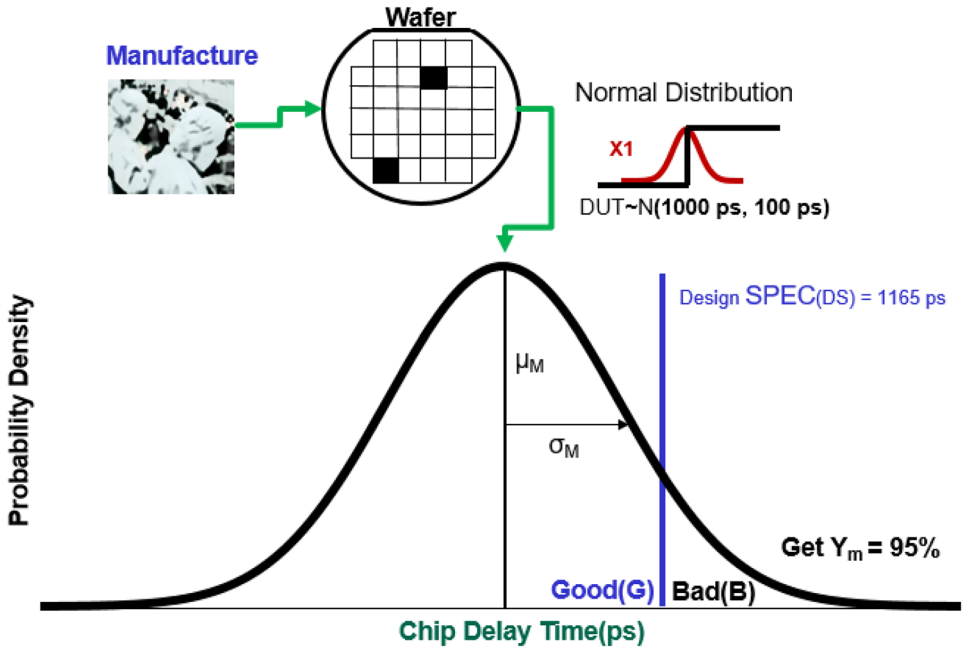

Fig. 3 Manufacturing yield (Y_m) distribution and estimation

2.2 Chip Testing Yield (y_t) Estimation

IC testing contains many projects, including delay testing, parameter testing, and function testing. Additionally, three general categories of defect classes are as follows: (A) bridge, (B) open circuit, and (C) parametric defects. Even between wafers of the same process, there are differences due to process capability. Therefore, the test circuit (Test Key) is often used for testing on the wafer. However, because the chip contains too many parameters, the parameter relationship between each layer is complicated. Although we know that the best test circuit for the chip is itself, the current application test circuit is mainly to monitor the process. Therefore, it is very useful to test the parameters of the circuit to judge whether the chip is good or bad. In general, using key parameters to determine whether a chip is good or bad will not only affect the test cost and speed, but also the final test results. As a result, we refer to the test parameters of chip products and electrical appliances, as well as consider the speed of progress in process capabilities and the development of automated test equipment (ATE) capabilities. Finally, we employed the timing speed parameters of ATE and the delay time parameters of the chip to judge the quality of its wafer products to simplify the calculation of wafer test yield and quality. Figure 4 shows the threshold test system, wherein the signal sent by the IC tester (ATE) is compared with the delayed signal in the ATE. In the tester system model, X1 is the expected chip delay time of the DUT, and X2 (strobe) is the test strobe time as measured by the tester. The two signals are sent to the comparator of the IC tester, which compares the fast, and slow timing to determine whether the chip product is good or bad. Based on the output of the timing comparator, the D-type flip-flop judges the pass and fail of the product. ATE can determine whether the DUT is a "pass" or "fail" chip based on the timing comparison of the two signals. V_{ref} provides an input fixed reference voltage to the comparator, If $\times 1 > V_{ref}$, then $V_0 = V_{cc}$; if $\times 1 < V_{ref}$, then $V_0 = 0$. If the tester signal arrives faster than the chip delay time (X1 > X2), the chip is classified as faulty, and a fault is signaled. Conversely, if the tester signal is slower than the chip delay time (X1 < X2), then the chip is classified as a good part, and the test passes.

Chips after fabrication may produce chips that meet specifications and those that do not meet specifications due to uncertain factors in the semiconductor manufacturing process. We can select the bad chips by using the testing mechanism through the testing steps. However, the signal ST sent out by the ATE tester demonstrates edge displacement due to the inaccuracy of the IC tester (ATE). Therefore, we assume that the performance of the test equipment (tester) is normally distributed in this study. The electrical distribution of the test equipment is $X \sim N(x; \mu_T, \sigma_T)$, (tester) mean μ_T, and standard deviation σ_T. After estimation, the test yield Y_t is calculated as $Y_t = P[pass] = P[X < Y]$ and can be expressed as the following:

$$\begin{aligned}\text{Test Yield} = Y_t(\%) &= P[\text{pass}] = P[x < y] \\ &= \int_{-\infty}^{\infty} \text{Chip}(x) \int_{x}^{\infty} \text{Tester}(y, \mu_T)\,dydx \\ &= \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\sigma_M} e^{-\frac{1}{2}\left(\frac{X-\mu_M}{\sigma_M}\right)^2} \int_{x}^{\infty} \frac{1}{\sqrt{2\pi}\sigma_T} e^{-\frac{1}{2}\left(\frac{y-\mu_T}{\sigma_T}\right)^2} dydx \\ &= \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}(x)^2} \int_{\frac{\mu_M+\sigma_M x-\mu_T}{\sigma_T}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}y^2} dydx\end{aligned} \tag{3}$$

R_{lt}^{1+} indicates that the traditional test method is used to test the DUT but is only tested once.

In the measurement of semiconductor product quality, DL can be used to represent the quality of semiconductor products. DL units are usually defined in PPM, $DL = P[\text{Bad} \mid \text{Pass}] = P[(X > DS) \cap (X < ST)] / P[X < ST]$.

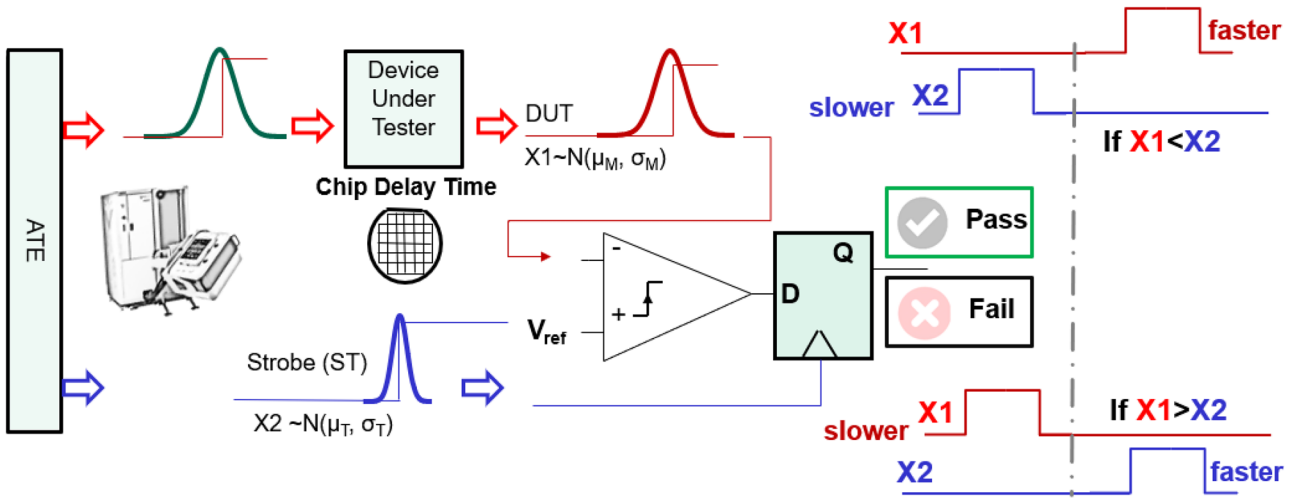

Fig. 4 IC Testing Model

$$\begin{aligned}\text{DL (Defect Level)} &= \frac{\text{P[Bad|Pass]}}{Y_t} \\ &= \frac{\text{Missing Errors}}{Y_t} \\ &= \frac{\int_{DS}^{\infty}\text{Chip(x)}\int_{x}^{\infty}\text{Tester(y)dy dx}}{\int_{-\infty}^{\infty}\text{Chip(x)}\int_{x}^{\infty}\text{Tester(y)dydx}} \\ &= \frac{\int_{DS}^{\infty}\frac{1}{\sigma_M\sqrt{2\pi}}e^{\frac{-(x-\mu_M)^2}{2\sigma_M{}^2}}\int_{x}^{\infty}\frac{1}{\sigma_T\sqrt{2\pi}}e^{\frac{-(y-\mu_T)^2}{2\sigma_T{}^2}}\text{dydx}}{=\int_{-\infty}^{\infty}\frac{1}{\sqrt{2\pi}}e^{-\frac{1}{2}(x)^2}\int_{\frac{\mu_M+\sigma_M x-\mu_T}{\sigma_T}}^{\infty}\frac{1}{\sqrt{2\pi}}e^{-\frac{1}{2}y^2}\text{dydx}}\end{aligned} \tag{4}$$

3 Test Guardband (TGB) Decisions Affect Test Results

The trigger signal ST sent by the IC tester has an edge placement error due to the inaccuracy of the IC tester. In the testing process, the trigger signal sent by the IC tester is faster than the predetermined time of the IC tester, which will increase the probability of test errors in which the good product is judged as the failed product. Conversely, if the trigger signal sent by the ATE tester is slower than the time scheduled by the IC tester, then the probability of test errors for the bad product to be judged as a pass will increase. Therefore, the tester accuracy [24, 25] of the ATE tester must also be considered when using the IC tester to measure the DUT to be tested. The TGB must be emphasized considering the inaccuracy of the tester. Figure 5 shows the TGB, which is defined as the distance between the TS and the DS: TGB = DS − TS [26, 27]. Expanding the TGB (TGB ↑ = DS − TS) indicates changing the TS, which will increase killing errors and decrease missing errors. If the TGB is expanded in this manner, then the test quality (DL) will be improved and the test yield (Y_t) will be decreased. On the contrary, we lowered the TGB (TGB ↓ = DS − TS). Such a small TGB will result in an increase in missing error and a decrease in killing error. Therefore, the test quality (DL) will become increasingly worse, resulting in a large number of customer returns. Thus, the choice of the TGB can be used as a reference for measuring the test yield (Y_t) and test quality (DL).

For example, the circuit characteristic parameters of the chip are X ~ N (x; μ_M = 1000 ps and σ_M = 100 ps) to design a circuit whose design DS = 1165 ps. Following the estimated formula above, the manufacturing yield Y_m = 95% can be obtained. If all are sold at will, then the defect rate DL will reach 50,000 ppm (100,000,000 × 5% = 50,000). Using the ATE tester characteristic parameter OTA = 120 ps, the TS is set to TS = μ_T = 1082 ps (TGB = 1165 − 1082 = 83 ps) through the traditional test method R_{1t}^{1+} and the test yield Y_t = P[Pass] = P[X < ST] = 77.76% and DL = 300 ppm test quality (DL), which is consistent with general central processing unit (CPU) quality.

Conversely, the test yield Y_t = 63.42% and the test quality DL = 10 ppm can be obtained by setting the TS as 1037 ps (TGB = 1165 − 1037 = 128 ps) (Fig. 6 and Table 1). A large TGB guarantees the improved quality of the shipment. Although the number of products that passed the tester test decreased (due to the high rate of killing error), 14.34% (14.34 = 77.76 − 63.42%) loss of test yield (Y_t) was exchanged for high-quality products. Using the traditional test method R_{1t}^{1+} to move the TGB, the test yield (Y_t) and test quality (DL) of the product are interchangeable but not both. Uncertain factors in the semiconductor process, product defects, and inaccuracy and operational problems in the testing process are also observed. Engineers can effectively reduce the defective products to a minimum only when they choose to test the guardband properly.

3.1 Ate Accuracy Affects IC Test Yield and Quality

Next, the chips are sent to the test house for analysis. OTA refers to the accuracy parameter specification of the ATE tester. A small OTA value [24, 25] leads to improved accuracy of the ATE tester. This condition indicates that the testing capability of the tester is superior to the

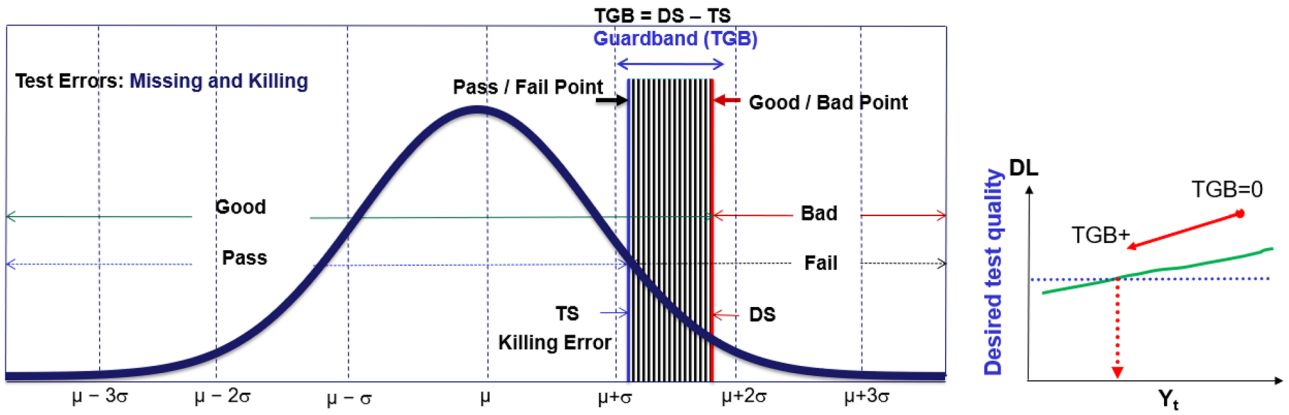

Fig. 5 Setting of the test guardband (TGB) affects the test yield (Y_t) and test quality

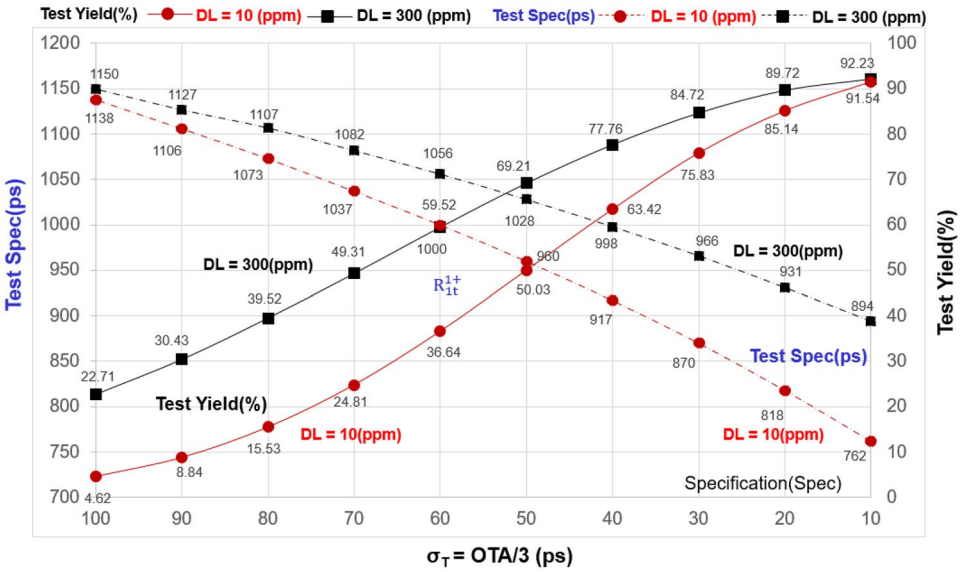

Fig. 6 Test guardband (TGB) affects test results

semiconductor manufacturing capability. Similarly, a large OTA value leads to poor accuracy of the ATE tester, that is, the testing capability is lower than the manufacturing capability. We use different ATE testers below to examine the DUT. Figure 7 and Table 1 show the selected ATE tester characteristic parameter $\sigma_T = 60$ ps (a large σ_T leads to low accuracy) and OTA $= 3 \times \sigma_T = 180$ ps. The product quality is set to DL = 300 ppm and the TS = 1028 ps is used. Through the above estimation formula, the test yield $Y_t = 59.52\%$ can be obtained by the traditional test method R_{1t}^{1+}. A high-precision ATE tester whose characteristic parameters $\sigma_T = 30$ ps (a small σ_T indicates high accuracy) is then selected and the OTA $= 3 \times \sigma_T = 90$ ps. The product quality was maintained at DL = 300 ppm and the DUT was tested using the test parameter TS = 1107 ps. The test yield $Y_t = 84.72\%$ can be obtained through the above estimation formula. The high-precision ATE tester improves the test yield (Y_t) by approximately 25.2% (84.72% − 59.52% = 25.2%).

Taking CPU desktop computer as an example, the quality requirement of DL = 300 − 200 ppm should be acceptable to manufacturers and consumers. However, some products, such as biomedical or automotive electronics, require high-standard quality requirements close to zero defects (10 ppm). Two ways are used to obtain high-quality chip products. Under the OTA = 30 ps test conditions, the first method uses the traditional test method R_{1t}^{1+} and moves the TGB to test the DUT. For example, defect levels are limited to 10 ppm after the foundry fabrication and the TGB is moved and tested using traditional test methods R_{1t}^{1+}. According to the previously estimated formula for the test yield (Y_t) estimation of the product, the test yield (Y_t) drops to 75.83% (Fig. 8) when the TS $\mu_T = 1073$ ps is used. A total of 8.9% (84.72% − 75.83% = 8.89%) of the test yield (Y_t) is lost and a stable and high-quality chip is obtained. High-quality semiconductor chip products can be exchanged for superior and high sales prices, which introduce improved visibility and market reputation to manufacturers. Under the condition of the same product quality DL = 10 ppm, the second method is the ATE tester with high accuracy (a small σ_T leads to high accuracy) $\sigma_T = 20$ ps (the accuracy of the ATE tester OTA $= 3 \times \sigma_T = 60$ ps) and the TS parameters are TS = 1106 ps are set. The test yield $Y_t = 85.14\%$ can be

Table 1 ATE tester to improve the test yield (Y_t)

σ_T = OTA/3	ps	100	90	80	70	60	50	40	30	20	10
OTA	ps	300	270	240	210	180	150	120	90	60	30
Y_m	%	95	95	95	95	95	95	95	95	95	95
DL	ppm	300	300	300	300	300	300	300	300	300	300
μ_T	ps	894	931	966	998	1028	1056	1082	1107	1127	1150
Y_t	%	22.71	30.43	39.52	49.31	59.52	69.21	77.76	84.72	89.72	92.23
DL	ppm	10	10	10	10	10	10	10	10	10	10
μ_T	ps	762	818	870	917	960	1000	1037	1073	1106	1138
Y_t	%	4.62	8.84	15.53	24.81	36.64	50.03	63.42	75.83	85.14	91.54

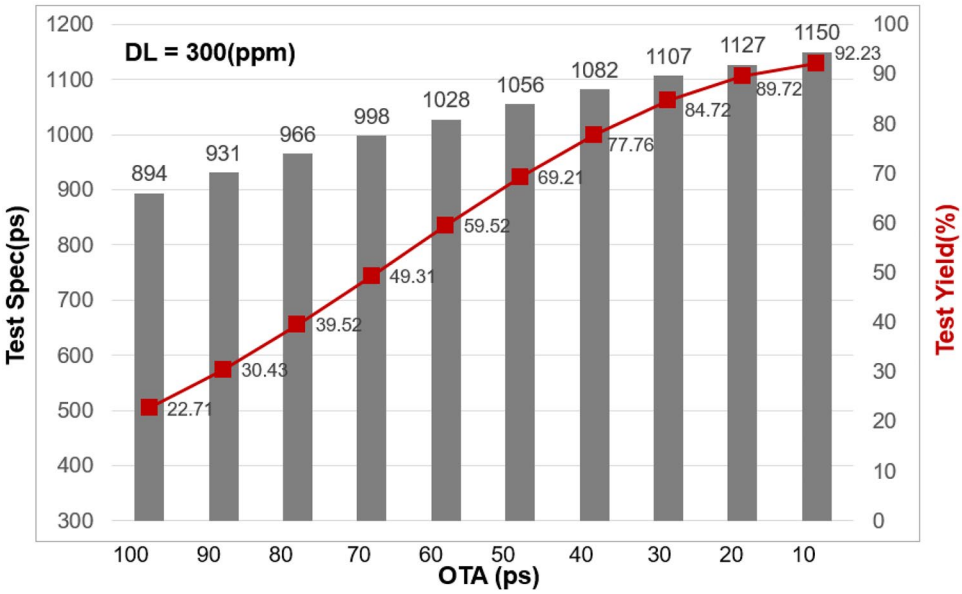

Fig. 7 Test specifications (TS) affect test results under general quality conditions (300 ppm)

obtained through the traditional test method R_{lt}^{1+}, which was approximately 9.31% ($OTA_{20} - OTA_{30} = 85.14 - 75.83\%$) higher than that of the traditional test method R_{lt}^{1+}.

The above results reveal that as the accuracy of the characteristic parameter (OTA) of the tester decreases, the test yield (Y_t) will become increasingly worse and the problems of killing and missing errors will become highly serious. Conversely, the test yield (Y_t) can be improved by approximately 25% when using a high-precision (OTA) tester. However, the price of the ATE tester is high and that of high accuracy (OTA) ATE tester can be as high as several million dollars. The tester adopts an hourly rental system, but an expensive tester raises the rental price. Based on market demand and response, in addition to considering test cost and test yield (Y_t), selecting an appropriate and cost-effective ATE tester according to the circuit characteristics of the DUT to be tested is necessary for test decision-makers.

4 New Scheme of MRS

Critical electronic products require strict quality control to improve product reliability by eliminating all defects in the product population. However, according to the report introduced by the ITRS roadmap, the progress of the IC

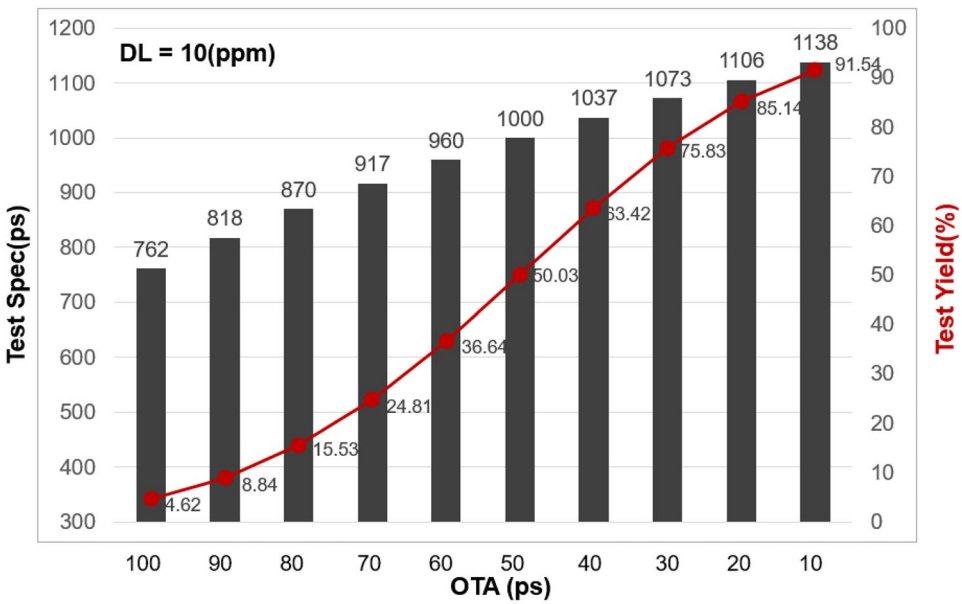

Fig. 8 Influence of test specifications (TS) on test results under conditions of high-quality products (10 ppm)

tester is still slower than that of the manufacturing process. Using existing instruments and tools to select electronic products with high reliability will be a considerable challenge for suppliers due to the slow development of test technology. At present, retesting has been widely used in test production lines to improve the shipment and test yield (Y_t) chips. For example, Horng et al. [12] proposed a two-stage approach to ordinal optimization theory, in which sufficient values are obtained in a reasonable computation time, reducing overkill, and retesting problems. Cheng et al. [11] utilized machine learning algorithms to detect defect-inducing features automatically, thus utilizing re-testing of chips to improve yield. In addition, Selg et al. [13] proposed a method for applying machine learning to predict test–retest effectively. This method is utilized in the manufacture of real products, thus optimizing the manufacturing test time.

Therefore, under the premise of acceptable test costs, to improve product quality and test yield (Y_t), we extended the test time and changed the test conditions and methods to enhance the test yield (Y_t) by re-testing the chip. The decision-making process is shown in Fig. 9. First, starting the first test, all tested chips are divided into Pass DUT (P) part and Fail (F) DUT part. We conditionally retest the parts that pass the test (P) several times. Figure 9 shows the corresponding decision diagram, where the first passing chips were tested N times (i.e., different TS parameters). We call this method the "repeat test method." The test result formula of retest (M_{nt}^{np}) is defined as the following:

$$\begin{aligned}
&\text{Retest Test Yield}(\%)Y_t = (M_{nt}^{np}) \\
&= \int_{-\infty}^{\infty} \text{Chip}(x) \int_x^{\infty} \text{Tester}\left(y, \mu_{T1}\right)dy \int_x^{\infty} \text{Tester}\left(z, \mu_{T2}\right)dz \ldots\cdots \int_x^{\infty} \text{Tester}\left(w, \mu_{Tn}\right)dw\, dx \\
&= \int_{-\infty}^{\infty} \frac{1}{\sigma_M\sqrt{2\pi}} e^{\frac{-(x-\mu_M)^2}{2\sigma_M{}^2}} \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(y-\mu_{T1})^2}{2\sigma_T{}^2}} dy \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(z-\mu_{T2})^2}{2\sigma_T{}^2}} dz \ldots\ldots \\
&\ldots\ldots\ldots\ldots \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(w-\mu_{Tn})^2}{2\sigma_T{}^2}} dwdx
\end{aligned} \tag{5}$$

$$\begin{aligned}
&\text{Retest DL (Defect Level)} \\
&= (M_{nt}^{np}) \\
&= \frac{\text{Missing Errors}}{Y_t} \\
&= \frac{\int_{DS}^{\infty} \text{Chip}(x) \int_x^{\infty} \text{Tester}\left(y, \mu_{T1}\right)dy \int_x^{\infty} \text{Tester}\left(z, \mu_{T2}\right)dz\cdots \int_x^{\infty} \text{Tester}\left(w, \mu_{Tn}\right)dw\, dx}{\int_{-\infty}^{\infty} \text{Chip}(x) \int_x^{\infty} \text{Tester}\left(y, \mu_{T1}\right)dy \int_x^{\infty} \text{Tester}\left(z, \mu_{T2}\right)dz\cdots \int_x^{\infty} \text{Tester}\left(w, \mu_{Tn}\right)dw\, dx} \\
&= \frac{\int_{DS}^{\infty} \frac{1}{\sigma_M\sqrt{2\pi}} e^{\frac{-(x-\mu_M)^2}{2\sigma_M{}^2}} \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(y-\mu_{T1})^2}{2\sigma_T{}^2}} dy \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(z-\mu_{T2})^2}{2\sigma_T{}^2}} dz \ldots\ldots\ldots\ldots .}{\int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}(x)^2} \int_{\frac{\mu_M+\sigma_M x-\mu_{T1}}{\sigma_T}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}y^2} dy \int_{\frac{\mu_M+\sigma_M x-\mu_{T2}}{\sigma_T}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}z^2} dz \ldots\ldots\ldots\ldots .} \\
&\ldots\ldots\ldots\ldots \int_x^{\infty} \frac{1}{\sigma_T\sqrt{2\pi}} e^{\frac{-(w-\mu_{Tn})^2}{2\sigma_T{}^2}} dwdx \\
&\ldots\ldots\ldots \int_{\frac{\mu_M+\sigma_M x-\mu_{Tn}}{\sigma_T}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}w^2} dwdx
\end{aligned} \tag{6}$$

4.1 Flowchart for MRS Decision Making

The application of repeated testing through the actual production line [10] can improve the test yield (Y_t) and quality. However, the test costs will increase with the number of tests. Furthermore, the repeated testing method is unnecessary when the cost of testing outweighs the added profit. Unlimited retesting is also called blind testing, which not only wastes manpower but also increases testing costs. Therefore, the test yield (Y_t) and the test cost must be considered when implementing the retest method. Furthermore, choosing an effective number of retests and avoiding blind retests is necessary to obtain the highest cost-effectiveness. Therefore, under the premise of an acceptable test cost, we have changed the test conditions and methods, extended the test time, and proposed an MRS to retest the chip to improve the test yield (Y_t) of the chip. This test system is based on

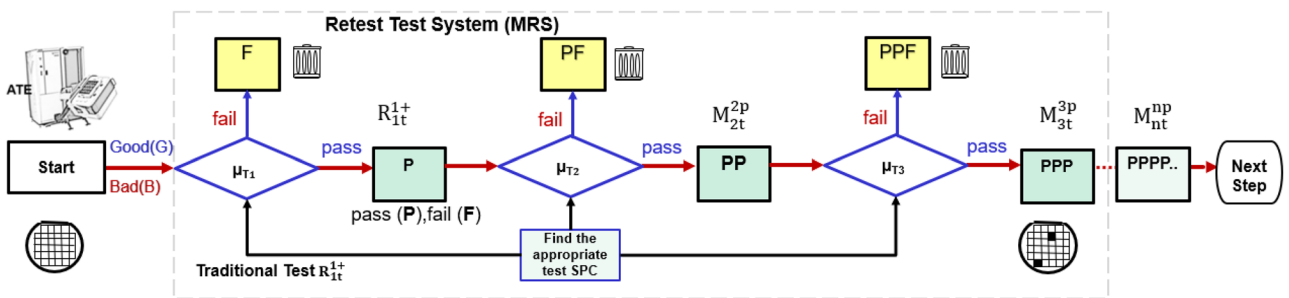

Fig. 9 Decision diagram for the repeat test method

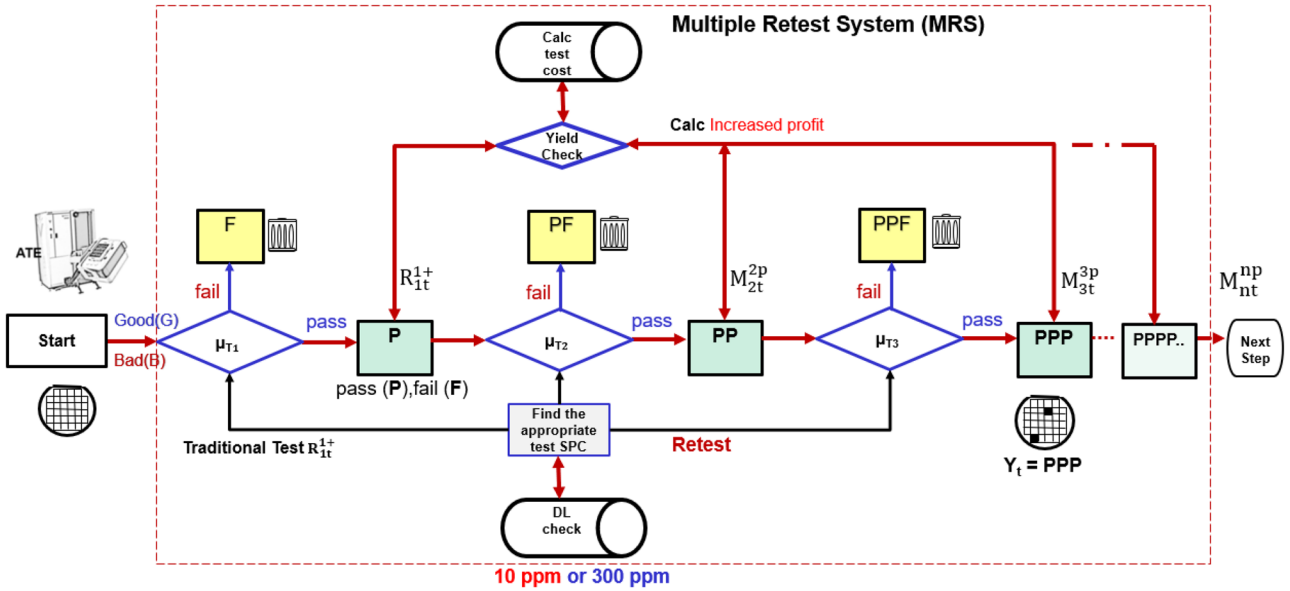

Fig. 10 Flowchart of multiple retest system (MRS) decision making

the test method for retesting (Fig. 9) and adds a mechanism for calculating the profit cost. The optimal number of retests is determined through sequential analysis of the flowchart according to the obtained test cost and test yield (Y_t). The execution steps of the MRS are presented as follows (Figs. 10 and 11).

Step 1 First, we perform the traditional test method R_{1t}^{1+} on the DUT and then estimate the test yield (Y_t) and test quality (DL) of the traditional test method. We take the obtained results using the traditional test method R_{1t}^{1+} as a reference value and compare them with the test results of the next stage retest.

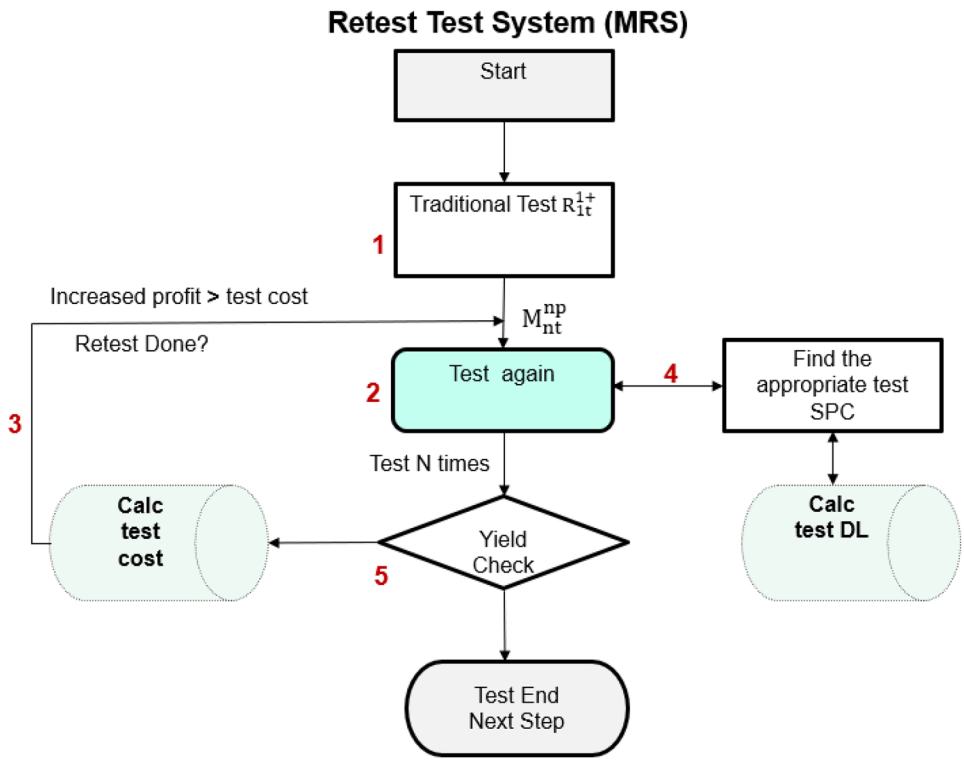

Fig. 11 Execution flowchart of multiple repetition system

Step 2 Next, we test the DUT using the test method for retesting and moving the guardband (i.e., different TS parameters). This step utilizes the moving TGB to reduce killing and missing errors and improve test quality (DL) and test yield (Y_t).

Step 3 We then calculate the profit cost according to the obtained test cost and test yield (Y_t). We will determine the optimal number of retests through sequential analysis of the flowchart. Such a step can help avoid blind retests, save labor, time, and testing costs, and assist in finding the optimal number of retests.

Step 4 The DITM model contains many complex parameters and the calculations of manufacturing yield (Y_m) and test yield (Y_t) are cumbersome. Small changes in electrical parameter values can lead to large changes in yield estimates. Therefore, we use the approximate search method to adjust the TS value of the test and obtain the highest test yield (Y_t) and the best profit by adjusting the best test protection.

Step 5 The proposed MRS is established considering that the improved profit is larger than the testing cost. Therefore, through repeated test methods and cost calculations, we can determine that the (MRS) test system can maximize test yields (Y_t) and maximize company profits.

4.2 Selection and Setting Mechanism of Test Specifications (Approximate Search Method)

The ST sent by the tester during the test process would have edge placement due to the problem of tester inaccuracy. When the ST tester is faster than the time set by the tester, the testing error probability of determining "good" as "fail" would increase; on the contrary, when the ST sent by the tester is slower than the time set by the tester, then the testing error probability of determining "bad" as "pass" would increase. Thus, the accuracy of the tester should also be considered when using testers to measure the DUT. The inaccuracy of the tester leads to killing and missing errors. Therefore, the test engineer must weigh the movement of the test guard to reduce the probability of errors. Moreover, the expansion of TGB will improve the test quality and reduce the test yield, TGB can be used as a tradeoff factor between test quality and yield.

Selecting a test point is important to satisfy the custom's requirement. First, the scope of the test quality is set, and then the movement of the TGB is used to find the appropriate TSs. When using traditional testing method, TGB could be changed and moved while product test yield and quality could be exchanged but could not be obtained concurrently. Defective manufacturing would lead to product defects; therefore, adjusting the TGB appropriately during the test process is necessary to eliminate most of the defective products. When the MRS method is used to test the DUT, the most important issue is to choose the appropriate TS because the TS will affect the test yield and quality. The digital integrated circuit testing model (DITM) contains many complicated parameters; thus, the calculations of manufacturing and test yields are complicated. A slight change in the value of a parameter will lead to a substantial change in the calculation result. Therefore, an approximate search method was used to determine the TS value for the traditional test method (Figs. 12 and 13).

An example is a chip with a DS of (0.86 GHz) 1165 ps and circuit property parameter of $X \sim N(x; \mu_M = 1000$ ps, $\sigma_M = 100$ ps), as well as the above-mentioned estimated formula was used. The manufacturing yield was 95% (Fig. 12 and Table 2). Before selecting the test specifications (TS), the product quality must be considered, and the quality value must be set (DL = 300 ppm). Subsequently, numerical approximation was employed to find the TSs (Fig. 12). The DUT was also tested using ATE (overall timing accuracy (OTA) $= 3 \times \sigma_T = 120$ ps, then $\sigma_T = 40$ ps). The average of ST is equal to TS, $\mu_T = TS$. As a result, the decision of TSs was related to testing yield and quality. In this evaluation, TSs only played the role of mediator. However, corresponding information for the DS parameter could be provided and the information could be expressed clearly and conveniently by using the specification parameter. The standard deviation of ST was obtained from tester accuracy, and overall timing accuracy (OTA) (overall timing accuracy) was the specification parameter of the tester accuracy in this study (assuming OTA $= 3 \times \sigma_T = 120$ ps and so $\sigma_T = 40$ ps). TGB is defined as the distance between the test and DSs if ti is tested (TGB = DS – TS). This distance is three times larger than the tester ST standard deviation (σ_T), namely TGB $= 3 \times \sigma_T = 40$ ps = OTA. Thus, the test specifications are as follows: TS = 1165 – 40 = 1125 ps, namely $ST \sim N(\mu_T, \sigma_T) = N(1125$ ps, 40 ps). Next, four test points were selected ($DS - 3 \times \sigma_T$; $TS = DS - 2 \times \sigma_T$; $TS = DS - 1 \times \sigma_T$; TS = DS), the DUTs were tested separately (Table 2), and the individual test findings of the four test points were estimated ($DS - 3 \times \sigma_T = 1045$ ps, DL = 20 ppm; $TS = DS - 2 \times \sigma_T = 1085$ ps, DL = 356 ppm; $TS = DS - 1 \times \sigma_T = 1125$ ps, DL = 2918 ppm; TS = DS = 1165 ps, DL = 11,756 ppm). Between $TS = DS - 2 \times \sigma_T$ (DL = 356 ppm) and $TS = DS - 3 \times \sigma_T$ (DL = 20 ppm) test specifications, the required test quality could be obtained (DL = 300 ppm). Therefore, the product conformed to the quality conditions, and the best TSs were discovered ($\mu_{T1} = 1083$ ps), the obtained test yield (Y_t) was 77.8%. Next, the TGB was moved, and the test range was narrowed based on the above DL and TSs. Finally, the product conformed to the quality conditions, and the M_{3t}^{3p} best TSs were found ($\mu_{T1} = 1083$ ps, $\mu_{T2} = 1100$ ps, and $\mu_{T3} = 1101$ ps), the obtained test yield (Y_t) was 83.24% while the desired DL (300 ppm) was maintained, and the yield improved by 17.2% (83.24% – 77.8% = 5.44%). When strict TSs are used, the test pass rate is reduced while the test

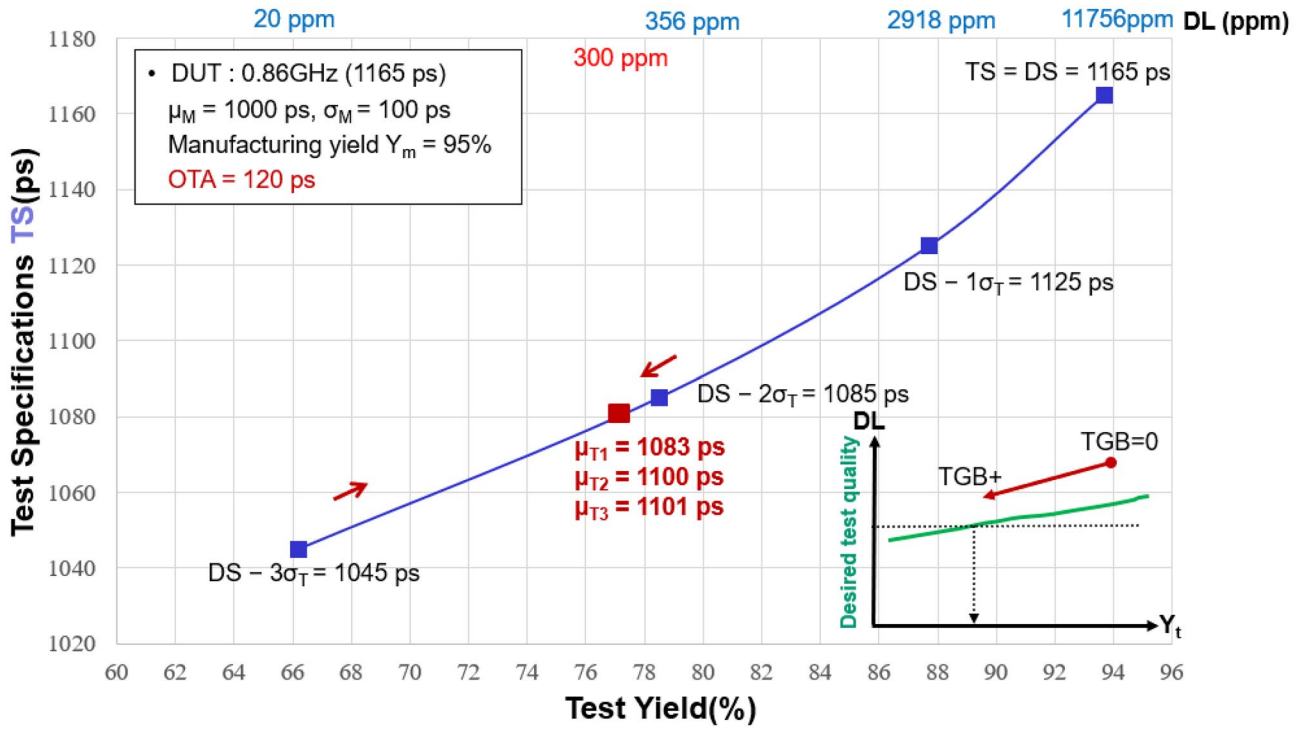

Fig. 12 Flow chart for determining test specifications (TS)

quality is relatively improved. Assuming that the TGB is lowered, that is, a loose TS is applied, the test pass rate will increase and the test quality will be relatively reduced. The above analysis shows that the TSs directly affect the final test yield. Hence, test engineers must be careful in choosing TSs (test guardband).

4.3 Most Cost-effective Retest System (MRS)

The purpose of the test is to identify the chip's characteristics and value, such as its highest frequency, power consumption, and processor level. However, with the continuous advancement of the semiconductor manufacturing process and packaging technology, not only are the functions of the chip increasing, but the chip's speed is also increasing. Therefore, effectively testing the yield, and quality of the wafer becomes extremely complicated. Furthermore, the design, and function of ultra-large-scale integrated circuit chips are increasingly complicated. The greater the number of test items covered, the higher the proportion of test cost to wafer manufacturing cost. However, how to reduce testing costs through effective testing strategies has become a very important issue. As a result, chip suppliers must strive to strike a balance between quality and profit, improve chip yield, and pursue high quality with a high profit as the end goal.

However, the progress of IC tester is slow to almost stagnant in the rapidly advancing semiconductor industry. How to reduce product defect rates and distinguish high-quality chips has also become a critical issue. Therefore, the testing industry invests more funds and manpower, especially in IC tester updates and breakthroughs in test methods. Although, retesting has been widely used in wafer testing, and obtained quite good yield improvement results. However, the more times retested, the higher the cost of labor and IC tester rental. If the total cost of testing exceeds the profit from wafer sales, the retest method has no meaning. Although the speed of testing wafers of the IC tester is very fast, wafer production is in millions. However, the retesting time and the tester rental cost will increase multiple times, causing the company's profits to be compressed. Therefore, before the test, cost control, and profit estimation must be considered. Following that, we seek the best profit and loss balance point for the cost problem and the increased profit of retesting. We use the cost calculation and take to find the optimal number of tests. It does not only consider the cost of testing and the best benefit of retesting, but it also improves the test yield.

The calculation method of 8:20 [28] is used considering the chip pricing in the international market. For example, an IC that is sold for $20 costs $8 to manufacture. In the manufacturing process of semiconductor chips, the cost of chip testing accounts for approximately 5% of the total manufacturing cost [20]. Assuming Company "C" produces 100 million chips per year, if each chip costs $8 to manufacture, then the

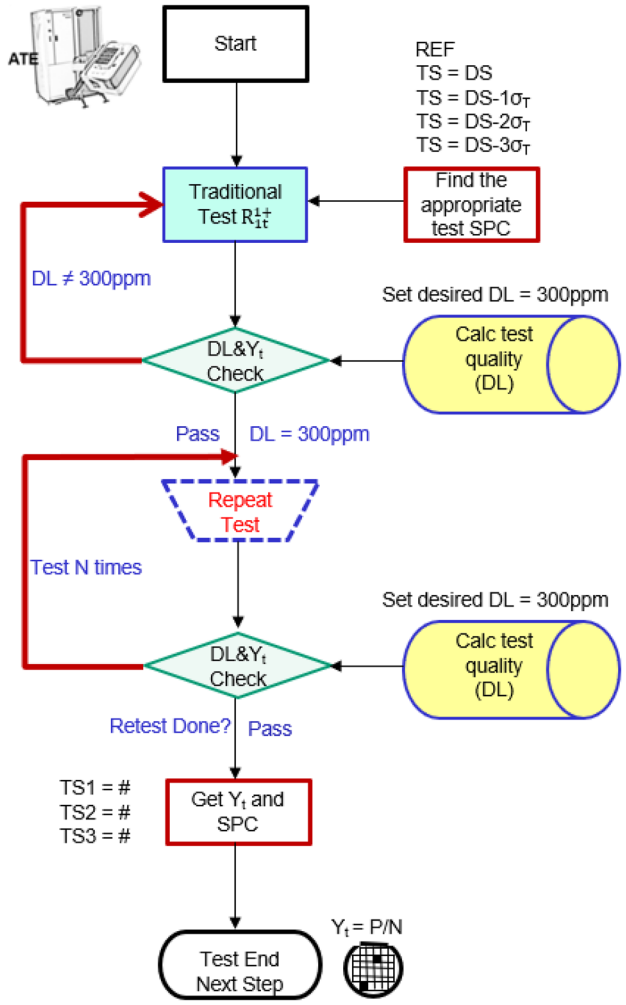

Fig. 13 Optimal test specification (approximate search method) selection and setup mechanisms

total cost of testing required by company "C" is approximately \$40 million (100,000,000 × 8 × 5% = \$40,000,000).

For example, the design house created a chip with DS = 1165 ps (0.858 GHz) with electrical parameters X ~ N (x; μ_M = 1000 ps and σ_M = 100 ps). Using the estimated

Table 2 Test specifications and methods affect test results

Test Method	Test specification TS(ps)			Y_t (%)	DL (ppm)
R_{1t}^{1+}	TS(μ_T)	DS	= 1165	93.7	11756
		DS − σ_T	= 1125	87.7	2918
		DS − 2σ_T	= 1085	78.5	356
		DS − 3σ_T	= 1045	66.2	20
M_{3t}^{3p}	TS(μ_{T1})	1083		83.24	300
	TS(μ_{T2})	1100			
	TS(μ_{T3})	1101			

Eqs. (1)–(2) above, we obtained a manufacturing yield of Y_m = 95% (Fig. 14 and Table 3). The test quality DL was set to 300 ppm and an IC tester with OTA = 120 ps was chosen to test the DUT. We adopt the traditional test method R_{1t}^{1+} and set the TS to 1082 ps, which yields Y_t = 77.76%.

As shown in Fig. 14, under the same test conditions (DL = 300 ppm and OTA = 120 ps), we set the TS value (μ_{T1} = 1124 ps, and μ_{T2} = 1126 ps) and used the repeated test (M_{2t}^{2p}) to test the DUT, based on the above estimates. The test yield is improved from Y_t = 77.76% (R_{1t}^{1+}) to Y_t = 83.47% (M_{2t}^{2p}) after estimation. The company can increase its sales by 5,710,000 chips (100,000,000 × 5.71% = 5.71 million) per year after our iterative estimation. Therefore, the company generates an additional annual revenue of \$114.2 million per year (100,000,000 × 20 × 5.71% = 114.2 million). The company could earn an additional \$34.2 million (114.2 − 40 − 40 = \$34.2 million) after deducting the testing cost of the two retests. Next, we test the DUT using the retest (M_{3t}^{3p}) method. Setting the TS value (μ_{T1} = 1142 ps, μ_{T2} = 1146 ps, and μ_{T3} = 1148 ps) to test the DUT, the retest method can improve the test yield from Y_t = 77.76% (R_{1t}^{1+}) to Y_t = 85.6% (M_{3t}^{3p}). The test yield (Y_t) increased by 7.84% (85.6% − 77.76% = 7.84%), resulting in an additional \$36.8 million in revenue after deducting the cost of three repeat tests (156.8 − 40 − 40 − 40 = \$36.8 million). Next, we test the DUT with repeated test (M_{4t}^{4p}) (TS μ_{T1} = 1156 ps, μ_{T2} = 1155 ps, μ_{T3} = 1158 ps, and μ_{T4} = 1159 ps), and the test yield (Y_t) can be improved from 77.76% (R_{1t}^{1+}) to 86.76%(M_{4t}^{4p}). The total profit is lower than that of the retest M_{3t}^{3p} test method (\$36.8 million > \$20 million) after deducting the cost of testing (180 − 40 − 40 − 40 − 40 = \$20 million). We also compared the test results of different test–retest methods (R_{1t}^{1+}, M_{2t}^{2p}, M_{3t}^{3p}, and M_{4t}^{4p}) under the same quality DL = 300 ppm. The retest plan (M_{3t}^{3p}) can improve the best test results and obtain the best company profit under the condition of 300 ppm quality.

Due to the stagnation of testing capabilities, how the IC tester can distinguish between good and bad objects under test (IC) will become an important issue. An effective Multiple Retest Systems test method is proposed to enhance the test yield, which can effectively improve the test results by utilizing the mobile test guardband (Fig. 5) and prolonging the test time. First, narrow down the test specification (TGB↓, α↓, Y_t↑) and perform the first test of the DUT. The occurrence of killing errors can be reduced by moving the test guardband, thereby improving the test yield. On the other hand, the movement of the test guardband directly affects the test results. Therefore, the number of chips in the pass part increases, while the number of chips in the missing error part also increases (β↑). Therefore, removing the bad chips (missing errors) in the past part becomes the main purpose of the second and third retests. Next, the second, and third tests are carried out on the object to be

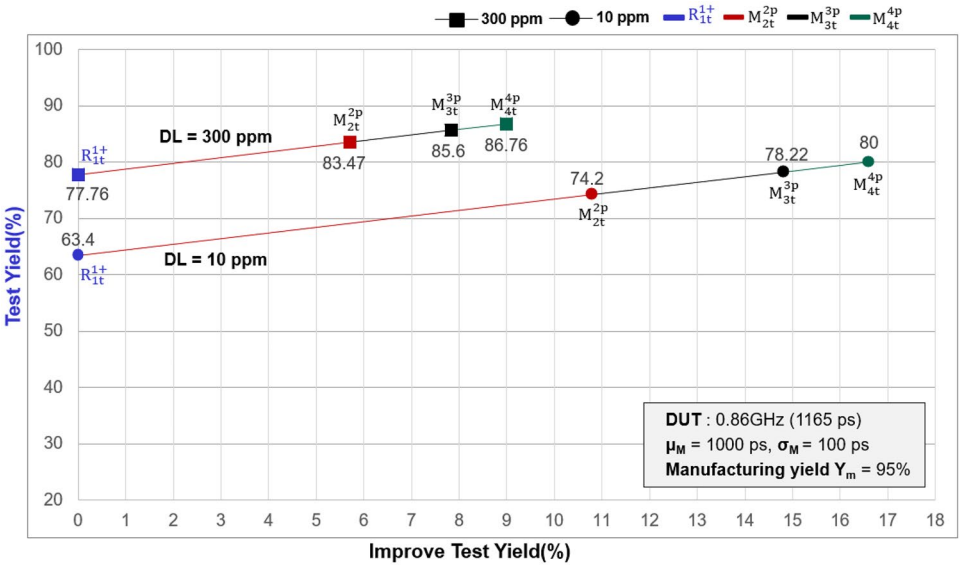

Fig. 14 Number of retests determines the test yield

tested. Similarly, we improve the test yield and test quality (reduce missing errors) by fine-tuning the test guard (test specification). By reducing killing errors (α↓) and missing errors (β↓), the problem of test yield can be solved, and the ability of the IC tester can be improved. However, when entering the fourth retest phase. Although the test yield has increased slightly, the growth rate is too small. The profit generated by a slight increase in yield rate is less than the cost of testing, so overall profit will naturally decline. Therefore, three retests are not only cost effective but also increase the maximum commercial profit. We can conclude from the above inferences that using the Multiple Retest test method and an appropriate test protection area (approximate search method) can solve the problems of missing errors and killing errors, thereby improving the test yield and test quality. The Multiple Retest test method removes abnormal parts from the total parts under the requirement of equal quality DL by moving the test guardband (changing the test specifications). The increase in the number of retests and the appropriate movement of the test guardband improve not only the test capability of the IC tester but also the test yield. In other words, increasing the test time (Test Time) and increasing the number of tests can reduce the probability of killing and missing errors, and improve the test results. From the simulation outcome, the appropriate number of retests is interchangeable with accurate test guard band movement, test yield quality, and test time.

Next, the above simulation test is repeated on the same test equipment with the quality set at DL = 10 ppm for high-quality products. As shown in Fig. 15, under high-quality test conditions (DL = 10 ppm and OTA = 120 ps), we set the TS value ($\mu_{T1} = 1112$ ps, $\mu_{T2} = 1115$ ps, and $\mu_{T3} = 1119$ ps)

Table 3 Estimation of test costs for multiple repetition systems

Chip frequency		GHz	0.86	0.86	0.86	0.86	0.86	0.86	0.86	0.86
Device period		ps	1165	1165	1165	1165	1165	1165	1165	1165
μ_M		ps	1000	1000	1000	1000	1000	1000	1000	1000
σ_M		ps	100	100	100	100	100	100	100	100
Y_m		%	95	95	95	95	95	95	95	95
OTA		ps	120	120	120	120	120	120	120	120
Test method			R_{1t}^{1+}	M_{2t}^{2p}	M_{3t}^{3p}	M_{4t}^{4p}	R_{1t}^{1+}	M_{2t}^{2p}	M_{3t}^{3p}	M_{4t}^{4p}
DL		ppm	300	300	300	300	10	10	10	10
Y_t		%	77.76	83.47	85.60	86.76	63.4	74.2	78.22	80
TS(μ_T)	μ_{T1}	ps	1082	1124	1142	1156	1037	1089	1112	1118
	μ_{T2}			1126	1146	1155		1093	1115	1132
	μ_{T3}				1148	1158			1119	1133
	μ_{T4}					1159				1139
Improve Y_t		%		5.71	7.84	9		10.8	14.82	16.6
Increased maximum profit		million US		34.2	36.8	20		136	176.4	172

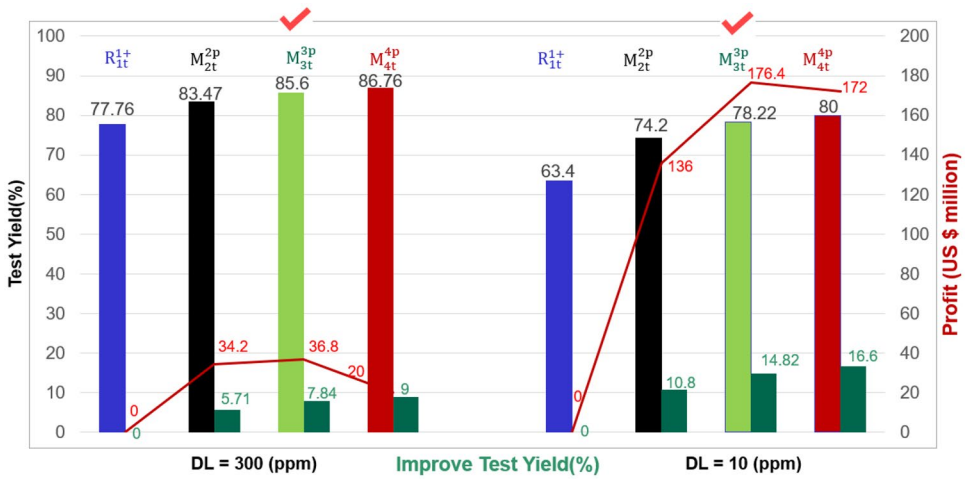

Fig. 15 Calculation of the best cost-effectiveness of the multiple repetition system

and used the repeated test (M_{3t}^{3p}) to test the DUT based on the above estimates. The test yield (Y_t) is improved from $Y_t = 63.4\%$ (R_{1t}^{1+}) to $Y_t = 78.22\%$ (M_{3t}^{3p}) after estimation. The company could earn an additional \$247.4 million (296.4 − 40 − 40 − 40 = \$176.4 million) after the cost of testing for two retests is deducted. We also compared the test results of different test–retest methods ($R_{1t}^{1+}, M_{2t}^{2p}, M_{3t}^{3p}$ and M_{4t}^{4p}) at the same quality DL = 10 ppm. The retest plan (M_{3t}^{3p}) can improve the best test results and obtain the best company profits under the condition of 10 ppm high quality. In addition, at high quality (10 ppm), the improved yield and company profits achieved using the retest method are far larger than those achieved by general test quality (300 ppm). Therefore, we confirm that the retest plan (M_{3t}^{3p}) is the best test plan after the above simulation and test results.

Undoubtedly, as shown in Fig. 16 clearly shows where the break-even point occurs and how the optimal number of tests varies with testing cost. The graph drawn by the above estimates illustrates the optimal number of retests taking both profit and cost into account. Whether it is general test quality (300 ppm) or high-quality product testing (10 ppm), retesting the plan three times can achieve not only the best profit and loss balance but also the best profit. That is to say, the occurrence of killing errors and missing errors is reduced by moving the test guard band and changing the test method. Not only has the test yield rate been improved, but a profit greater than the retest cost will open up business opportunities for the company.

The above results reveal that the repeated test method can improve the test yield (Y_t). However, the test cost increases with the repetition of test times. When the cost of testing is larger than the profit added by testing, the testing method will not help the company's contribution and profit despite its effectiveness. Therefore, we must choose an appropriate number of tests while avoiding blind retesting. On the basis of cost estimation and judgment,

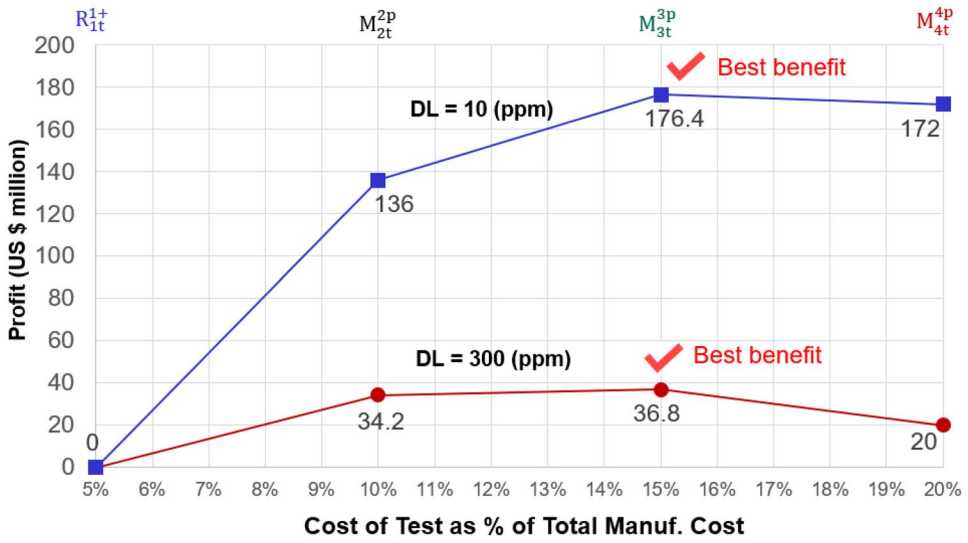

Fig. 16 How the optimal number of test passes would change as a function of test cost

the MRS test strategy can reduce the test cost, save workforce and time, and improve the profit of the best company.

5 Multiplex Test Method (MRS) Applied to the IRDS 2021 Data

The development of IC products is rapidly accelerating, and the semiconductor process has been developed from 90 to 7 nm. Test verification of chips has become an important issue due to the increasing complexity of chip functions. However, using slow-moving testers to distinguish between good and bad chips has become increasingly inaccurate due to the differences in the development of test and manufacturing technologies. Furthermore, the inaccuracy of the ATE tester (IC tester) will lead to additional yield losses. Therefore, utilizing existing semiconductor test equipment (IC tester) (with insufficient test capabilities) to achieve zero-defect products is a growing challenge for suppliers. Therefore, seeking an effective solution and improving the performance of the VLSI tester is currently a crucial topic. We propose an MRS solution to maximize test yield (Y_t) and test quality (DL) to address the product quality requirements of consumers. Furthermore, we can accurately predict the future test yield (Y_t) of the chip through reliable data and estimation methods (DITM). We can propose additional effective testing methods and develop remarkably advanced testing equipment by estimating the trend curve of future yield rates. The test results and company profits can also be aligned with the future goals of the company by proposing additional effective test methods in advance.

Table 4 shows the data of the estimated electrical parameters of IRDS 2021 chips [23]; thus, DITM is utilized to estimate the test yield (Y_t) of future chips. The product DUT electrical characteristic parameters in 2022, wherein the DS is 3.3 GHz (303 ps), the average $\mu_M = 195$ ps, and the standard deviation $\sigma_M = 65$ ps, are also used. We can obtain the production yield of 95% (Y_m) according to the estimated formula above. Next, we use a tester with OTA = 100 ps to test the DUT under the condition that the quality is set by the manufacturer as 300 ppm (Fig. 17 and Table 4). The TS is set to 230 ps, and the test yield (Y_t) of 68.4% can be obtained through the iterative estimation of formula (3).

Using DITM to estimate the future product test yield (IRDS 2021), the slow progress of the tester is found to be relative to the rapid progress of the process and the test yield (Y_t) will become increasingly worse. The testing technology is also far behind the semiconductor process technology. Thus, using an ATE tester whose performance lags behind the process capability for selecting high-reliability electronic products will be a big challenge. IC test manufacturers must perform strict quality control to ensure the reliability of key automotive or biomedical electronic products. Therefore, we change the test method and introduce the MRS. The test yield (Y_t) can be effectively improved without sacrificing the test quality (DL) by relaxing the TS. Referring to the IRDS 2022 product DUT electrical characteristic parameters, we estimated the test yield (Y_t) of chips produced in 2022 using the MRS after changing the test method under the same ATE equipment (OTA = 100 ps). The MRS achieved a test yield (Y_t) of 80.9%, which was approximately 12.5% higher than that of the traditional test method R_{lt}^{1+} (68.4%).

We will use the MRS as shown below to estimate the additional profit provided by the semiconductor company on a cost basis. For example, suppose "C" Semiconductor Company produces 100 million chips per year and uses an 8:20 international chip pricing strategy. In this case, if the manufacturing cost per chip is \$8, then the selling price per chip is \$20. Referring to IRDS estimates, the test cost per chip is 5% of the manufacturing cost; therefore, the total cost of testing for 100 million chips is approximately \$40 million (100,000 ,000 × 8 × 5% = \$40,000,000). Referring to the above example (Estimate the chip production in 2022 (IRDS in 2021)), we will then estimate the additional profit provided by semiconductor companies after deducting test costs. Next, after deducting the cost of retesting three tests, repeating the test can increase the profit by \$130 million (100 million × 20 × 12.5% = \$250 million, 250 − 40 − 40 − 40 = \$130 million). We then estimate the chip production in 2025 (IRDS in 2021). The test yield will increase to $Y_t = 78.3\%$ by using the MRS method to test the DUT. The MRS improves the test yield (Y_t) by approximately 14.7% (78.3% − 63.6% = 14.7%). Next, after deducting the cost of retesting three tests, repeating the test can increase the profit by \$174 million (100 million × 20 × 14.7% = \$294 million, 294 − 40 − 40 − 40 = \$174 million). The estimated results reveal that an MRS can significantly improve the test yield (Y_t). By contrast, the use of a TGB can reduce the incidence of detection and killing errors and achieve high-yield delivery and the overall revenue and profits of the company will be significantly improved.

5.1 Improved Yield and Increased Profits for High-quality Chips

Reducing the defect rate of chips can reduce the malfunction of electronic parts and improve driving safety. Cars require ultrahigh levels of reliability and safety [5–9], thus, the auto industry is setting tough goals for "zero defects" in chips. Defect-free chips not only provide stable and safe operation of automotive electronics but also help companies gain improved reputation and high profits. Therefore, we propose an MRS testing method, which utilizes a slightly backward ATE tester and a retesting mechanism to find truly zero-defect and reliable products, to pursue zero-defect high-quality chips. We then set product quality requirements at high specification DL = 10 ppm and use the

Table 4 Comparison of traditional testing methods and multiple testing (M_{3t}^{3p}) under the 300 and 10 ppm test quality (DL) conditions

Year		Unit	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Chip frequency		GHz	3.00	3.10	3.20	3.30	3.40	3.50	3.60	3.70	3.80	3.90	4.00	4.10	4.20	4.30	4.40
Device period		ps	333	322	313	303	294	286	278	270	263	256	250	244	238	233	227
μ_M		ps	212	208	202	195	190	185	179	174	170	165	161	157	154	150	146
σ_M		ps	72	69	67	65	63	62	60	58	57	55	54	52	51	50	49
Y_m		%	95	95	95	95	95	95	95	95	95	95	95	95	95	95	95
OTA		ps	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
DL		ppm	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300
R_{lt}^{l+}	Y_t	%	73.9	70.8	69.4	68.4	66.3	64.4	63.6	62.3	60.2	59.2	57.5	56.4	53.9	53.3	51.3
	$TS(\mu_T)$	ps	263	250	240	230	220	211	203	195	187	180	173	167	160	155	148
M_{3t}^{3p}	Y_t	%	83.7	81.5	81.7	80.9	79.9	78.5	78.3	77.6	76.4	75.8	74.9	74.4	72.5	72.2	71.3
	$TS(\mu_T)$	ps	315	305	296	284	275	266	258	250	242	235	228	223	216	211	205
			316	302	294	283	274	265	257	249	241	234	227	222	215	210	204
			315	303	294	285	276	267	259	251	243	236	229	224	217	212	206
Improve Y_t		%	9.8	10.7	12.3	12.5	13.6	14.1	14.7	15.3	16.2	16.6	17.4	18	18.6	18.9	20
Increased maximum profit		million US	76	94	126	130	152	162	174	186	204	212	228	240	252	258	280
DL		ppm	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
R_{lt}^{l+}	Y_t	%	56.5	52.1	50.5	48.9	46.1	43.8	42.5	40	37.5	36	34.1	32.5	29.4	28.6	26.6
	$TS(\mu_T)$	ps	225	212	203	193	183	174	166	157	149	142	135	129	121	116	109
M_{3t}^{3p}	Y_t	%	74.8	72	71.1	70.2	68.1	66.7	66.1	64.8	62.6	61.7	60.1	60	57	56.4	55
	$TS(\mu_T)$	ps	291	277	270	260	250	242	234	226	218,217	211	205	199	192	187	181
			292	280	268	259	251	241	233	225	219	210	204	198	191	186	180
			290	281	272	261	250	243	235	227		212	206	200	193	188	182
Improve Y_t		%	18.3	19.9	20.6	21.3	22	22.9	23.6	24.8	25.1	25.7	26	27.5	27.6	27.8	28.4
Increased maximum profit		million US	246	278	292	306	320	338	352	376	382	394	400	430	432	436	448

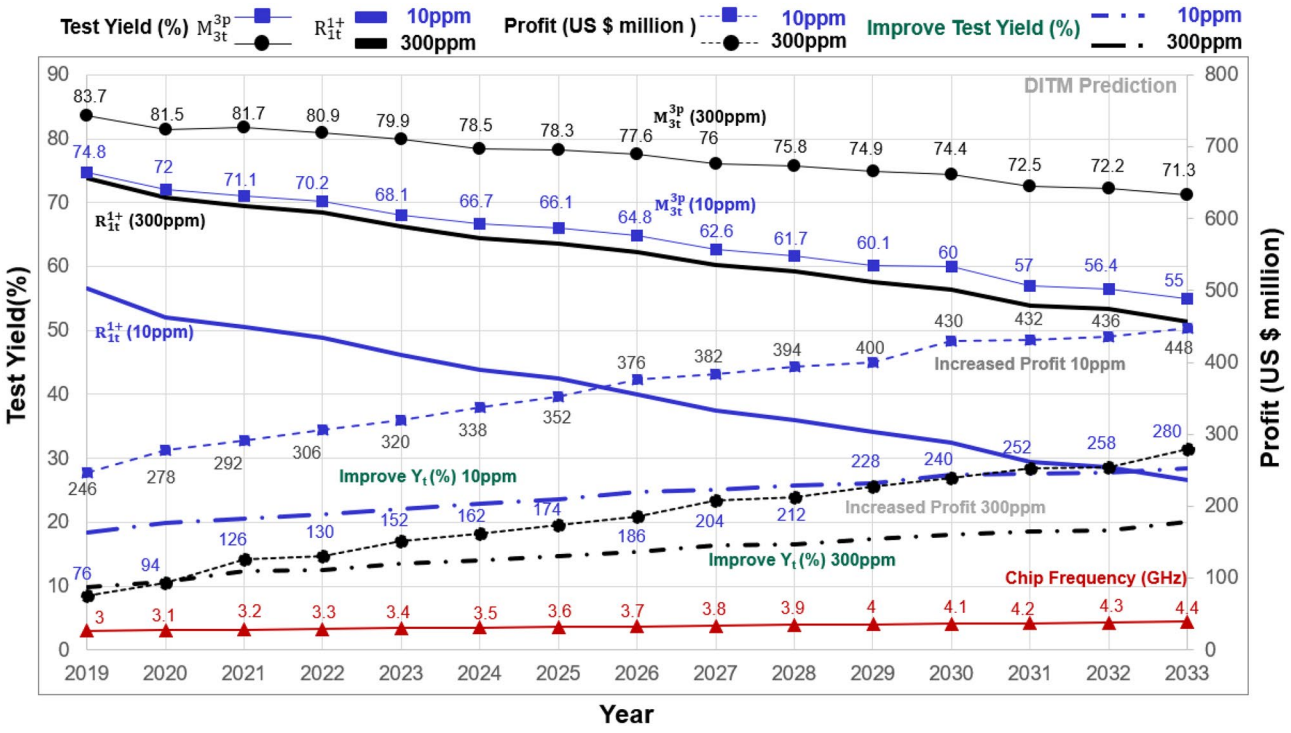

Fig. 17 MRS applied to the IRDS table [23] for guardbanding (300 and 10 ppm)

same ATE test equipment to test the DUT (OTA = 100 ps). Referring to the product DUT electrical characteristics parameters in 2022, the TS is set to 193 ps and the test yield (Y_t) of 48.9% can be obtained through the traditional test method R_{1t}^{1+}. Next, the test yield (Y_t) for chips produced in 2022 was re-estimated using the MRS method. After estimation, the test yield (Y_t) of the MRS reaches 70.2%, which is approximately 21.3% higher than that of the traditional test method R_{1t}^{1+} (48.9%). After deducting the test cost of retesting three times, the retest method can add 306 million US dollars to the profit.

Referring to the DUT electrical characteristic parameters of the product in 2025, the TS is set to 166 ps through the traditional test method R_{1t}^{1+} and a test yield (Y_t) of 42.5% can be obtained (Fig. 17 and Table 4). Testing the DUT using the MRS increases the test yield to $Y_t = 66.1\%$. The MRS also improved test yield (Y_t) by approximately 23.6% (66.1% − 42.5% = 23.6%). After deducting the test cost of retesting three times, the retest method can increase the profit by 352 million US dollars. After estimating and comparing different qualities (10 and 300 ppm), we found that the yield and improved profit obtained using the retest method are far larger than the results obtained from the general test quality (300 ppm) under the condition of 10 ppm high quality. That is to say, under the condition of 10 ppm high quality, the retest plan (MRS) can markedly improve the test results and obtain the best company profits.

The retest method has been widely used in the testing of semiconductor ICs and can effectively improve the test yield (Y_t) and test quality (DL). However, endless blind retesting may reduce the profit of the company and even cause the testing cost to exceed the retesting profit. Therefore, we propose multiple test schemes to meet consumer demand for the expected product output (MRS). The above simulation results reveal that changing the test method changed and relaxing the TS can effectively improve the test yield (Y_t) without sacrificing the test quality (DL). Owing to the repeated inspection of the chip, the number of chips with killing errors is reduced, which not only effectively improves the test yield (Y_t) but also enhances the test quality (DL). In addition, the costing of the retest method verified that the multiple test system (MRS) solution can maximize the test yield (Y_t) by improving the performance of the automated test equipment (ATE) and maximizing company profits. Considering improving the test yield (Y_t), the best balance of increasing profit and reducing test costs is achieved through the MRS mechanism.

5.2 The Innovations and Advantages of Multiple Retest Systems

The development speed of automated test equipment (ATE) (OTA, overall timing accuracy), according to the ITRS report, lags behind the progress speed of semiconductor manufacturing. The testing ability of the automated test

equipment (ATE) is backward and insufficient, just like using a ruler with an inaccurate scale to measure an item with a precision greater than it, this will reduce the accuracy of the measurement. Consequently, we propose multiple test system (MRS), which can not only improve test yield but also test machine capability. The MRS retesting schemes can not only reduce the test cost but also greatly increase the test yield. Because the number of high-quality products that can be sold increase, but also increase the company's profits. The innovations and advantages of Multiple Retest Systems include the following

1. According to the cost feedback calculation, the optimal retest times can be calculated to save manpower and cost.
2. Move the test guardband (TGB) using the approximate search method, which is easy to use and fast in operation.
3. Save more testing costs and increase profits.
4. The maximum benefit between the profit and the test cost can be obtained.
5. Enhance the testing capability of the IC tester.
6. When used in high-quality chip testing (as in automotive aviation and electronics), the yield rate can be increased even further.
7. More company profits can be increased through high-level and high-quality wafer testing.

6 Conclusion

We propose a test model for digital semiconductor chips, which can effectively analyze the impact of different test parameters on quality and yield. We also describe the impact of ATE tester accuracy and TGB on test yield (Y_t) and quality. In addition, the DITM model and the data provided by IRDS 2021 are used to estimate the future test yield (Y_t) trend of semiconductor chips. Therefore, test manufacturers can improve the performance of ATE testers in advance and propose superior test methods by effectively predicting the future Y_t. According to ITRS roadmap estimates, the testing capability has failed to keep up with the capability of the semiconductor process. In the future, if no breakthrough development in the testing methods of chips emerges, then the test yield (Y_t) will become increasingly worse due to the inaccuracy of the ATE tester. Therefore, major manufacturers are also actively seeking effective testing methods to address the problem of insufficient testing capabilities. However, the retest is not only widely used in the testing of actual semiconductor production lines but can also markedly improve the test yield (Y_t) and test quality (DL) through its application to actual production lines [10]. The MRS is proposed considering high-yield product testing methods; this system overturns the traditional theoretical concepts of yield-for-quality and quality-for-yield. The ATE tester with ordinary performance is used to improve the yield after the test effectively, and the method for moving the TGB is repeated to find a truly zero-defect and reliable product, thus achieving high-quality, zero-defect goals for avionics and biomedical electronics with cost estimation and effective retesting. The MRS can reduce the occurrence of killing and missing errors and the cost of testing. By contrast, the improvement in test yield (Y_t) increases the number of chips sold, which not only raises sales profits but also enables the selection of additional high-quality chips.

Acknowledgment The author would like to thank Dr. Jwu E Chen for his invaluable contribution in both defining the model and implementing it mathematically.

Data Availability The data that support the findings of this study are available from the corresponding author, [Yeh CH], upon reasonable request.

Declarations

Conflict of Interests The authors declare that they have no conflict of interest.

References

1. Yeh CH, Chen JE (2019) Repeated testing applications for improving the IC test quality to achieve zero defect product requirements. J Electron Test 35:459–472. https://doi.org/10.1007/s10836-019-05812-0
2. Yeh CH, Chen JE (2020) Test yield and quality analysis models of chips. J Chinese Inst Eng (JCIE) 4
3. Yeh CH, Chen JE (2023) Predict the test yield of future integrated circuits through the deductive estimation method. J Circuits Syst Comput. https://doi.org/10.1142/S021812662350202X
4. Yeh CH, Chen JE (2021) The decision mechanism uses the multiple-tests scheme to improve test yield in IC testing. Proceedings of the International Test Conference in Asia, ITC-Asia 2020. Taipei, Taiwan, pp 23–25
5. Psarommatis F et al (2020) Zero defect manufacturing: state-of-the-art review, shortcomings and future directions in research. Int J Prod Res 58(1):1–17. https://doi.org/10.1080/00207543.2019.160522
6. Automotive Electronics Council (2006) Zero Defects Guideline, AEC - Q004. http://www.aecouncil.com/Documents/AEC_Q004_DRAFT.pdf. Accessed 11 Aug 2022
7. Automotive Electronics Council (2003) Guidelines for part average testing, AEC - Q001-REV-C. http://www.aecouncil.com/Documents/AEC_Q001_Rev_C.pdf. Accessed 11 Aug 2022
8. Nigh P (2004) Achieving quality levels of 100 DPM: it's possible... but roll up your sleeves and be prepared to do some work. 2004 International Conference on Test 1420. https://doi.org/10.1109/TEST.2004.1387428
9. Raina R (2008) Achieving zero-defects for automotive applications. IEEE Int Test Conf 2008:1–10. https://doi.org/10.1109/TEST.2008.5483611
10. Chang P, Huang YK (2021) Intelligent method for retesting a wafer. Teslence Technology Co., Ltd. Retrieved April 3, 2021, from https://www.swtest.org/swtw_library/2019proc/PDF/S02_02_Chang_SWTest_2019.pdf

11. Cheng KC et al (2021) Machine learning-based detection method for wafer test induced defects. IEEE Trans Semiconductor Manuf 34(2):161–167. https://doi.org/10.1109/TSM.2021.3065405
12. Horng SC et al (2003) Reducing the overkills and retests in wafer testing process. Proc IEEEI/SEMI, 286–291. https://doi.org/10.1109/ASMC.2003.1194508
13. Selg H, Jenihhin M, Ellervee P (2020) Wafer-level die re-test success prediction using machine learning. Proceedings of the 2020 IEEE Latin-American Test Symposium (LATS) 1–5
14. Lin W, Shi WL (2013) An on-chip clock controller for testing fault in system on chip. Proceedings of the 2nd International Conference on Computer Science and Electronics Engineering (ICCSEE 2013), China. https://doi.org/10.4028/www.scientific.net/amm.347-350.724
15. Li H, Zheng D (2021) Study on retest reduction by minimizing probe card contact resistance at wafer test. Proceedings of the Semiconductor Technology International Conference (CSTIC), China, pp 1–4
16. Jena SK, Biswas S, Deka JK (2021) Retesting defective circuits to allow acceptable faults for yield enhancement. J Electron Test 37:633–652. https://doi.org/10.1007/s10836-021-05980-y
17. Selg H, Jenihhin M, Ellervee P (2020) Wafer-level die re-test success prediction using machine learning. IEEE Latin-American Test Symposium (LATS) 2020:1–5. https://doi.org/10.1109/LATS49555.2020.9093672
18. Yeh CH, Chen JE (2022) Recycling test methods to improve test capacity and increase chip shipments. IEEE Design & Test. https://doi.org/10.1109/MDAT.2022.3221703
19. Yeh CH, Chen JE (2021) Unbalanced-tests to the improvement of yield and quality. Electronics 10(23):3032. https://doi.org/10.3390/electronics10233032
20. International Technology Roadmap for Semiconductors (2001) Test and test equipment. 5–6. https://www.dropbox.com/sh/vxigcu48nfe4t81/AACuMvZEh1peQ6G8miYFCSEJa?dl=0&preview=Test.pdf. Accessed 23 Sept 2021
21. International Technology Roadmap for Semiconductors 2.0 (2015) System integration. http://www.itrs2.net/itrs-reports.html. Accessed 11 Aug 2022
22. International Technology Roadmap for Semiconductors (1999) Test and test equipment. 5–6. http://cva.stanford.edu/classes/cs99s/papers/roadmap1999.pdf. Accessed 23 Sept 2021
23. International Roadmap for Devices and Systems (IRDS™) 2021 Edition (2021) System integration. https://irds.ieee.org/editions/2021. Accessed 11 Aug 2022
24. Dalal W, Miao S (1999) The value of tester accuracy. Proceeding IEEE International Test Conference (ITC) pp 518–523
25. West BG (1999) Accuracy requirements in at-speed functional test. Proceeding IEEE International Test Conference (ITC) pp 780–787
26. Chen JE, Yeh CH (2004) Test Guardbanding for Yield and Quality Estimation. Proceeding International Test Synthesis Workshop pp 114–115, USA
27. Williams RH, Hawkins CF (1993) The economics of Guardband placement. Proceeding IEEE International Test Conference (ITC) pp 218–225
28. Jacquelyn (2018) Break through process: Why is 7nm the physical limit? What is the 1 nm manufacturing process in America? https://www.elinfor.com/knowledge/break-through-processwhy-is-7nm-the-physical-limitwhat-is-the-1-nm-manufacturing-process-in-america-p-10872. Accessed 11 Aug 2022

Chung-Huang Yeh received the Ph.D. degree in electronics engineering at National Central University, Taoyuan, Taiwan, R.O.C., in 2020. His research interests are in reliability and test quality of circuits.

Jwu E Chen received his BS, MS, and Ph.D. degrees in Electronic Engineering from National Chiao-Tung University, Taiwan, in 1984, 1986 and 1990, respectively. Presently, he is an associate professor of Electrical Engineering at National Central University, Taiwan. His research interests are in reliability, fault tolerant and test quality of circuits.