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Light Emission Tracking and Measurements for Analog Circuits Fault Diagnosis in Automotive Applications

Tommaso Melis[1] · **Emmanuel Simeu**[2] · **Etienne Auvray**[3] · **Luc Saury**[1]

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Abstract
The automobile industry's rapid growth enables developments in all branches of the sector. This also includes electronics, where the latest technological nodes are used today. New challenges to providing safety and reliability for such circuits are thus to be faced. One of these is the diagnostics of analog and mixed-signal circuits. Performing failure analysis has become very difficult indeed, due to the lack of auto-diagnosis methods. This paper describes a solution to improve the diagnosis of such circuits. We can insert elementary devices that return circuit states via light emission by utilizing the basic principles of light emission from silicon electronic components. These elementary devices are used to check every fundamental signal of the circuit, with significant benefits for diagnostics and failure analysis. All actions leading from concept to real silicon are explained. The reported results for a real silicon circuit and a failure analysis case demonstrate the effectiveness of this method.

Keywords Photon light emission · Analog and mixed-signal · Diagnosis · Failure analysis · Fault isolation

1 Introduction

The market for electronics in automobiles is very dynamic and constantly growing. This is evident from the latest estimates reported in [1, 2, 4], where a value of $53.6 billion is expected in 2025. Considering a single vehicle, the electronic components in a traditional car make up about 40% of the cost, reaching about 75% for electric cars. A modern car has about 100 ECU [30], which gives an idea of the magnitude of this phenomenon. Electronic applications cover many areas. The main innovations are aimed at the Internet of Things (IoT), infotainment, and especially advanced driving assistance systems (ADAS). Besides these, there are also constant improvements to devices for classic applications (e.g., circuits for car doors). Thus, all this contributes to the uniform evolution of this field. This pushes the automotive market to use the latest technology nodes by introducing new challenges in all its sub-domains. These devices, in fact, have two main requirements in common since they are used in such an important market: reliability and safety. Both are critical aspects considered during the design phase.

Reliability ensures that the circuit works properly according to its specifications for a stated period of time (typically the car's life) [10]. The required tests to ensure reliability targets are defined in the AEC-Q100 standard [3]. In particular, it focuses on tests such as environmental, accelerated life, package assembly integrity, and die level. When all the tests are performed and passed correctly, the product is ready for the market. The goal will be to have a population of devices with a failure rate of less than 1 ppm/year[9].

The safety aspect is more inherent to the circuit design and its functionalities. Two standards are present to define the safety of an electronic circuit. One is the IEC 61,508 [13], which is the functional safety standard for the general electronics market. The second is ISO 26262 [16], which is

Responsible Editor: L. M. Bolzani Pöhls

✉ Tommaso Melis
tommaso.melis1@st.com

Emmanuel Simeu
emmanuel.simeu@univ-grenoble-alpes.fr

Etienne Auvray
etienne.auvray@fastnet-technologies.com

Luc Saury
luc.saury@st.com

[1] STMicroelectronics Grenoble, Grenoble, France

[2] CNRS, Grenoble Institute of Engineering Univ. Grenoble Alpes, Univ. Grenoble Alpes, TIMA , Grenoble, France

[3] Fastnet Technologies, Grenoble, France

the standard for functional safety in automobile circuits. This is actually the guideline in automotive and defines the criteria and metrics for the functional safety of a circuit. These metrics are determined by the application's safety risk. The definition of the hazard depends on the Automotive Safety Integrity Level (ASIL) grades. These four levels (from ASIL-A to ASIL-D) are based on the risk of the application considered from the system level down to the single device. The devices for safety applications must be defect-tolerant with high test coverage. This means that even if a failure occurs during the application, the device must remain safe to avoid endangering human lives.

Among reliability and safety requirements, we have a third crucial area, which is failure analysis (FA). It supports the design of the circuit by determining if there are any weaknesses before the device is available on the market. This is accomplished through FA on devices subjected to reliability tests. It helps achieve reliability goals. When a product already on the market fails, FA assesses the risk for a population of devices. This ensures the safety of all devices throughout their lifecycle The actual FA challenge in automotive circuits is analog and mixed-signal. In fact, the same automatic diagnosis tools and solutions are not available as for digital circuits [7, 8]. Some fault diagnosis approaches deal with machine learning algorithm applications [15, 23, 31, 34]. Yet, none of these is a standard approach to solving large-scale failure analyses on analog circuits. The diagnosis approaches implemented on analog devices are thus limited. BIST solutions are possible [6, 14, 24, 32], but difficult to apply to all the devices. In addition, area consumption, transparency in applications, and especially the need for additional output pins on the integrated circuit (IC) are the main constraints. Moreover, these must be adapted to the different circuit types. Another solution we proposed [17] is to use the techniques of the FA and the automatic analog fault simulators (AFS) [5, 27, 35] to have an automated diagnosis. Many failure analyses of analog automotive circuits were resolved using this method [19]. Most of them were solved using emission microscopy (EMMI). Indeed, in FA, we use EMMI measurements extensively to locate a failure within the circuit. In general, with EMMI, the analyst often observes the consequences of a failure or the circuit state. In particular, it is not actively exploited by predicting it during the design of ICs. Yet, time-resolved measurements of light emission are possible and simulated for transistors [26]. In addition, EMMI simulation at the product level is possible and automated for analog and mixed-signal circuits [19]. This also means that EMMI images are characterized for such devices. In this sense, it is demonstrated that the characterization of the emission spot can be exploited as input for an automatic flow of diagnosis with AFS [19].

This paper proposes two new approaches to exploiting the EMMI for improving the fault detection and testability of analog circuits. The first method consists of using the light emitted by the silicon integrated circuit as input for the fault diagnosis done with the AFS. In this way, the consequences of the failures observed with EMMI can be used to drive the fault diagnosis. The second approach deals with detecting faults with elementary light-emitting devices intentionally placed within the ICs. Such devices, called "light trackers", are used to check the state of the circuit through their light emission. These elements are light probes that represent an indirect measurement of the signals monitored by them and return the global state of the circuit through EMMI measurements. This method can potentially enable fast FA by acquiring a few images. Part of the outcomes of these solutions were previously presented in [18]. The latter work focused more on the first solution, giving some results on real failure analyses. In this paper, we will describe both solutions for using the light emission from integrated circuits for diagnosis, with more emphasis on the second solution. Light trackers will be explained in detail, with a step-by-step implementation procedure and more complete results.

The work is organized as follows. The second section explains a general failure analysis flow. The third section describes how to actively exploit the light emission for fault diagnosis with AFS. The fourth part presents the second main idea of this work, the light trackers. It explains the general concepts, the implementation, and its applications. Section 5 reports the results of the two approaches applied to real-world diagnosis cases and a silicon device. In Section 6, we draw the conclusions of this paper.

2 Failure Analysis Process

A sample that arrives in the FA laboratory is generally the result of reliability tests, either a design verification or a customer return (failure in the field). There is a failure description for each of the cases mentioned above. The first step in the laboratory is to verify the failure descriptions and confirm the presence of an electrical failure signature (see Fig. 1). This latter is called the failure mode of the device under test (DUT). To do that, the circuit is first analyzed with an automatic test equipment (ATE). This provides the failing output of the device and defines the failure mode. The failure is then reproduced on the electric bench. This allows a suitable setup to be used inside the equipment for the analysis (such as microscopes). Analysis tools indeed require setups that can be mounted in a small space. A set of non-destructive verification inspections is then performed on the sample. These techniques are used to check if a defect is visible without applying any electric input or sample preparation to the device. If the failure cannot be directly located using these techniques, the analysis moves on to fault isolation. This is a key part of the analysis, where the area affected by the failure is precisely defined and

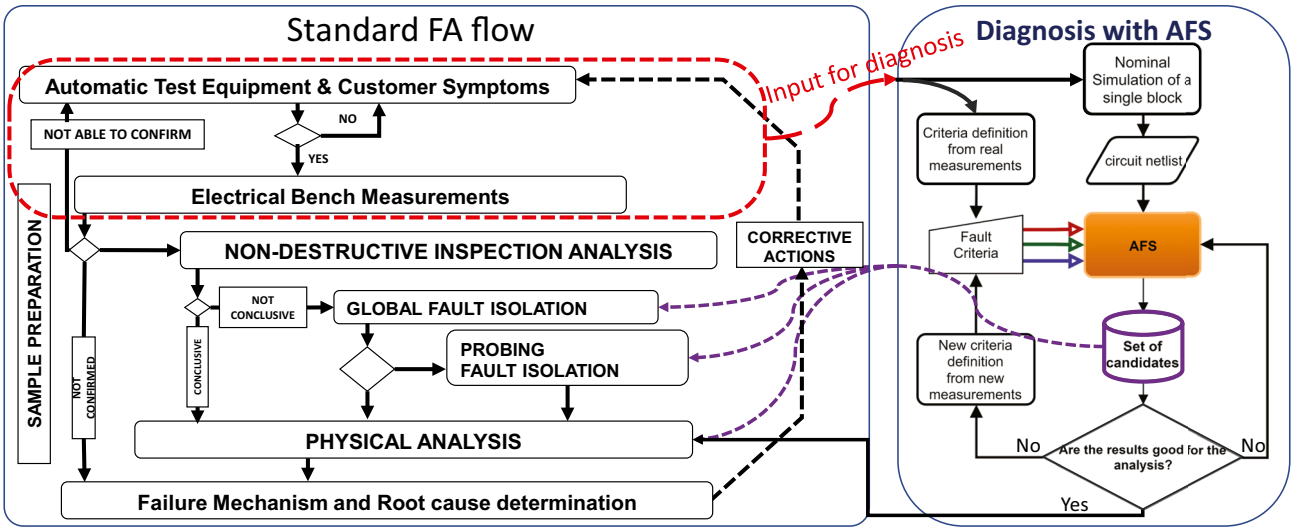

Fig. 1 Failure Analysis workflow inside a laboratory. On the left-hand side the standard techniques. On the right-hand side the possible diagnosis method using the AFS. This latter takes as input the measures of the standard techniques (highlighted in red) and returns candidates (violet) to be used inside in many steps of the standard flow

located. In general, a sample preparation is required to achieve this step. This is done by keeping the sample functional and allowing for inspection with some microscopy techniques. There are two main sample preparations: front-side or back-side. The former discovers the upper metal layers. It is generally used to perform mechanical probing or to check the metal layers with the optical microscope. The latter discovers the silicon surface. When this is possible, it is particularly suitable for Thermal Laser Stimulation techniques [11, 22, 25] or photon emission microscopy (EMMI) [12]. These techniques use detectors and lasers in the near-IR range. In this range, the silicon is transparent, allowing the analyst to see the layout and devices without being masked by the metal surfaces. The fault isolation process can be split into two categories: global fault isolation and probing fault isolation. The goal of global fault isolation is to find a location by using techniques like EMMI [12] or thermal laser stimulation microscopy [11, 22, 25]. The majority of analyses are solved using these techniques. Both techniques are based on comparing images acquired on a good sample with those of the DUT. The goal is to detect spots or light emissions that may characterize a failure. A normal analog circuit typically has a lot of emission activity (see Figs. 2 and 3), resulting in a difficult interpretation. As a consequence, finding differences is complicated too. For this reason a solution is the EMMI simulation for analog and digital circuits [20]. This is an important advantage for the analysis because it enables defect hypothesis validation with simulation. Analogously, the simulation for the thermal laser stimulation technique is starting to be available [19]. This allows the same benefits as those for the EMMI. If the global fault isolation is not successful, the probing fault isolation continues the analysis. The goal is to backtrack the failure by measuring the internal signals of the DUT and comparing those with the nominal circuit simulation. Several techniques are available to perform these measurements [21, 29]. After this step, the fault is usually located. In this way, a single area around the

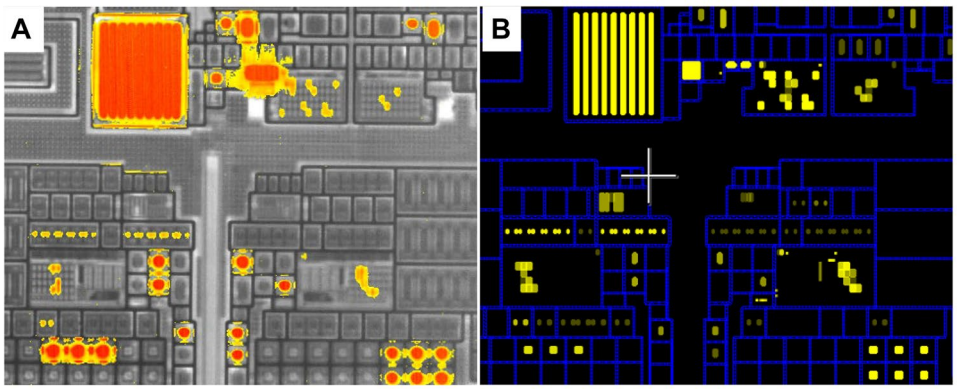

Fig. 2 **A** Example of EMMI image of a golden sample of analog circuit block; **B** EMMI simulation of the same block in nominal conditions

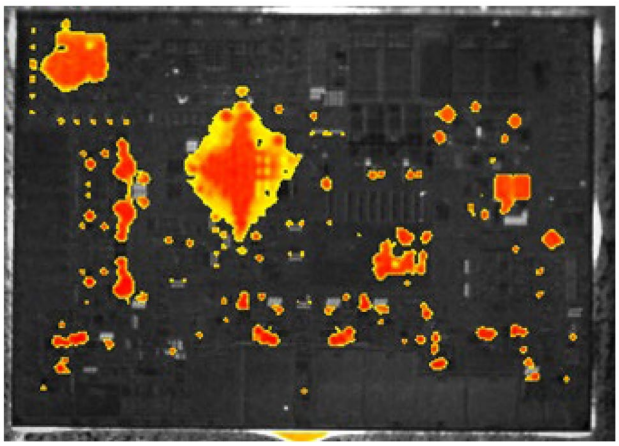

Fig. 3 Example of light emitted from the backside silicon surface of an analog circuit at 1X magnification

defect is individuated, and the physical analysis (PA) is then performed. Destructive preparation techniques are used to do that. As a result, it reveals the physical defect by means of the optical microscope or the scanning electron microscope. If the defect is found, the root cause is identified, and a corrective action is deployed. This is the standard FA flow (see Fig. 1).

Alongside the classical FA process (see Fig. 1), automatic analog fault simulators (AFS) can be used. This procedure is based on the identification of a macro functionality of the circuit affected by the failure. The goal is to find the subcircuit that is failing in order to build a simulation of it. The electrical measurements from the ATE or bench can give the information necessary to retrieve this portion of the circuit. From these steps, we generally obtain one or more outputs of the circuit affected by the failure and identify the block most likely involved in the failure. In this way, we build a simulation around that block, and with AFS, we inject and simulate all possible faults. Among all these faults, we look for the one that comes closest to the characteristics of the faulty outputs. This is an iterative approach in which the AFS provides a set of candidates based on the measurements performed during the FA (in the steps presented in the previous flow). Thus, AFS and FA techniques are used iteratively to obtain a set of candidates for analysis and to reduce that set at the same time. This process ends when the set of candidates is small enough to start the PA or when there is a match between one candidate and the FA measures. The details of this procedure are described in [17, 19].

3 Light Emission Input for Automated Diagnosis

The silicon elementary devices emit light in the near-IR range. This mechanism is the basic principle used by the EMMI to locate the defect inside the device. The process, as explained before, is based on comparing the images of a DUT with a golden unit to locate the differences and isolate the fault inside the device. The differences are often a consequence of the failure and do not help to locate it visually. The method described here focuses on the examination of such differences as the starting point for AFS's diagnosis. The emission of elementary electronic devices is in fact well known and has been successfully simulated [20] (see Fig. 2). However, in this work, we will not inspect the intensity of the light emitted by the structures, the respective simulation, or its accuracy. Such details are explained in [20] and are not required here to define which voltage ranges can have a specific emission spot. In other words, this method is used to define the conditions for the presence of the light emitted (or not) in an elementary device that is individuated by the comparison of the DUT with a golden unit. We will focus on MOSFETs since their emission activity is very high for analog devices. Yet this method is also used for other elementary devices that emit light (diodes and bipolar transistors).

The emission from MOSFETs occurs when they are in two particular conditions. The first is the most important and frequent and is generated by MOSFETs in saturation conditions. It is recognizable because the emitted light is located on the drain side. The second occurs when they are used in diode configuration (often used for protection circuits, e.g., ESD). This mode is identified by the emission spread over the entire surface of the elementary device. For the method described here, the emission from MOSFETS is possible if they are saturated. The following relation valid defines this condition for nMOS without scaling effects:

$$V_{DS} > V_{GS} - V_{th} \tag{1}$$

where Vds is the drain to source voltage, Vgs is the gate to source voltage and Vth is the threshold voltage. Analogously, the diode emission from nMOS is defined by:

$$V_{GS} < V_{th} \;\&\; V_{DS} < 0 \tag{2}$$

The goal of this approach is to understand if a variation of a nominal simulation value can satisfy relations (1) or (2). All these parameters can be derived from simulation results. In this paper, the value of Vth is instead extrapolated from the design rules of the technology employed.

The other elementary devices that emit light are diodes and BJTs. Diodes emit when they are both in forward and reverse bias. In reverse bias, the emission is present when they are in the avalanche region (common for Zener diodes). For the forward bias, the emission occurs when the applied voltage is greater than the knee voltage. An analogous argument can be made for BJTs, which are composed of two junctions. In this case, the emission is qualified by the collector current [33].

The algorithm is run based on these distinctions. First, EMMI images are acquired in the fault-affected area of the DUT. Then they are compared with the images of the same area on a good device. Alternatively, they are compared with the nominal emission simulation for even faster results. This comparison leads to differences between the images, characterized by the presence or absence of light spots from the elementary devices in the DUT. These differences are then located within the layout so that the elementary devices related to them can be identified. A list of differences is then created and sorted visually (e.g., the strongest spots are analyzed first). Next, a device is selected from this list, and its nominal simulation is examined. In this way, the operating region of the device is defined under nominal conditions. Yet, the nominal conditions define the opposite state of the pointed-out difference. In other words, based on the nominal conditions, the emission of the good device is studied. From these conditions, the emission of the DUT is deduced. To understand the latter conditions, a change in a signal applied to the elementary device is assumed. To do it, the possible operating regions that cause the emission are considered (e.g., infer how to make a transistor that nominally operates in the linear region become saturated). If these assumptions are univocal (e.g., only one signal can change the operating region of the device), then they are defined as a voltage range. This range then becomes a criterion for automatic diagnosis. If these variations are not unique (e.g., many conditions can cause the device to emit), then the difference cannot be considered a criterion, and a new device is selected. The process is repeated until sufficient criteria are obtained (see Fig. 4). Otherwise, the process ends if all differences are analyzed. The list of criteria derived from this process is used for the AFS diagnosis (see Fig. 1, right side). In this way, the subcircuit affected by the failure is deduced from the ATE and bench measurement results. The nominal simulation for this subcircuit is prepared to be used by AFS to inject the faults. The additional inputs are the fault criteria. These are the fault signatures that characterize the failed sample, defined as electrical ranges. For this reason, the list deduced by the procedure defined in this section is important because it enlarges the set of data that can be used for fault diagnosis. In fact, the fault criteria also include the electrical measurements carried out during the FA. The fault simulation is performed in this manner and returns a list of candidates. This list can be reduced iteratively by successively applying the fault criteria determined during the FA. The new criteria apply to the previous iterations' sets of candidates. In this way, the set of candidates is constantly reduced. The fault diagnosis ends when a set small enough to conclude the analysis is obtained [17, 19].

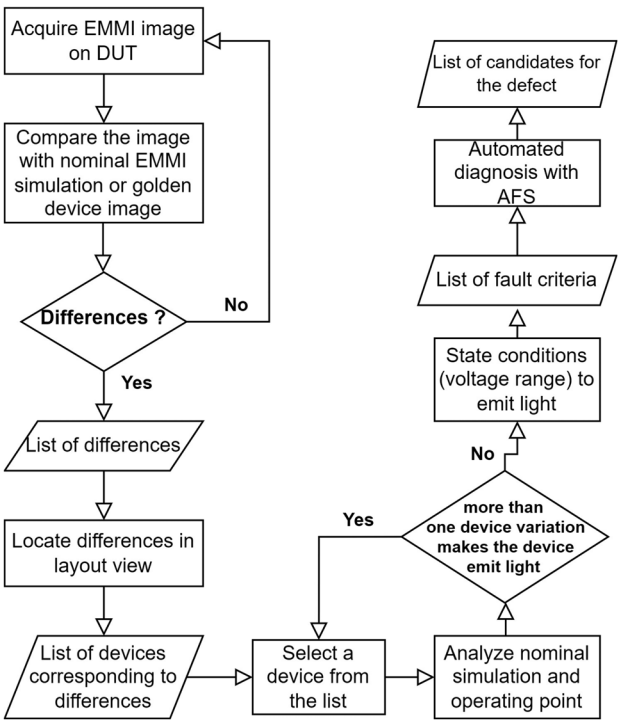

Fig. 4 Algorithm to deduce a voltage range and fault criteria starting from an EMMI image

4 Light Tracker

This section begins with a general description of this new technique. Then the fundamental steps leading to the practical implementation of the circuit are explained. Finally, the exploitability of the method inside the failure analysis flow is given.

4.1 General Idea

This new approach to fault detection exploits the natural tendency of silicon devices to emit light in the near-IR range. An analog circuit can be divided into various macro-functionalities. These compose the fundamental analog blocks of the design and are characterized by one or more principal outputs. The main idea is to assign a light-emitting device to each of these outputs. In this way, the state of the signal is reported by the component connected to it (pass or fail). In other words, by analyzing the presence (or absence) of light emitted by intentionally placed devices, we may understand whether an internal signal has been properly generated or not.

This system is called Light Tracker (LT). It is composed of two main circuits: the control and the emitting unit (see Fig. 5A). The role of the control unit is to prepare the signal that will be applied to the emitting unit. It may contain an input to disable the light tracker in the case of a specific test or to reduce

the current consumption of the whole circuit. Thus, within this block, there may be a part of combinational logic that mixes the input signal with a control signal (see Fig. 5B, at bottom). This also depends on the nature of the signal to be controlled. In fact, this is only possible when the signal has a range of voltages that allows for combinational logic. Otherwise, when the input voltages are too low or too high for a digital circuit, it is possible to use transistors in a switch configuration (see Fig. 5B, at top). In any case, the output of this module must provide enough voltage to make the second block emit light.

The emission unit contains the device indicating the state of the monitored signal. In our case, we use a diode for simplicity (see Fig. 5C). Yet, one can use any component that emits light in the near-IR range (MOSFET, BJT, or diodes) [12], allowing for more advanced uses and integrations. A resistor is connected in series with the diode and controls how much current flows in the diode and thus how much it emits.. This aspect will be discussed in detail in the next section.

The diode's polarization depends on the type used. A normal *pn* diode emits in forward bias mode, while Zener diodes can emit both in forward and reverse bias. These latter are most often used in reverse bias, presenting a strong emission. However, since they can also emit when forward biased, there may be ambiguity about the LT status. To resolve this ambiguity in this work, we have used only normal *pn* diodes.

The LT emission represents the status of the signal. The most logical implementation would be for the LT to emit when there is a fault in the monitored signal. However, such devices are employed in circuits used in safety applications. This implies that when a failure occurs, the circuit must remain in a safe state. It is often also a state in which some internal voltages are automatically forced to zero. Yet, implementing the LT in such a way that it emits when a fault is present could have dangerous consequences. In fact, we could have a situation in which a catastrophic fault is present and the circuit tends to switch off all supplies. In this case, we would be forced to keep an active current path to let the LTs emit, creating a potentially much more catastrophic situation. For this reason, except in some situations, a signal is considered good if its LT emits light.

The overall result should be a set of devices that emit light and show the status of the monitored signals. This allows the analyst to understand where a fault originates. However, the non-functionality of a block can propagate within a circuit since we are dealing with analog applications. We could therefore observe that after a fault in a certain point of the circuit, other internal voltages do not have the desired values. For this reason, the information given by the single LT cannot furnish the origin of the defect. In order to fully understand its cause, we must read the states of all the LTs and create a kind of truth table. Based on such a table result, a general conclusion can be drawn. This will state at the same time that both the block and the internal node were first affected by the failure.

4.2 Implementation

The starting point of the implementation focuses on the emitting unit. The choice of light-emitting devices and their dimensions are the first requirements. As stated before, we chose normal *pn* diodes that emit in forward bias mode for this design.

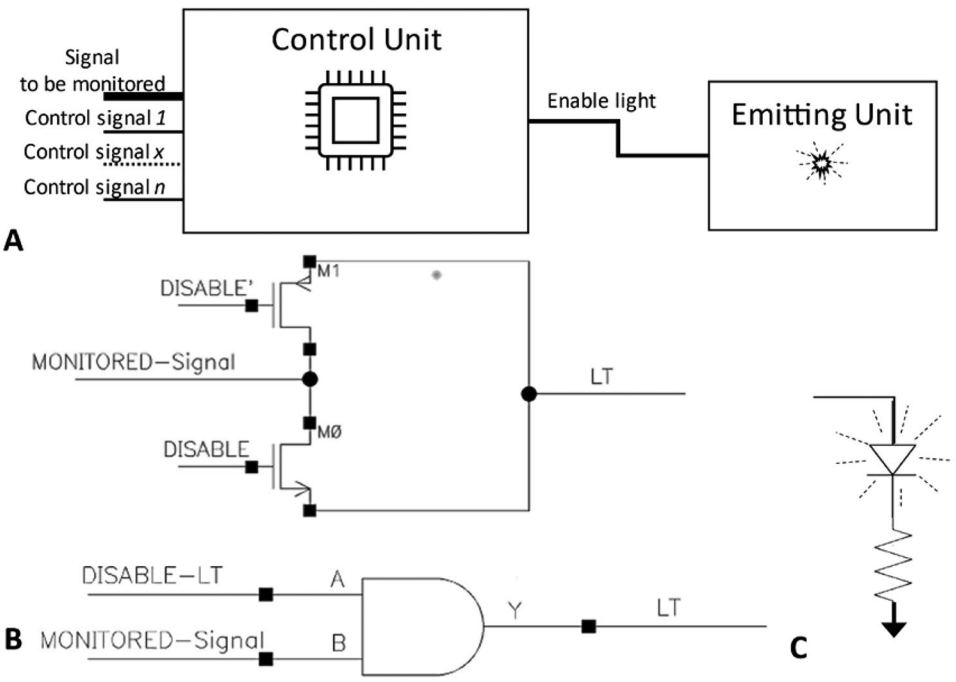

Fig. 5 **A** representation of the Light Tracker structure; **B** two examples of control units; **C** example of emitting unit with a general diode

Regarding the dimensioning of the devices, we performed a characterization. The goal was to find the minimum amount of emitted light detectable by a standard emission microscope. This is also motivated by the need to find the lowest possible current consumption while still causing enough light to be emitted by the devices. To accomplish this, we used a wafer with mechanical probing access to single devices. We chose a *pn* diode with an area of 16 pm2 and applied the voltage for the forward biasing.

We used the Meridian IV emission microscope to measure the light emitted by the diode. It is equipped with an InGaAs camera cooled with a Peltier system to capture light in the near-IR range. For the measurement, we used the 20× magnification lens that is most commonly used during our fault isolations with EMMI.

We supplied the diode with different voltages in forward bias and measured the current consumption and light emitted. From Fig. 6, the diode shows a faint light with a current of 250nA. It presents a greater emission with a current of 10 uA. Although the current of 250 nA is associated with the smallest detectable light, we need to consider the potential light emitted in the surrounding real circuit. In fact, the analog blocks are usually characterized by strong emission activity (see Fig. 3). This aspect can mask the emission of the LT, losing the benefits of this method. For this reason, the prudent decision is to consider the current in the middle of this characterization (1 uA). This offers discrete emissions with relatively low consumption.

The current flowing inside the diode is fixed. It is now possible to dimension the resistance in series. The resistor keeps the current constant and is the only parameter that differs in each LT. In fact, the diode area, current, and threshold voltage are fixed, while the applied voltage to the LT varies. This is the signal to be monitored, and the resistance will be proportional to it.

The remaining parts of the design are the control unit and the signal to be checked within the IC. The control unit is dependent on the signal to track, as previously said. However, this will not be discussed in this paper because it is specific to the application and not fundamental to the understanding. As for the internal voltages to be monitored, these are dependent on the circuit type and how it is designed. If possible, it would be preferable to design the circuit with the startup sequence determined by a state machine. In this way it would be possible to associate a LT to each state of the machine. The resulting combination of light emitted will indicate the state of the circuit or, in the event of failure, the state in which it is locked.

Yet a state machine is not always implementable in an analog circuit. In this case, we need to analyze in detail the startup sequence and identify the important signals within the design. This is a difficult task because in analog circuits, the signals are often not completely sequential but are dependent on each other. This is also the reason why this method is essential and why LT information is to be read as a whole and not individually. Interesting signals to check are, for example, reference voltages created inside the circuit (bandgap, LDO, charge pump) or oscillators. Naturally, it is convenient to associate a LT with these voltages if it is not possible to measure them directly through a pin.

4.3 Use of Light Tracker in Failure Analysis

The availability of LT within a circuit can improve any eventual failure analysis's accuracy and speed. In particular, there are two main benefits to this approach. The former is the failing block location, the main reason why these emitting devices are used. A table indicating all the LT emission combinations is used to achieve this goal. This has to be prepared during the design phase, and it is necessary to have a rapid analysis.

The latter benefit is the identification of a faulty node, and it is a natural consequence of the LT use. This information can be exploited as a fault criterion for the analog fault simulator if it is available. During an FA, we can have many symptoms or failing signatures that are measured through the external pin of the device. These are collected as failing criteria to be used to perform an automatic diagnosis by means of the AFS. As explained in [19], we can also use some internal light emission as a failing criterion.

This solution is compact in terms of silicon area consumption. In fact, it consists of a control circuit (composed of a few transistors) and an emission unit composed of a diode and a resistor. The total area can vary from the type and number of LTs inserted in the circuit (consequently from the monitored signals). There is no lack of performance with the introduction of LTs with respect to the standard functionality. The only penalty introduced is related to the current consumption that is required to make the LT emit light. This drawback can be overcome by using the control unit to enable and disable the LTs only in specific conditions (e.g.,

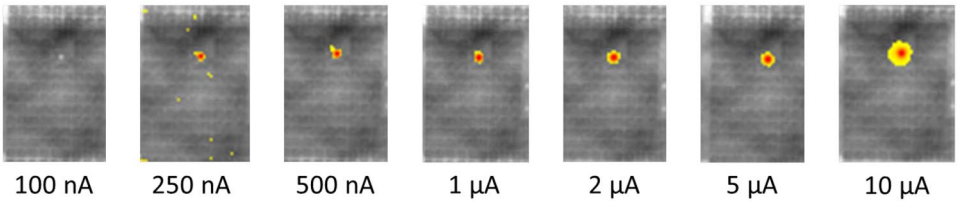

Fig. 6 Diode light emission characterization with different voltage polarizations. Here is reported for each value of the current flowing in the junction, the image of the light emitted by the diode

debug mode). LTs do not need to be co-designed with the circuit. A library containing different kinds of LTs can be created, and they can be added a posteriori once the design of the circuit is finished. In fact, LTs can be seen as light probing points. The choice of LT to be used depends, in fact, only on the signals to be monitored. In this sense, the only adaptation needed is for the control units to process the signal for the emitting unit. Finally, today's placement is completed by layout designers using their expertise with the assistance of FA engineers. It is possible to automate such a process with an algorithm that follows standard layout rules, and this aspect will be a subject for future study. The number of LTs needed to monitor a circuit depends on the type of fault to be detected. The number of LTs needed to monitor a circuit depends on the type of fault to be detected.

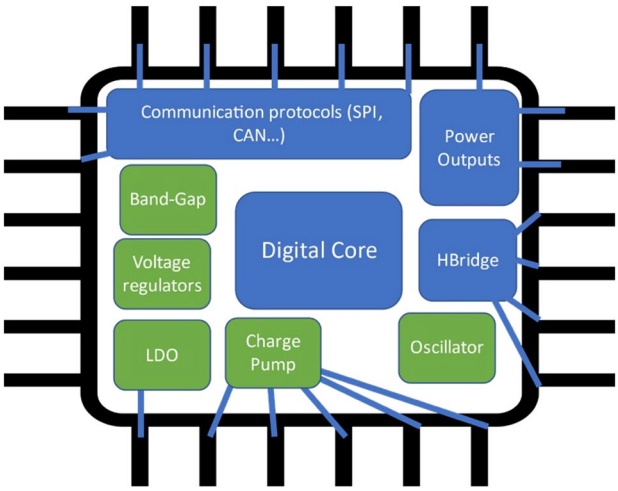

Fig. 7 Example of door-zone device. In green, the core functionalities for the circuit startup, are highlighted

5 Results

This section presents results from the methods previously explained. The first part reports a failure analysis case in which the light emission is exploited as input for the AFS.

The second part is dedicated to the results of the LTs inserted in a real IC for automotive purposes. First, the simulation of a single LT is presented to determine the values characterizing the light emitted from it. After that, some trials of physical fault injection and simulation are described.

The third part presents a real-life failure analysis of a device where LTs are not present. It is an example of a complex analysis solved with many techniques and simulations. The goal is to show how, with LTs, the same analysis would have been solved much more efficiently.

The circuits inspected are mixed-signal, analog-on-top devices for automotive purposes. This indicates that while they are made up of both analog and digital circuitry, the analog part makes up the majority of the circuit. These circuits are of the same type, and the main functionalities are reported in Fig. 7. They have communication-specific functional blocks (e.g., CAN, SPI, etc.). Depending on the size of the circuit, they have a multitude of power outputs (to drive lights, for example); a half-bridge circuit to drive DC motors (e.g., window lifters); a number of internal and external voltage generators, including a charge pump circuit, low-dropout, band-gap, and voltage regulators. The digital core circuit generates a clock using an oscillator. This clock is used by many internal subcircuits.

5.1 Light Emission in Automated Fault Diagnosis

This failure analysis case deals with a mixed-signal circuit used inside the car doors. In particular, a failure of a specific voltage output affected the faulty device. The failure mode was validated inside the laboratory with both the ATE and the electrical bench. The output was measured at a correct value of 0.6 V, like the golden unit, when it was driven off. When turned on, it measured 1.5 V rather than the 12 V of a good device. The sample was submitted to a backside sample preparation, to access the silicon surface and perform the EMMI inspection. In the meantime, the simulation was prepared both for the EMMI (see Fig. 8A) and to use the diagnosis through the AFS. This latter was possible since, with such a failure mode, the area of the device to analyze and the macro functionality were already defined. Indeed, there is a specific IP that drives the output inside the device. A simulation test bench for this IP was prepared for diagnosis by imposing a first fault criterion on the faulty output range. The number of components of this power output is 908, including 180 transistors, 140 resistors, 268 capacitors and 220 diodes. The fault universe for this block was composed of 2290 possible failures to inject. After the first

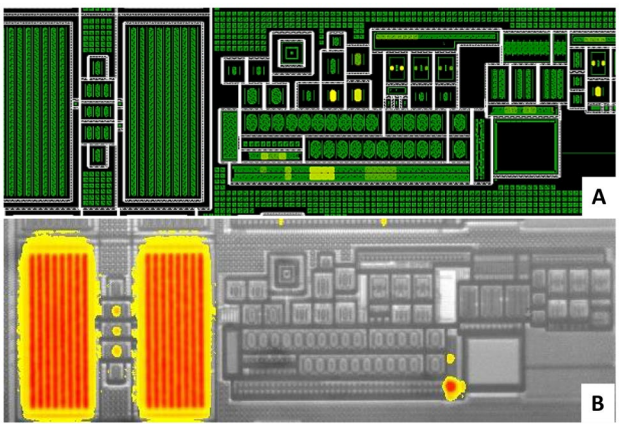

Fig. 8 **A** EMMI simulation in nominal conditions on the area affected by the failure (Output); **B** EMMI image of the DUT in the OUT area

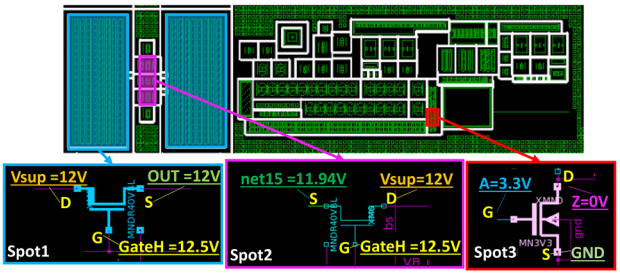

Fig. 9 On the top layout view of the output area. The main differences of Fig. 8A and B are highlighted with different colors. On the bottom the transistors corresponding to each highlighted spots and their nominal simulation values

iteration with the criterion for the output (V(output) < 2 V) the tool returned 525 candidates. The analysis continued with the EMMI inspection of the DUT in the area of the output (see Fig. 8B). From the comparison between this image and the simulation in nominal conditions, many differences were present. Yet none of these could directly point out the faulty location, since they were consequences of the failure. For this reason, we started the process explained in Section 3 by focusing on the different light spots. We began by inspecting the largest spot (see Fig. 9 spot 1) and locating it within the layout. It is a transistor whose nominal operating condition is cut-off. In fact, its gate-source voltage is higher than the threshold voltage (0.7 V), and even if its drain is connected to the supply (12 V), the source is the output of the circuit (nominally at 12 V). As a result, the lack of emissions in the good unit is explained. However, because the source is at 1.5 V (faulty output), the emission from the failed device was also understood for spot 1. Therefore, no further variation can be used as a criterion for the emission. For this reason, an additional spot was analyzed and located within the layout (see Fig. 9 spot2).

The second transistor was also in cutoff, since the source and drain were both at 12 V and the gate at 12.5 V. In this case, however, an assumption can be made to explain the emission in the failed device. In fact, only a source voltage lower than 11.7 V would cause the transistor to work in saturation. Applying this as the second criterion of the diagnosis, we have obtained 36 candidates. Finally, one last spot was analyzed. It was still a nMOS of a NOT logic gate (see Fig. 9 spot3). In this case, the transistor was in cut-off, and only an intermediate level of the gate could explain the emission of the faulty unit. In this way, we imposed as a third criterion the gate-source voltage of this transistor between 1.0 V and 1.5 V. We only got one candidate using this criterion. The candidate was a short between the gate and the drain of a transistor (see Fig. 10A). The results of the physical analysis confirmed this hypothesis. A leakage between the VIA (source) and the polysilicon (gate) of the candidate transistor was observed (see Fig. 10). Finally, the EMMI simulation as a consequence of the fault injection has been performed, resulting in a good match with the real image of the DUT (see Figs. 8B and 10C).

5.2 Light Tracker Application

In a real circuit for automotive purposes (similar to Fig. 7), we inserted LTs to detect startup failures. Such faults are difficult to monitor because circuit functionality is disabled,

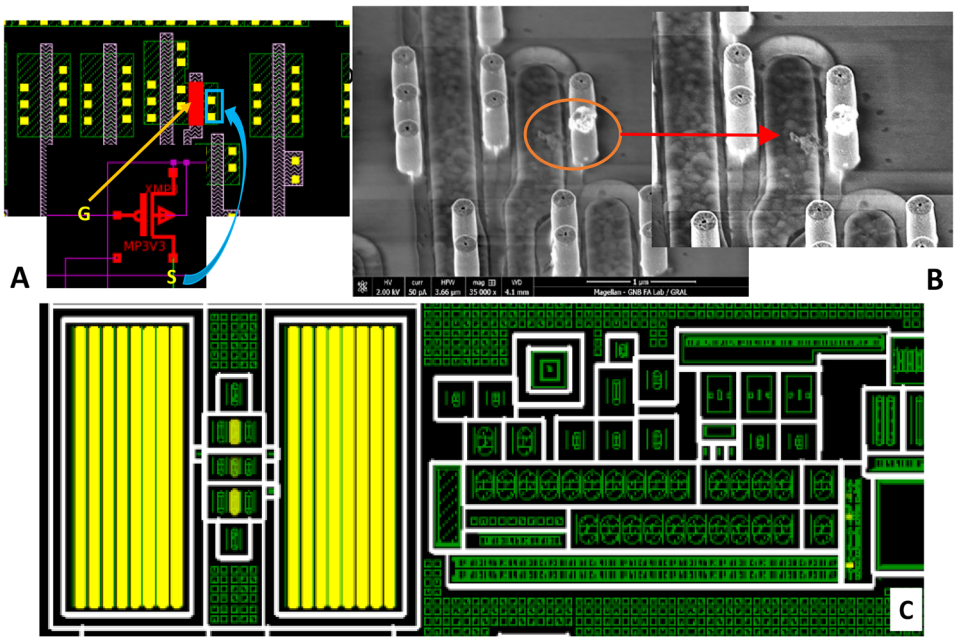

Fig. 10 **A** layout and schematic view of the candidate found with the AFS and the fault criteria; **B** SEM image of the defect highlighted in red; **C** EMMI simulation as a consequence of the fault injection inside the candidate

and testing is therefore limited. The number of LTs needed to monitor a circuit depends on the type of fault to be detected. This circuit consists of about 16,700 electronic components, including about 10,000 transistors. Hence, LTs were used to understand the functionality that is failing upstream of the startup sequence. For this reason, the outputs of the fundamental blocks that are used in the startup sequence and that cannot be measured externally were monitored. In this case, there were 5 of these blocks, and consequently, 5 LTs were used. The area of a single LT is about 1780 μm^2, which for 5 LTs is 0.11% of the total area of the device. The five subcircuits monitored are: a bandgap circuit (BG), an oscillator, a low-dropout (LDO) voltage generator, a voltage reference (VREF), and a digital signal used as an enable for a charge pump circuit (CP). The bandgap circuit is composed of 830 components, including about 670 transistors. The oscillator contains 170 components (140 transistors). The LDO consists of 615 components, including 500 transistors. The VREF has 500 components and about 170 transistors.

We ran the simulation following the flow of the single analog subcircuit instead of running the whole mixed-signal circuit simulation. This allows for an overall faster simulation. It is also the situation that is more similar to a real failure analysis. In fact, it is recommended to isolate the non-working portion of the circuit and run the simulations only on that. This is generally done using standard failure analysis techniques. However, using the single subcircuit simulation flow, we will not be able to test by simulation one of the 5 LTs. In fact, one of them is connected to a signal from the digital part of the circuit. This signal is directly dependent on analog functionality. Therefore, to simulate this specific LT, it would be necessary to extract a digital part and merge it with the analog block. The results of such a simulation are accessible via top-level mixed-signal simulators. Yet, this solution will not be discussed in this work. In fact, they would need a much longer simulation than would be necessary to understand this method. Nevertheless, this does not inhibit correct localization during an analysis. In fact, this was proven with real results after the physical fault injection involving this specific LT.

5.2.1 Nominal Behavior

The simulation is the first step in determining which values to associate with the enabled emission unit. The integrated circuit presents three types of LTs. They differ from each other for the control unit and the resistance of the emitting unit, as explained in the previous chapter. We prepared a virtual test bench to check them, using an ideal voltage generator as input. The resulting current flowing in the diode with forward bias is about 1.24 uA as shown in Fig. 11. This means that the emitting unit is activated when there is a positive current of about 1.24 uA, flowing through the

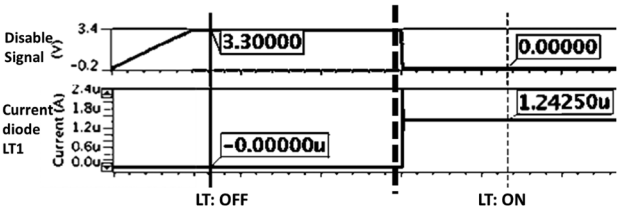

Fig. 11 Simulation of a single LT in nominal conditions. On the left the LT is in OFF state; on the right it is activated

diode. It is in fact, coherent with the values reported in the previous chapter of this paper. In the case of the test bench with ideal generators, the current flows with a positive sign when the diode is forward biased. This type of simulation aids in the construction of the truth table, which allows for failure diagnosis. We performed four simulations to validate all the LTs and allow further fault injection both in simulation and inside the circuit.

Within the circuit a specific LT is activated when the corresponding signal is not generated correctly. This is the LT associated with the bandgap voltage. It was possible to configure it differently from all the others without compromising the safety of the circuit. In fact, associated with the bandgap voltage is a digital signal that deactivates all the other analog blocks when the bandgap fails. The LT has been connected to this last signal, which becomes an enable for the emitting unit when the bandgap fails. All other LTs emit when the signal they monitor is not generated successfully.

After the simulation step, a back-side sample preparation was done to access the silicon surface. We performed an EMMI analysis focusing on the emitting unit, and we focused on the LTs to validate this method.

Inside a golden sample, we observed four emitting units activated and one LT in an off state (Fig. 12a). Among the emitting units in Fig. 12a, we note that the LT5 has two extra spots in addition to the diode spot. This LT monitors an oscillator. Therefore, the extra spots are a normal consequence of this application. They are located inside the control unit, at the input. They are transistors that switch between a cut-off and a saturation mode due to the oscillator signal. It is known that transistors in the saturation region emit light due to hot carriers [12]. It is also known that this emission is stronger for nMOS transistors than for pMOS transistors. In fact, in this case, the emission is within the nMOS. Moreover, the simulation shows how the current inside the LT switches between positive and negative values (see Fig. 13). Therefore, the value of the current to be considered for the emission is the average. As a consequence, the transistors will emit light with average behavior like the LT5.

With these measurements, we have proven the nominal functionality of this circuit.

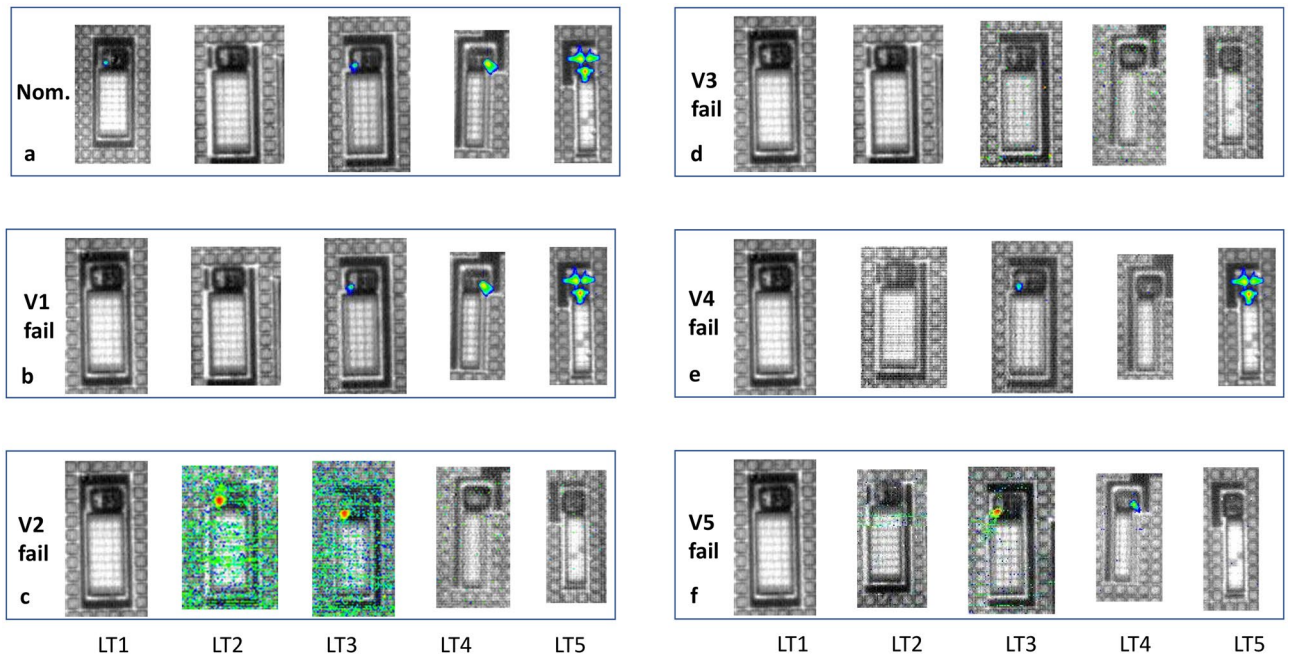

Fig. 12 EMMI acquisitions of all the LT in different circuit conditions. **a** the circuit is in a nominal state; **b**, **c**, **d**, **e**, **f** a physical fault injection has been applied to the circuit in one of the signals monitored by the LTs

5.2.2 Fault Injection

In order to understand the behavior of the LTs in a fault situation, we first performed simulations. Resistive faults were injected into the test benches used for nominal simulation. This allows one to understand the consequences of an injected fault in a circuit's functionality in the various LTs. Simultaneously, to confirm the results of the simulations, faults were added to the real circuit. To do this, the sample was first prepared by discovering the silicon on the backside. Then the backside was sealed with a transparent resin to allow EMMI analysis. Then the sample was opened from the front, in order to access the metal layers and physically inject the faults into the circuit. A focused ion beam (FIB) was used for fault injection. Platinum straps were created to reproduce resistive shorts (see Fig. 14).

Physical and simulation fault injections were done, considering only one fault at a time. This is a general assumption

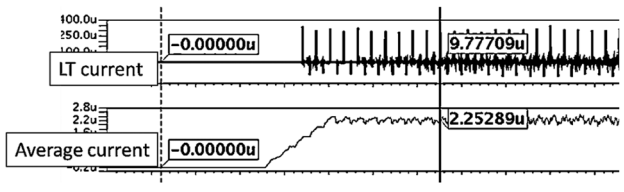

Fig. 13 Simulation results of the LT5. On the top there is the current flowing inside the diode of the LT with positive and negative peaks. On the bottom the average current of the LT

that is made in failure analysis. It is always supposed that there is only one defect in the circuit, and a unique cause is assumed. In a first step, fault injections were made only to test the correct operation of the LTs. This means that the first faults were injected into the signals monitored by the LTs. We performed a total of five physical fault injections (see Fig. 12) and four simulations. The results are reported in Table 1. In this table, all the fault simulations are reported except for V1, in which the fault simulation was not performed for the reason previously explained. Table 2 can be deduced directly from Table 1 and Fig. 12. The simulation results do, in fact, match the real-world behavior of the circuit. Table 2 is the starting point if a real failure occurs in the device.

From these results, we can observe that only the first fault injected causes one commutation of the LTs. In this case, the commutation is for LT1 linked to V1. It is the only signal that does not cause any other consequences at the other nodes monitored by the LTs. In all the other cases, as a consequence of a fault injection, many LTs changed their state. This confirms that the information provided by this method must be read in its entirely without considering individual LTs.

In a second phase, we performed a fault injection within the subcircuit that generates the internal reference voltages. This subcircuit is the most involved in the startup sequence. In fact, it provides the internal voltages needed for the IC to start correctly. Three LTs are also associated with this subcircuit. Since the operations of the LT have been proven in the first phase, we performed this step through the simulation.

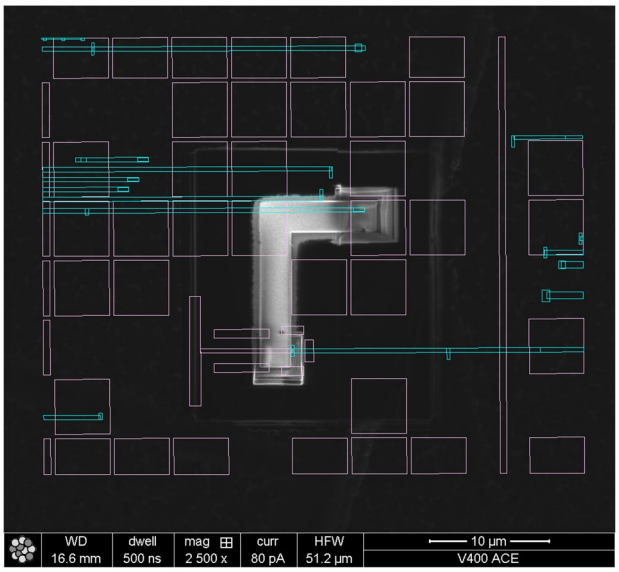

Fig. 14 Example of FIB strap to create a short between two signals allowing a physical fault injection

Multiple fault injections have been performed to study the fault detectability of LT in this subcircuit. Based on these findings, a coverage of approximately 73% of startup faults has been estimated. In this case, we consider a fault detected when the LTs switch with respect to the nominal state at least once. Some of these faults are not directly detected by the LTs, and therefore the subcircuit is not fully covered. Being an analog circuit, the reading of the individual LTs gives a partial fault response, and ambiguities are present in this regard. To resolve the ambiguities related to the individual LTs, it is recommended to read all the LTs that give global information about the fault. In this way, the failing block of the circuit can be detected. Based on that, inside the failing block, there are multiple faults that can create the same LT signatures, introducing fault ambiguities. The fault diagnosis with AFS and the first method described in this paper can be used to resolve such ambiguities. This is also the main reason why LTs, as of today, cannot be used alone for fault diagnosis but rather as a support for it. Finally, real tests have been made by injecting the FIB faults inside the mentioned subcircuit. The results of these tests are also consistent with the simulation and show how this approach enables fault detection (see Fig. 15).

Finally, the simulation results match the results obtained in the real samples. This was proven by the EMMI analysis.

Table 1 Simulation of fault injections

LT1 (A)	LT2 (A)	LT3 (A)	LT4 (A)	LT5 (A)	Status
-	0.034u	1.34u	1.46u	2.26u	Nominal
-	0.08u	0.04n	0.04n	0.03n	V3fail
-	0.034u	1.33u	1.45u	0.003n	V5fail
-	-	-	-	-	V1fail
-	1.24u	1.12u	0.04n	0.04n	V2fail
-	0.023u	1.38u	0.05n	0.03n	V4fail

Table 2 Light trackers status

LT1	LT2	LT3	LT4	LT5	Status
ON	OFF	ON	ON	ON	Nominal
OFF	OFF	OFF	OFF	OFF	V3fail
OFF	OFF	ON	ON	OFF	V5fail
OFF	OFF	ON	ON	ON	V1fail
OFF	ON	ON	OFF	OFF	V2fail
ON	OFF	ON	OFF	ON	V4fail

5.3 Real Failure Analysis Case

This failure analysis deals with a charge pump circuit [28]. It is a circuit to obtain an output voltage (CP) higher than the supply voltage (Vsup). The voltage conversion is possible thanks to a clock signal with its switching action and the energy storage of capacitors.

In this particular device, the CP voltage is given by:

$$Vcp = Vsup + 12 \tag{3}$$

with Vsup generally at 12 V

This voltage signal is especially important for the normal working conditions of the device. Without CP, the SPI internal registers are no longer accessible. So, all internal device voltages are no longer testable, making the failure analysis extraordinarily complex indeed. The CP circuit of this device is composed of 210 transistors, 15 resistors, 2 capacitors, 6 BJTs, and 20 diodes.

In this particular case, the device presented a failure in the CP voltage when it was heated. In detail, the device could start in nominal conditions with all the outputs properly working. After 2 min of heating, the CP voltage dropped from 24 to 12 V. According to the workflow presented in Chapter 2, the failure was confirmed with the ATE. Specifically, the device passed at room temperature and cold, but failed at hot. The failure mode was then characterized and reproduced on the electrical bench in the laboratory. This allowed further analysis inside the equipment.

The sample was prepared to discover the backside silicon surface and allow the EMMI inspection. The device was analyzed in both a nominal and faulty state using the Meridian IV microscope.

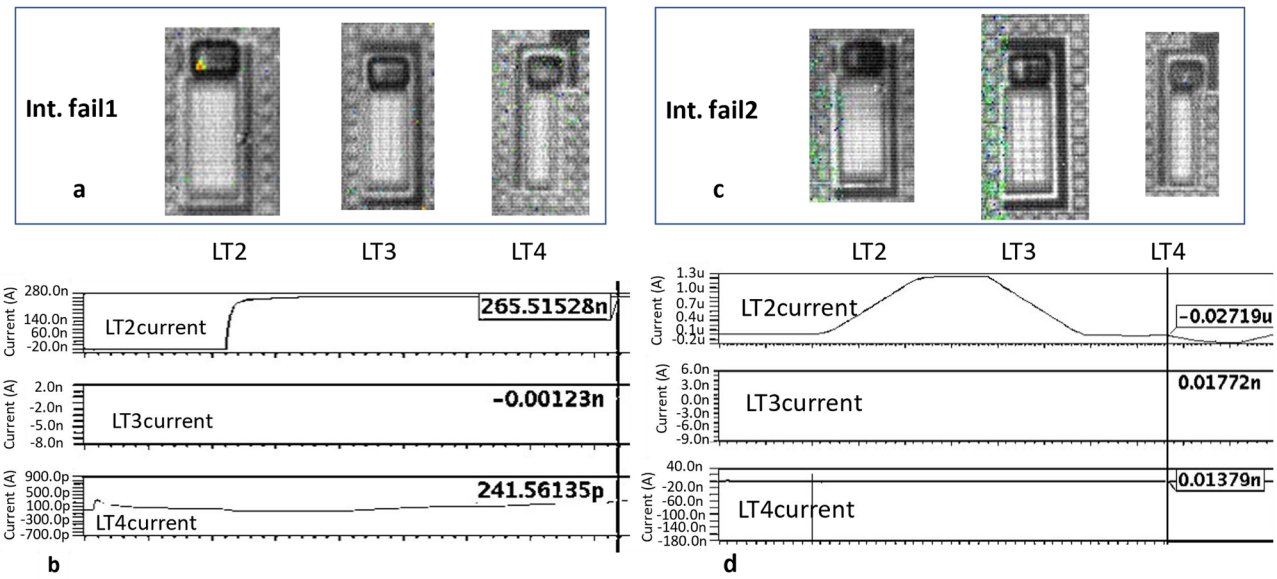

Fig. 15 Fault injection inside the voltage circuit. **a** EMMI result for a fault injection inside this block; **b** the simulation results of the injection of (**a**); **c** EMMI results for the second fault injection inside the same circuit block; **d** simulation results for the injection of (**b**)

Comparing the images of a good unit and the faulty unit at 1 × magnification, no anomalies were observed when the device was in its nominal state. In the failure conditions, a difference in the EMMI images was found in the CP area. This circuit part was inspected in more detail, but only the consequences of the failure were visible (see Figs. 16a and 17a). From the EMMI images, it was not possible to directly locate a faulty area. Therefore, simulation was used to solve this case. An emission simulation was first run to reproduce the nominal conditions (see Fig. 16b). Once these conditions were verified, three possible hypotheses of failure were found. With the simulation, is possible to evaluate them. The goal was to check if the consequences of such hypotheses caused an emission similar to that of the real device. From the results obtained (see Fig. 17), only the third failure hypothesis (see Fig. 17c) was consistent with the real image of the DUT (see Fig. 17a). This hypothesis involved a failure inside the clock signal used by the charge pump circuit. A failure on that signal is most likely related to the oscillator generating the clock. For this reason, the circuit area of the oscillator was investigated with physical analysis. With a layer-by-layer inspection using the scanning electron microscope, an anomaly was first observed at the contact level (see Fig. 18a). It was inside a transistor inside the oscillator, presenting an abnormal signature from a passive voltage contrast image. After contact removal, a defect

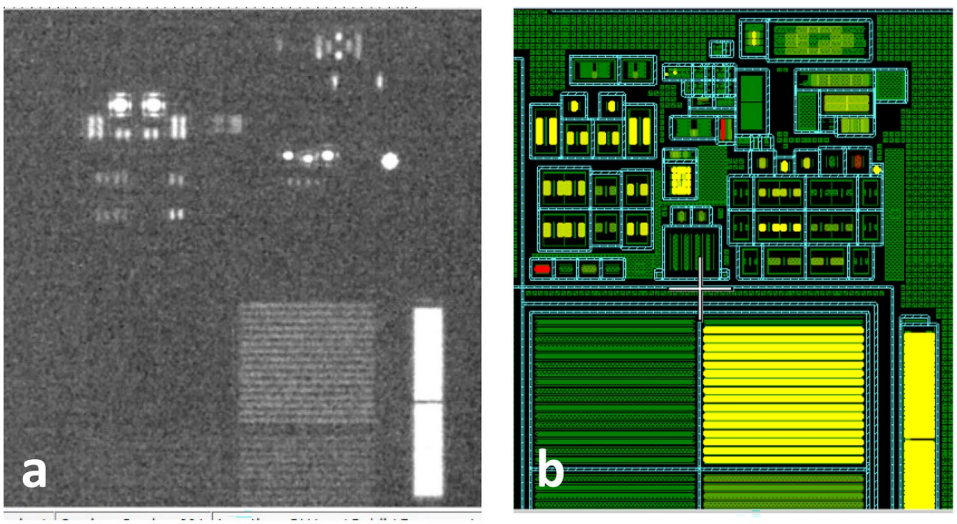

Fig. 16 **a** raw EMMI image of the CP circuit block in nominal conditions; **b** EMMI simulation of the same circuit in the same conditions

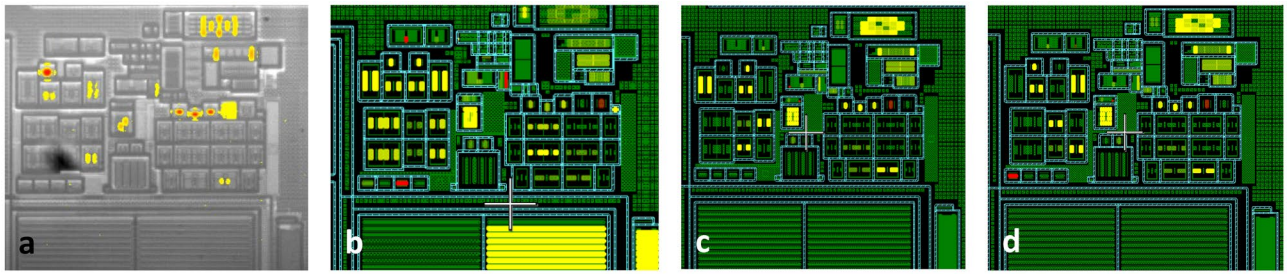

Fig. 17 **a** EMMI image of the faulty sample in the CP area; **b** EMMI simulation results concerning the first hypothesis of fail; **c** EMMI simulation results concerning the second hypothesis of fail; **d** EMMI simulation results concerning the third hypothesis of fail. This is the hypothesis with the best matching with the real image (**a**)

was visible in the same area at the poly-silicon level (see Fig. 18b). Finally, the presence of the defect was confirmed at the active level, confirming the hypothesis developed during the fault isolation (see Fig. 18c).

The analysis case presented here has been solved thanks to the simulation. The emission simulation, in particular, enabled the PA by confirming many hypotheses. Even though the whole time of the analysis could have been improved with the availability of LTs. These can avoid the list of actions that lead to a successful outcome (image acquisition, analysis, research of possible hypotheses, nominal and hypotheses simulations). These actions are quantifiable with at least one working day and a maximum of three. Similarly, the hypothesis could have been validated through failure reproduction.. This is possible with FIB circuit editing on a good device, but it will take even more time to analyze. Conversely, LTs might be a good improvement in such a circuit. Indeed, in Chapter 3, the LTs were successfully applied to a similar device type in an oscillator. The CP can be another possible application if it is not testable outside the package (output pin). Essentially, these signals are fundamental for the nominal operation of the circuit and must be testable. With LTs connected to them, the analysis could have been smoothly solved by acquiring a few images directly from the failing sample. This would have drastically reduced the number of actions to be performed and the analysis time. In fact, the failure hypothesis would have been validated during the EMMI inspection by providing a real-time answer.

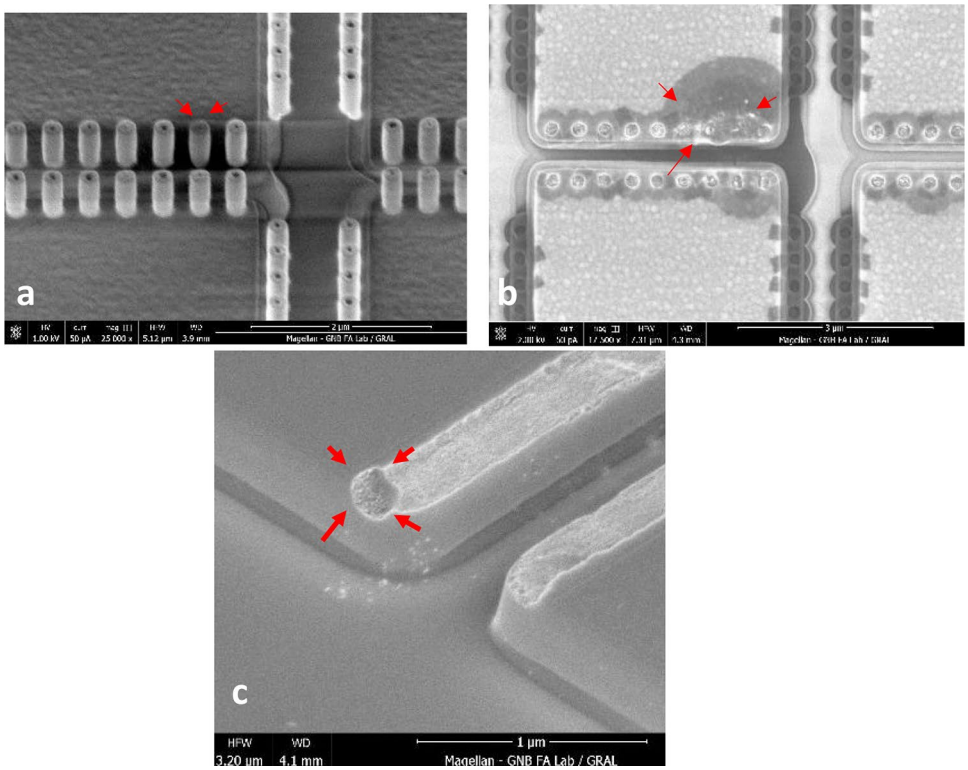

Fig. 18 **a** Passive voltage contrast at contact level. The abnormal contrast is pointed out by the red arrows; **b** SEM image of the same area with a defect at polysilicon level (red arrows); **c** SEM image of the physical defect at active level (highlighted with red arrows)

6 Conclusion

This work introduces two innovative approaches for the diagnosis of analog and mixed-signal circuits in automobiles. Such circuits indeed present many challenges for fault diagnosis and failure analysis. The solutions proposed in this paper exploit the ability of silicon to emit photons in the near-IR range. The first solution uses the consequences of the light emission in a failing integrated circuit to drive the diagnosis with modern analog fault simulators. The second solution, on the other hand, actively exploits the light emission phenomenon by strategically placing elementary emitting devices. Such devices serve to track the main functionalities of the circuit, reporting their status. In this way, a fault detection solution designed for failure analysis is provided. The basic actions and flow to perform failure analysis were first presented. Afterwards, the main ideas, the steps leading to their implementation, and the exploitability of such techniques were explained. We showed the results of a real failure analysis solved with the help of the fault simulators driven by the light emission measurements. This solution allowed us to solve a complex failure analysis case by successfully finding the physical defect. Other results concerned the light tracker solution implemented in a silicon integrated circuit. Using this circuit, we tested the nominal conditions. Moreover, we aligned the results of the simulation with the real-world behavior of the circuit through the photon emission images. After that, we explored the potentialities of the light trackers. We performed fault injections inside the device both physically and with simulation. The results proved that this idea is effective. In this way, complicated failure analysis could be performed by acquiring a few images. The use of such elementary devices actually helps to quickly isolate the upstream block of a failure within an analog circuit. The benefits will then be visible with faster and more accurate failure analyses. Evidence for this was reported in an example analysis where no light trackers were present in the circuit. This particular analysis required several steps, including image acquisition and simulation. The success of such an analysis was not compromised, but the number of actions and the time requirements were exceeded. All of this would not have been necessary if the light trackers had been used.

Future work will focus on the selection of the signal to monitor. This is crucial to obtaining a higher testability along with a better diagnosis, which has great impacts on failure analysis.

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Data Availability The data concerning the simulation results, which support the findings of this study are not openly available due to confidentiality reasons and are available from the corresponding author upon reasonable request. The authors declare that all other data supporting the findings of this study are available within the article.

Declarations

Conflicts of Interests and Competing Interests There is a potential financial interest because part of the content of the paper is related to a patent published in 2022 (EP3940401A1) in which some authors (M. Etienne Auvray and Dr. Tommaso Melis) were involved. Despite this fact, the value of this patent is not affected by the publication of this manuscript.

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Tommaso Melis received the B.Sc. degree in Electrical and Electronics Engineering in2016 and the M.Sc. degree in Electronic Engineering in 2018 from University ofCagliari, Italy. He received his Ph.D. degree in Nanoelectronics andNanotechnologies from University of Grenoble Alpes in 2021, while working withTIMA laboratory, EEATS doctoral school. Presently he is a failure analysisengineer at STMicroelectronics Grenoble, France, where he works in theautomotive and discrete group. His research interests currently focus on fault simulationand automatic diagnostic solutions for fault diagnosis of analog andmixed-signal circuits.

Emmanuel Simeu received master's and the Ph.D. degrees in AutomaticControl and System Theory from the INPG (Institut National Polytechnique deGrenoble) in 1988 and 1992, respectively. From 1989 to 1992 he was a researcherin CNET France Telecom research center. He has been the head of the riskmanagement department of the Polytechnic School of Grenoble INP since 2016.From 2010 to 2020, he was the leader of the research team RMS (ReliableMixed-signal Systems) at TIMA laboratory of Grenoble. He has been involved innonlinear systems modelling and control. His current field of research includesheterogeneous system modelling, reliability of embedded systems, and diagnosisand control of analogue/RF circuits.

Etienne Auvray was born in 1955 and received his MSC in Electronics from EcoleSuperieure d'Electricté in 1979. He worked on failure analysis of integratedcircuit in EFCIS Grenoble in 1979 and moved to Thomson CSF military and SpaceComponents near Grenoble with responsibility in the failure analysislaboratory. In 1996, he created Serma technologies Grenoble antenna dedicatedto failure analysis and starting FIB services. In 2001 he joinedSTMicroelectronics to work in the automotive and telecom laboratory to develop diagnosistools for failure analysis, until January 2021. He is now manager of FastnetTechnologies providing services in Failure analysis. He has published andparticipated in international conferences on failure analysis, and he holds onepatent.

Luc Saury received his MSC in Instrumentation from ISMRA / ENSI de Caen (F14) in1993 and his Ph.D. in Microelectronics from Université de Caen (F14) in 1998. Afteran initial work experience at Bureau National de Métrologie, he joinedSTMicroelectronics in 2001. He was appointed Principal Failure AnalysisEngineer in 2012 and Senior Member of the Technical Staff in 2013. He is nowleading the failure analysis team in charge of automotive products for STGrenoble. His field of expertise includes dynamic fault isolation techniquesand ATPG scan analyses. He has published and participated in internationalconferences on these topics in the last decade.