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Editorial

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This issue has eight articles. The topics discussed are hardware security (2 papers), analog and RF circuit testing (2), delay testing (1), test application, defect level and yield loss (1), and design for testability (2).

Hardware security is discussed in the first two papers. The first paper among these combines existing algorithms into a new one to detect hardware Trojans from side channel information. Contributors of this work are Tang, Su and Gao from Tianjin University of Science and Technology, Tianjin, China.

The second paper provides a method for securing the logic locking key against a SAT attack. The attack uses a SAT (Boolean satisfiability) solver to find the secret key. The authors propose the design of an anti-SAT block (ASB) to achieve security. Contributors are Naveenkumar, Sivamangai, Napolean, Sathya Priya and Ashika from Karunya Institute of Technology and Sciences, Coimbatore, Tamilnadu, India

Third and fourth papers, derived from the 22nd IEEE Latin-American Test Symposium, held at Punta del Este, Uruguay, during October 27-29, 2021, discuss analog and RF circuit testing. Among these, the third paper develops an indirect measurement method to monitor the performance of a radio frequency circuit. Easily measurable parameters are examined for their sensitivity to variation in performance. The selected indirect measurement provides an effective performance monitor. Authors are El Badawi, Azaïs, Bernard, Comte and Kerzerho from LIRMM, University of Montpellier, Montpellier, France, and Lefevre from NXP Semiconductor, Caen, France.

Fourth paper explores an interesting idea of embedding light-emitting diodes at selected locations on electronic chips used in automotive applications. The emitted signals provide diagnostic information. The authors are Melis and Saury from STMicroelectronics Grenoble, France, Simeu from University of Grenoble Alpes, CNRS, Grenoble, France, and Auvray from Fastnet Technologies, Grenoble, France.

Fifth paper is on delay testing. Machine intelligence is used to reorder tests while considering voltage, temperature, and delay characteristics of the circuit to improve test quality and reduce test application time. Contributors of this work are Song and Guo from Anhui University, Anhui, China, Huang from Hefei University of Technology, Anhui, China, and Milos from University of Potsdam, Brandenburg, Germany.

Sixth paper proposes a multiple retest system (MRS) that tries to make the most favorable tradeoff among defect level, yield loss, and cost of the final product. Authors are Yeh and Chen from National Central University, Jhongli City, Taiwan.

Seventh paper, the first of two papers on design for testability, proposes a novel design to reduce the application time of n-detect tests. These tests detect each modeled fault at least n times and are likely to detect many unmodeled defects as well, of course, at the cost of increased test time. A multiple input signature register of shadow flip-flops, receiving signals from a selected set of scan flip-flops, enhances fault detection rate. As shown, an effective way to select scan flip-flops is to pick out those with highest fault coverages. Authors are Jiang, Dworak and Manikas from Southern Methodist University, Dallas, TX, USA, Zhang from Cisco Systems, Inc., San Jose, CA, USA, and Nepal from University of St. Thomas, St. Paul, MN, USA.

The eighth and the last paper develops a concurrent test method to work in the functional mode. The idea is to sense selected input patterns as they occur in the normal operation and then compare the circuit output and the expected response, both in compressed forms. The hardware added to the circuit includes a test pattern detector, a decoding module, and several linear feedback shift registers (LFSRs). Contributors of this work are Menbari and Jahanirad from University of Kurdistan, Sanandaj, Iran.

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