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An Investigation into the Failure Characteristics of External PCB Traces with Different Angle Bends

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Abstract

The design of a Printed Circuit Board (PCB) involves satisfying numerous design constraints in terms of the positioning of components and the routing of conducting tracks or traces between components. One common design constraint is limiting the maximum angular bend that a trace can make (e.g. to 45°) for several potential reasons including reliability. In this paper, we systematically investigate the failure characteristics of PCB external traces with different angle bends to understand the implications in a modern context with modern PCB manufacturing processes. This involves destructive testing of straight traces with no bends, traces with only 45° bends and traces with only 90° bends. There are three aspects to the testing: (1) maximal current testing, in which the maximum current that a trace can withstand before failure is measured, (2) failure location testing for traces with bends i.e. trace failed on straight segment or at the bend, and (3) time to failure testing. We did not find a large difference between the maximum currents that can be withstood by straight traces, traces with 45° bends and traces with 90° bends. However, some of the interesting results are that traces with 45° bends are significantly more likely to fail at the location of a bend than traces with 90° bends, and straight traces take much longer to fail on average than traces with bends for a given test current.

Keywords PCB (Printed Circuit Board) · Reliability · Design rules

1 Introduction

There are many formal and informal design rules in Printed Circuit Board (PCB) design covering the positioning of components and the routing of conducting tracks or traces between components. One common design constraint, although not universally accepted or applied, is limiting the maximum angular bend that a trace can make (e.g. to 45°). The rationale for such a design rule varies between sources. In [12], it is stated that 90° bends in traces should not be used because of the non-ideal nature of the PCB manufacturing process. Specifically, during chemical etching to remove non-conducting areas of a PCB layer, the corner of a 90° bend may be etched back such that the width of the trace at the corner will be lower than the nominal width. This is particularly an issue with relatively thin traces (e.g. a trace width of 5 mil) and can lead to the inability to carry a specified current without failure or other reliability problems such as delamination of the trace from the PCB. In [6], it is stated that 90° bends in traces should not be used primarily for aesthetic reasons, although the possibility of manufacturing implications is also suggested. Both sources agree that, contrary to popular belief, 90° bends in traces do not actually lead to significant increased Electromagnetic Interference (EMI) at high frequencies due to radiated Radio Frequency (RF) emissions, and this is supported further in [11].

Given the maximum angular bend design rule has existed for decades, there is a question about whether it should still be applied for reasons of reliability in light of modern PCB manufacturing methods and tolerances. If the rule is no longer valid from a reliability perspective, PCB designers would have greater freedom in their designs, particularly with respect to the use of 90° bends, and this could potentially translate into further benefits e.g. more compact routing. This investigation is particularly of interest for relatively thin traces, given over-etching of such traces at bend locations may lead to significantly reduced

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width (and therefore possibly reduced reliability). In this paper, we report on the results of testing PCBs containing multiple straight traces, PCBs containing traces with only 45° bends and PCBs containing traces with only 90° bends. In all cases, the PCBs are rigid not flexible i.e. they are based on a solid substrate such as FR-4 that cannot be easily bent or flexed without potentially damaging some aspect of the PCB. In addition, the traces are external (i.e. on the top or bottom layers of the PCB) and the traces are of nominal width 5 mil, which is typically the smallest width that PCB manufacturers will currently accept for manufacture of general purpose designs.

We first examine whether there is any significant difference between the three types of test traces with respect to the maximum current they can carry before failure, with the assumption that if thin 90° bends are particularly susceptible to over-etching during manufacture, traces containing these bends will fail at a lower current than straight traces or traces with 45° bends. As a secondary objective of this maximal current testing, we determine the failure location of the traces with bends, in particular in terms of whether they failed on a straight segment or at a bend. Thirdly, we examine the time to failure of the different trace types with a specific sustained test current.

The contributions of this paper are as follows:

- Development of a methodology for testing the reliability of different angle bends in PCB traces in terms of maximal current testing, failure location testing and time to failure testing.
- The discovery that there is not a very significant difference between the maximum currents that can be withstood by straight traces, traces with 45° bends and traces with 90° bends, at least for the test PCBs we employed. However, we did observe some variance between different PCBs with the same trace type, which indicates that the manufacturing process is not always uniform.
- The somewhat surprising discovery that traces with 45° bends are significantly more likely to fail at the location of a bend than traces with 90° bends.
- The interesting result that straight traces take much longer to fail on average than traces with bends for a given test current.

The structure of the paper is as follows. In Sect. 2, we report on related previous work from the literature. Section 3 describes the methodology we employed for maximal current testing, failure location testing and time to failure testing, including details of the test PCBs that were manufactured for this purpose. Section 4 presents the results and our analysis of these results. In Sect. 5, we discuss our conclusions and how the work can be progressed further in light of the results obtained in this paper.

2 Related Work

There has been very little prior work with regards to scientifically investigating the potential for 90° bends in PCB traces to cause reliability issues due to over-etching during the manufacturing process, at least in recent times. This further motivates the current study, particularly as we wish to understand whether modern manufacturing processes render the maximum angular bend design rule obsolete.

However, there has been some loosely related research. The review into PCB defects in [15] discusses over-etching and its impact on traces, but the potential impact of trace angle on over-etching and therefore reliability is not covered. An investigation into the maximal current of conducting traces in high power flexible PCBs is discussed in [8] using ANSYS Workbench simulations. However, this study is quite different to ours, even though both involve maximum current testing, since the research in [8] is not concerned with the reliability of different angle bends in traces, and is for flexible PCBs rather than rigid PCBs. In [1], there is a review of design principles for 90° bends in PCB traces for high speed and mmWave circuits. The authors conclude that the sharp 90° should be rounded or mitered for performance reasons in terms of insertion and return loss, but there is no discussion about reliability. A transmission line model for microstrip traces with 90° bends is developed in [13], but again this is not related to reliability.

There has been considerable research into general reliability aspects of PCBs including thermal and mechanical reliability. In [14], the authors investigate the root causes of intermittent failures in electronic products, citing the PCB and component-PCB interconnects as two of the drivers of intermittent failures. This includes reliability issues associated with traces which is related to the research in this paper. Regarding mechanical reliability, the research in [2] investigates varying the thickness of the PCB board on the lifetime of a Ball Grid Array (BGA) solder joint using a Finite Element (FE) model and experimental investigation. The authors conclude that stiffening the board increases the lifetime of the BGA joint significantly. In [9], research into the reliability of copper traces using accelerated stress tests is undertaken. The authors conclude that failure due to tensile stresses are usually located at the junction of the trace and pad, and that equality in trace and pad dimensions increases reliability. They also find that traces which are perpendicular to the length of the board are more reliable. The reliability study in [10] agreed with the previous study in that trace failures are almost always at the junction of the trace and pad, and that equality in trace and pad dimensions increases reliability.

Failure of a PCB trace can also lead to signal integrity issues between nearby traces. An overview of signal integrity

Table 1 Test PCB Parameters

Parameter	Value
Manufacturer	JLCPCB
Substrate	FR-4 TG130
Board thickness	1.6 mm
Board size	100 mm x 100 mm
Number of copper layers	2 (Top and Bottom)
Surface finish	Hot Air Solder Levelling (HASL)
Trace thickness	34.29 µm (1oz of copper per square foot or 1.35 mil)
Trace width	0.127 mm (5 mil)
Trace length	85 mm (for straight traces) 145 mm (for traces with 45° and 90° bends)
Number of bends per trace (for traces with 45° and 90° bends)	28

issues in PCBs is provided in [16]. The research in [3] and [7] investigates signal integrity design for high speed digital circuits and includes in particular discontinuity modelling and characterization which is related to reliability.

3 Methodology

3.1 Test PCB Specification

Table 1 illustrates the parameters of the test PCBs employed in this study. The rationale for using some of these parameter values specifically (for example, a trace thickness of 34.29 µm) was that they are commonly employed values for commercial PCBs. The trace width of 0.127 mm (5 mil) is the smallest commonly available width that can be manufactured at a reasonable cost and requires the least current (of commonly available widths) to overload the trace.

Figure 1(a), (b) and (c) illustrate samples of the test PCBs with straight traces, traces with 45° bends and traces with 90° bends respectively.

3.2 Test PCB Preparation

Before any testing was undertaken on the PCBs, the following preparations were carried out to ensure consistent results across the whole batch:

1. Visual Inspection: Despite the fact that the PCB manufacturer performs flying probe testing to ensure that no unintentional open or short circuits exist before shipping, it is still possible that other defects exist from the manufacturing process (e.g. traces with varying width) or from shipping damage. The visual inspection tests removed PCBs or individual traces with obvious visual damage from further consideration. Quality testing was carried out following the IPC-TM-650 [5] standard. Inspections

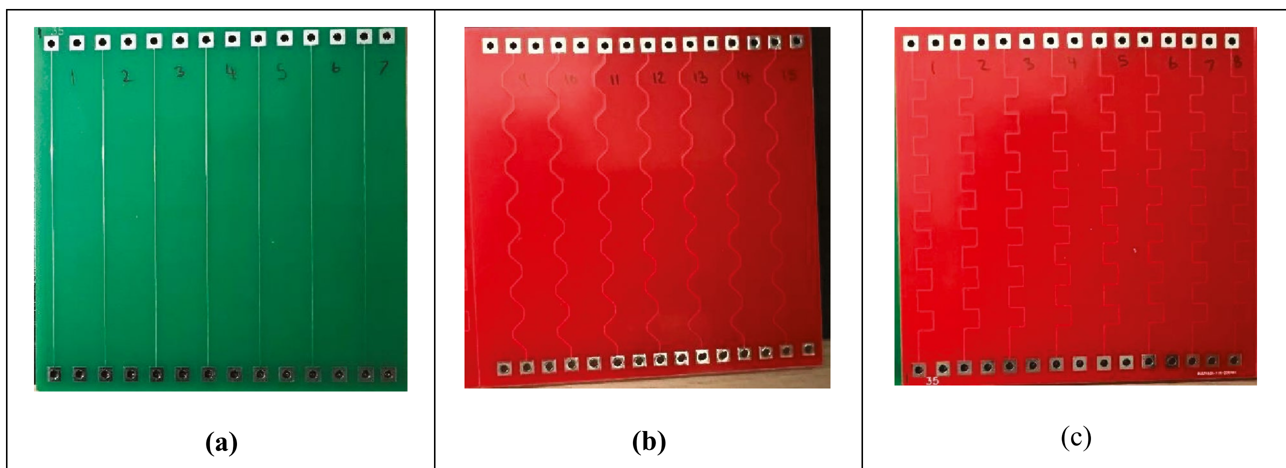

Fig. 1 Photos of PCBs with **a** Straight traces, **b**, Traces with 45° bends, and **c** Traces with 90° bends

were done using a magnifying glass. Particular attention was paid to 45° and 90° bends to determine if any obvious etching or cracking problems had occurred.
2. Acclimatisation to Ambient Conditions: Once all PCBs had been unpackaged, they were subject to an acclimatisation period of at least 1 day to balance temperature and relative humidity as set out in IPC-TM-650 [5]. The values were then recorded each testing day to ensure being inside the recommended ranges for testing. These ranges are 22 ˚C ± 3 ˚C for temperature and 50% ± 10% for relative humidity.
3. Cleaning: Immediately before each PCB was tested, precleaning using distilled water and isopropyl alcohol was undertaken to eliminate foreign matter contamination on the pad.

3.3 Maximal Current Testing

Maximal current testing was performed on straight traces, traces with 45° bends and traces with 90° bends to determine whether there were any significant differences in the maximum current these traces could carry before they were destroyed.

The procedure adopted was as follows. Once cleaning had been completed for a trace, the ambient temperature was recorded and then the trace was subject to an initial current of 50% of the maximum current the IPC-2221 standard [4] recommend for a 10 ˚C temperature rise for 15 min. For an external trace width of 0.127 mm (5 mil) with a thickness of 34.29 µm (1oz of copper per square foot or 1.35 mil), the maximum current the IPC-2221 curves recommend for a 10 ˚C temperature rise can be calculated as 536mA, therefore the initial current was set to approximately 268mA. Note, the exact initial current value is not critical since the maximal current that will destroy the trace (for an unlimited temperature rise) will be much larger than this current.

Once the preconditioning current had been applied for 15 min, the current was increased by 100mA every 15 s until the trace was destroyed, and the maximal current recorded. The temperature at which the trace was destroyed was recorded using a FLIR camera; this was mainly done for interest rather than for analysis.

Once one trace had been tested/destroyed on a PCB, that PCB was allowed to cool back to ambient temperature before an adjacent trace on the same PCB was tested.

3.4 Failure Location Testing for Traces with Bends

For the testing of traces with 45° bends and 90° bends, once the trace failed as discussed in the previous section, inspections were conducted to determine the location of the failure. Often there was a spark at a specific location at the instant when a trace failed which identified the failure point. However, failing such an obvious visual indication, inspections were conducted with a magnifying glass or a microscope if needed. Each failure location was recorded and categorised as one of:

- a straight segment of a trace.
- a bend.
- a plated through hole or pad connector where the trace begins or ends.
- other, which comprises traces where the failure point could not be located unambiguously.

The aim was to determine whether there were any significant differences between traces with 45° bends and 90° bends with respect to the location of failures.

3.5 Time to Failure Testing

As a separate test from maximal current testing, the time to failure was tested by recording how long each trace survived with a sustained current of 2.83 A applied through it. This current was sufficient to destroy most test traces employed in this testing if sustained for a sufficiently long time. A timer was started as soon as the current was introduced and stopped when the trace failed. The aim was to determine whether there were any significant differences between straight traces, traces with 45° bends and traces with 90° bends with respect to the time to failure.

4 Results and Analysis

4.1 Maximal Current Testing

Table 2 illustrates the summary statistics, in particular the mean, median and the standard deviation, of the maximal currents for each of straight traces, traces with 45° bends and traces with 90° bends. The median is well known to reduce

Table 2 Summary Statistics for Maximal Currents

	Straight Traces	Traces with 45° bends	Traces with 90° bends
Number of samples	28	60 (4 PCBs x 15 traces)	60 (4 PCBs x 15 traces)
Mean maximal current	2.773 A	2.823 A	2.842 A
Median maximal current	2.773 A	2.831 A	2.904 A
Standard deviation	0.120 A	0.270 A	0.207 A

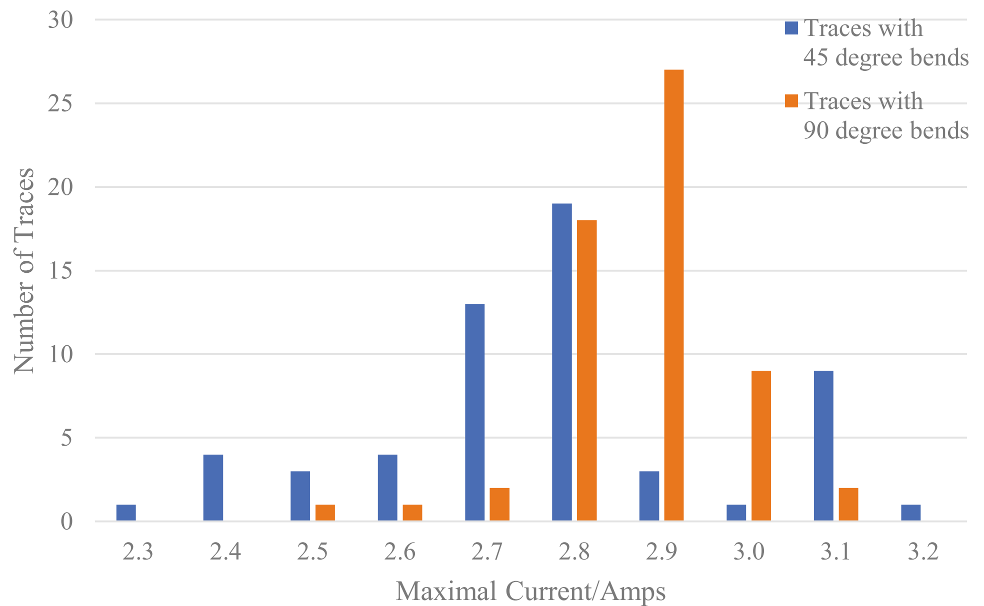

Fig. 2 Histogram of Maximal Currents for Traces with Bends

the effect of outliers in the measurements, which justifies its inclusion. At first glance, the maximal currents for the three trace types appear similar, perhaps indicating that the presence of bends does not clearly change the maximum current rating of a trace despite any over-etching that may occur at bend sites during manufacture. The standard deviation values demonstrate that the maximal currents have larger variability for traces with bends than for the straight traces. This could possibly indicate that the manufacturing tolerances are larger for traces with bends. However, we note from Table 1 that the straight traces, with length 85 mm, are shorter than the traces with 45° and 90° bends, which both have length 145 mm. Therefore, only the results for the traces with 45° and 90° bends are directly comparable with each other.

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It is also beneficial to examine the distribution of the individual maximal currents, in particular to understand whether they have a Normal/Gaussian distribution. Figure 2 compares the histograms of maximal currents for traces with 45° bends and traces with 90° bends, each of which are formed from 60 measurements as illustrated in Table 2. In order to explain the histogram bin labelling, for an example bin of 2.7 A, the measurement in this bin had a maximal current of greater than or equal to 2.7 A, but less than 2.8 A. The distribution of maximal currents for the traces with 90° bends appears somewhat Gaussian, but is left skewed rather than symmetric. The distribution of maximal currents for the traces with 45° bends is clearly multimodal (i.e. having multiple local maxima) rather than Gaussian. For example,

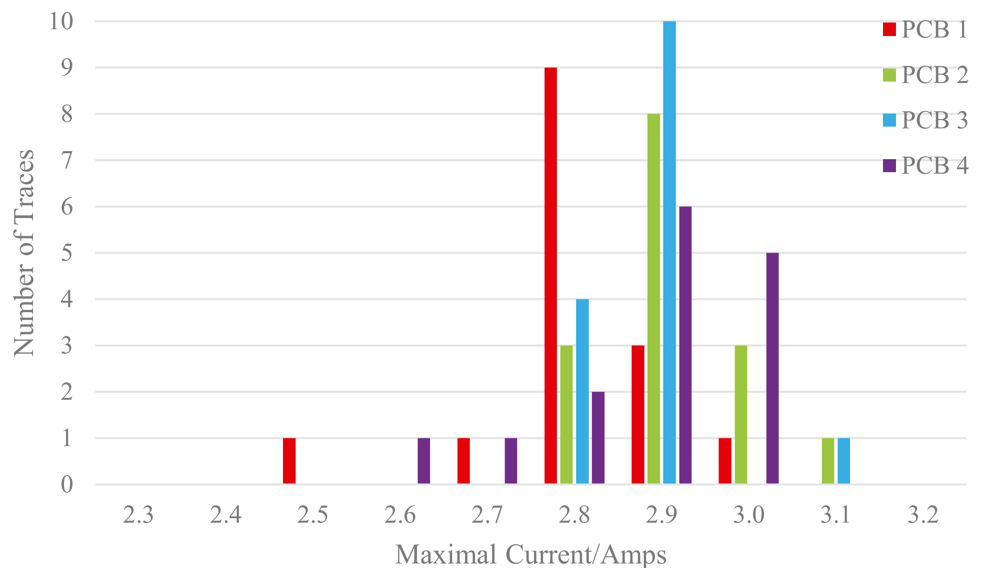

Fig. 3 Histogram of Maximal Currents for Traces with 90° Bends

Table 3 Summary Statistics for Maximal Currents Across PCBs For Traces with 90° Bends

	PCB 1	PCB 2	PCB 3	PCB 4
Number of samples	15	15	15	15
Mean maximal current	2.87 A	2.96 A	2.94 A	2.95 A
Median maximal current	2.87 A	2.96 A	2.93 A	2.98 A

looking at the histogram for traces with 45° bends, there are local maxima at 2.4, 2.8 and 3.1 A.

A possible reason for these observations is differences between the PCBs produced for a given trace type. The 60 samples tested for each of the traces with 45° bends and traces with 90° bends were distributed across 4 PCBs, with 15 traces per PCB. Figure 3 compares the histograms of maximal currents for traces with 90° bends as a function of the PCB on which the trace was located. Table 3 illustrates the summary statistics, in particular the mean and the median, of the maximal currents for each such PCB. The distribution of maximal currents for each PCB considered individually is basically unimodal (i.e. has a single local maximum), but the individual distributions exhibit clear differences both in terms of their mean values and variance. PCB 3 has the "peakiest" distribution (i.e. lowest variance in maximal current), whereas some of the other PCBs (especially PCB1 and PCB4) exhibit a relatively large variance in the maximal currents. This demonstrates that PCBs ostensibly made according to the same specification (and in the same manufacturing run) can exhibit significantly different electrical characteristics. From the perspective of characterising the electrical properties of traces with different bend angles, it suggests we not only need to consider a large number of such traces overall, but also a large number of PCBs accommodating those traces, in order to gain visibility of not just trace variations, but also PCB variations.

4.2 Failure Location Testing for Traces with Bends

Figure 4 compares the histograms of failure locations for traces with 45° bends and traces with 90° bends, each of which are formed from 60 measurements. There are significant differences between the results for the two types of traces. In particular, traces with 45° bends are more likely to fail at the bend than traces with 90° bends. Conversely, traces with 90° bends are more likely to fail on the straight segments of a trace than traces with 45° bends.

Figure 5(a), (b) and (c) show thermal images of straight traces, traces with 45° bends and traces with 90° bends respectively shortly before failure occurs due to overcurrent. These illustrate that the temperature at the hotspot or point of failure generally exceeds the maximum measurement temperature of 270 °C for the thermal camera in use when the failure occurs. Note that the failure location was not determined based upon these thermal images because the temperature distribution resolution along the trace is too low; instead, the methodology described in Sect. 3.4 was used to determine the failure location.

4.3 Time to Failure Testing

Table 4 illustrates the summary statistics, in particular the mean, median and the standard deviation, of the time to failure for each of straight traces, traces with 45° bends and traces with 90° bends. It is immediately clear that straight traces take much longer to fail on average than traces with bends, which suggests that straight traces are more robust than traces with bends. The time to failure measurements for

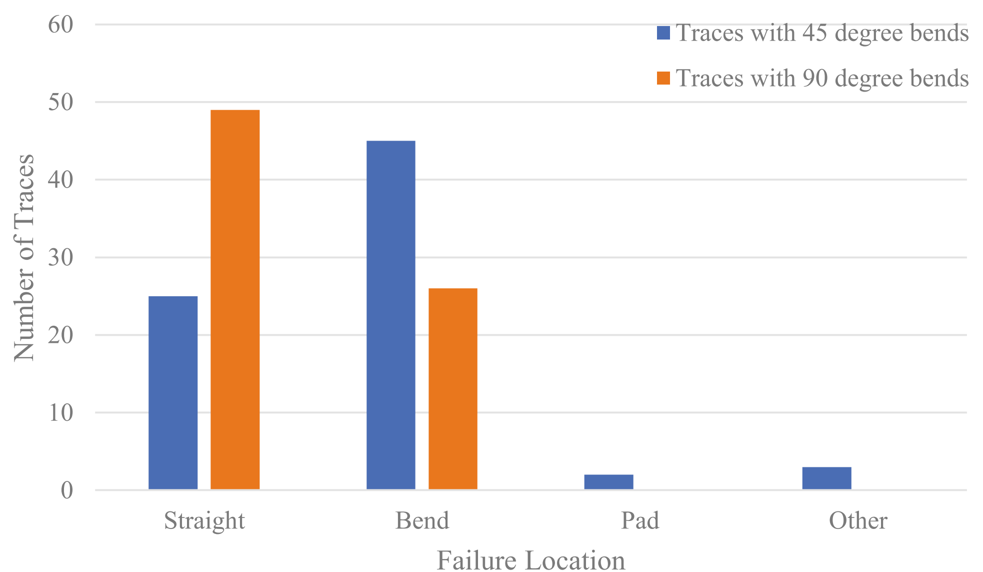

Fig. 4 Histogram of Failure Locations for Traces with Bends

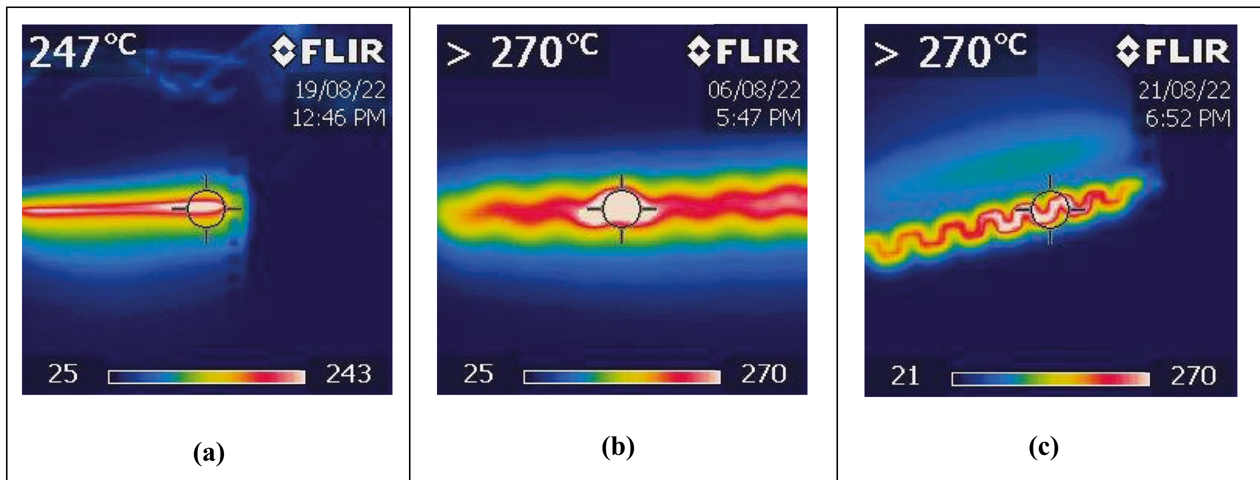

Fig. 5 Thermal Images of Traces Shortly Before Failure **a** Straight traces, **b** Traces with 45° bends, and **c** Traces with 90° bends

Table 4 Summary Statistics for Time to Failure

	Straight Traces	Traces with 45° bends	Traces with 90° bends
Number of samples	15	15	15
Mean time to failure	175.0 s	23.0 s	23.1 s
Median time to failure	160.0 s	23.0 s	19.0 s
Standard deviation	102.0 s	3.1 s	11.3 s
Minimum time to failure	42.0 s	18.0 s	11.0 s
Maximum time to failure	373.0 s	29.0 s	40.0 s

straight traces were significantly more variable than those for traces with bends, as indicated by a larger standard deviation. However, the minimum measured time to failure for straight traces was 42 s, and this is greater than the maximum measured time to failure for traces with bends of 40 s, so it is clear that straight traces always take longer to fail.

5 Conclusion and Further Work

The results did not demonstrate a large difference between the maximum currents that can be withstood by straight traces, traces with 45° bends and traces with 90° bends. This is encouraging from a PCB design perspective because it implies one of the historical reasons not to use 90° bends (i.e. they may be over-etched during manufacture leading to reduced reliability and other issues) may no longer be true in the context of modern manufacturing processes.

Some of the interesting results are that traces with 45° bends are significantly more likely to fail at the location of a bend than traces with 90° bends, and straight traces take much longer to fail on average than traces with bends for a given test current.

With regards to future work, more data can be collected and analysed, corresponding to different PCB manufacturers, internal as well as external traces, bend angles other than 45° and 90°, and different trace widths and thicknesses. It is certainly important to run corresponding tests on PCBs from other manufacturers who may be using different manufacturing techniques and tolerances.

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Data Availability The raw data for this study is not currently available on a public server, but can be made available to interested parties.

Declarations

Conflicts of Interests The authors have no relevant financial or non-financial interests, including conflicts of interests, to disclose.

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