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Refined Self-calibration of an Inductorless Low-noise Amplifier with Non-intrusive Circuit

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Abstract
Alternate test can dramatically reduce the cost of circuit testing. In one type of alternate test, copies of parts of the circuit and process-control monitors (PCM) are used as non-intrusive sensors for calibration algorithms, which can be time-consuming. A straightforward design procedure for process-aware sensors is proposed and proved efficient, and calibration results with process-aware sensors of different sizes are compared. Device size variation and process variation were found to have an impact on the mapping accuracy of the model. In addition, the results were found to degrade with a decrease in sensor size. Specifically, the low-noise amplifier (LNA) pass ratios with the largest sensor size were 3% ~ 4.5% less than the ratios obtained without the prediction error of alternate test. When the size of sensors was reduced by up to 30 times, the LNA pass ratio dropped by 5% ~ 7%.

Keywords Alternate test · Inductorless low-noise amplifier · Non-intrusive sensors · Neural network · Self-calibration

1 Introduction

CMOS has been a promising process for Radio Frequency (RF) [9, 26] or even millimeter-wave frequency circuits in the past two decades. Integrating RF, analog, and digital parts of a radio system on one chip can reduce the system cost. With the reduction of device size, the percentage of process variation becomes more significant, and the yield of digital chips decreases [1, 17, 23, 25]. Considering that RF and mm-wave circuits tend to be designed at the minimum channel length allowed by a process to ensure a cost-saving and performance-optimal solution, the corresponding performance deviation due to process variation will also lead to severe yield loss.

The performance deviation induced by scaled-down dimensions can be canceled by retracting the scaling. However, this means relinquishing the bonus brought by advanced technology and bearing the increasing production cost. Hence, scaling down device size and compensating for yield loss through calibration seems the only reasonable way to adapt to the developing CMOS technology.

The calibration of RF/millimeter-wave circuits is relatively expensive. Testing the analog portion of a chip can account for half of the total test cost, despite its less than 5% occupation of the chip area [27]. Considering the much more expensive testing apparatus and more complicated testing procedures, the corresponding verification cost for the RF or mm-wave portion will be significantly higher.

About two to three decades ago, the idea of fault-based testing was borrowed from digital circuit testing, and simple fault-based alternate tests replaced the functional tests for analog and mixed-signal circuit testing. These new methods include static DC testing, steady-state frequency domain testing, and time domain transient testing [30]. Several calibration methods based on alternate test adopt statistical analysis. These methods fall into two categories: iterative and one-shot. Compared with iterative testing, the one-shot method only needs one batch of testing [22]. Consequently, the method investigated in this paper is one-shot.

A chip with a self-calibration system can compensate for performance deviations, saving the cost of advanced automatic testing apparatuses. Nevertheless, on-chip resources are usually not sufficient for measuring diversified performance parameters. Alternate test is to build the mapping model between low-cost indirect measurements (IMs) and

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circuit performance and then predict the circuit performance rather than measuring them [20]. Therefore, the circuits and test signals needed for performance measurement can be significantly simplified.

Circuit designers are usually reluctant to have sensitive signal paths, like the output of a low-noise amplifier (LNA), tapped into for useful information extraction since this tapping results in some performance reduction that needs to be accounted for during the design [14]. In a non-intrusive self-calibration system [7], customized non-intrusive sensors are measured to obtain a set of IMs, and the interference to functional circuits is minimized. Based on the above discussions, the non-intrusive self-calibration method based on alternate test is studied in this paper.

Thus far, previous studies have improved the effectiveness of calibration based on alternate test [2–7, 10–16, 18, 20, 21]. Four IM selection strategies are compared by evaluating model accuracy [20]. However, the study is based on given sets of IMs, and how these sets are generated is left undiscussed. In [7], the correlation between circuit performance and design parameters instead of process parameters is analyzed. Furthermore, in [10], the correlation between process parameters and circuit performance is analyzed by the so-called Brownian distance correlation-directed search. Both methods reduced the workload of the analysis to some extent, but sensitivity analysis is still needed. Process-aware sensors were designed based on the correlation analysis, but specific design procedures were not given [7, 10]. Consequently, getting appropriate sensors and IMs may require some attempts.

Previous studies of the method have dealt with the construction of process-aware sensors and the generation of IMs. However, there has been no detailed investigation of the model of alternate test. Consequently, there is a lack of specific procedures for designing the sensors or analyzing the factors affecting the mapping accuracy of the model quantitatively. This paper presents a design procedure for process-aware sensors. In addition, the study of the link between IMs and circuit performance offers vital insights into the source of mapping accuracy deterioration and highlights the trade-off between the calibration results and chip area.

Nowadays, transceivers in newly flourishing applications like drones and intelligent robots are required to support different wireless standards. Consequently, receivers that support multiple frequency bands are desirable. Compared with a bunch of narrowband front-ends, using a single wideband front-end in a receiver can lead to a cost-saving system [24]. With the reduction of parasitic capacitances of the MOSFET, inductors for the capacitance resonating are no longer indispensable. In the past decade, inductorless LNAs in advanced CMOS technologies can achieve bandwidths of several GHz [24]. The inductor brings the drawback of large area consumption, which will not be improved by the progress of CMOS technology. Meanwhile, the inductor-induced parasitic devices will complicate circuit design. Hence, the wideband front end based on inductorless LNAs will be a better solution for those novel applications. Another benefit of applying the inductorless LNA is that the process-aware sensor for inductors [14] is saved.

Our previous work designed a non-intrusive self-calibration system for an inductorless low-noise amplifier [31]. Based on the previous research, this paper conducts an in-depth study on the model of alternate test.

The rest of the paper is structured as follows. Section 2 will introduce the model of alternate test. The proposed method will be described in Section 3. The trade-off in sensor size and calibration results will be discussed in Section 4. Details of the verification experiments are described in Section 5. Simulation results are analyzed in Section 6. The conclusions of this paper are given in Section 7.

2 The Model of Alternate Test

The investigated model for alternate test is stated in [7], and it is restated here for the convenience of explanation. After the circuit is designed, the performance parameters $\mathbf{p}$ depend on process parameters $\mathbf{p_r}$ and tuning knobs $\mathbf{tk}$ with a function f, as shown in (1). The tuning knobs are adjustable parts added to the circuit for performance improvement. Bold lower-case letters denote vectors in this paper.

$$\mathbf{p} = f\left(\mathbf{p_r}, \mathbf{tk}\right) \tag{1}$$

Since it is difficult to measure the process parameters directly, some electrical quantities, namely IMs influenced by the same process parameters, are measured to offer an ‘image’

$$\mathbf{m} \approx g\left(\mathbf{p_r}\right) \tag{2}$$

where the approximation accounts for the fact that measurements may not reflect all process parameters.

Substituting (1) into (2) gives

$$\begin{aligned} \mathbf{p} &\approx f\left(g^{-1}(\mathbf{m}), \mathbf{tk}\right) \\ &\approx f_z(\mathbf{m}, \mathbf{tk}) \end{aligned} \tag{3}$$

Therefore, the circuit performance is a function of IMs and knob settings. However, this expression is so difficult to be expressed analytically that a neural network is trained to fit it. A trained neural network can predict the circuit's performance, and the appropriate knob settings can be selected based on the predictions. Consequently, the calibration of the circuit is realized.

Figure 1 shows the implementation of the calibration system, which is very similar to that in [7]. The calibration system consists of process-aware sensors and the circuit to

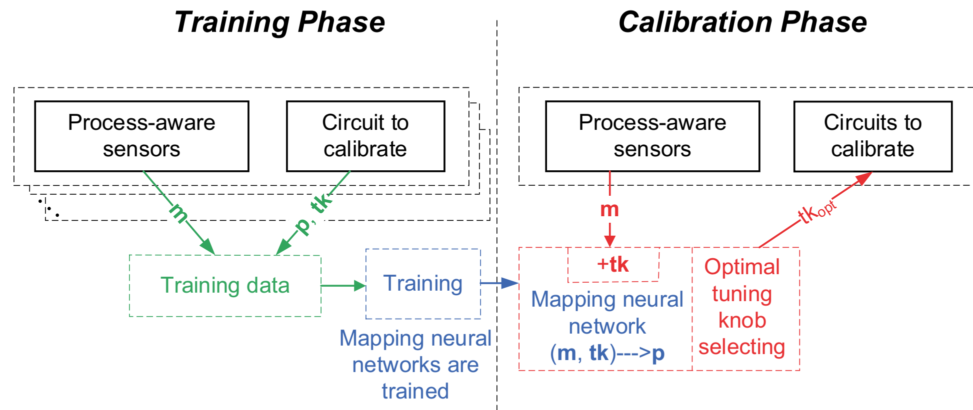


Fig. 1 The implementation of non-intrusive self-calibration systems

calibrate. The sensors are located close to the circuit. Thus, similar process parameters will influence them. The IMs **m** are generated by measuring the sensors. The data needed for network training are generated through Monte Carlo simulations. The IMs **m** and knob settings **tk** of the training data form the input of the network, and the circuit performance **p** is used as the training target. The implementation of the method is divided into two phases: the training and the calibration phase. The network to fit the expression in (3) is trained in the training phase. In the calibration phase, the IMs and different knob settings are combined and fed to the trained network. According to the predictions of the network, the optimal knob setting can be selected, and the circuit is adjusted accordingly.

3 Sensor Design Procedure

There are many kinds of circuits, each with its characteristics. The sensor design procedure proposed in this paper aims to calibrate CMOS inductorless low-noise amplifiers.

The critical parameters of a low-noise amplifier include noise figure (NF), input impedance, gain, and linearity. The gain depends on the transistor transconductance, the drain-source conductance, and the resistance of resistors. When the frequency is high, capacitors in the circuit and parasitic capacitors will also affect it. The noise figure depends on the noise gain and strength, while the noise of a resistor depends on its resistance, and the thermal noise and flicker noise of a transistor depends on its size and bias condition [29]. The input impedance also depends on the transistor transconductance, the drain-source conductance, and the resistance of resistors.

Therefore, we can infer those critical parameters when we know the transistor transconductance, drain-source conductance, and resistance of resistors. It is worth noting that the NF, the gain, and the input impedance can all be analyzed by small-signal models.

The current of a transistor is determined by its terminal voltages after its size is set [29]. Conversely, its model can be inferred when a transistor's current and terminal voltages are known. Therefore, when a transistor cascades devices of different types in series, the model of the transistor can be inferred through its terminal voltages. It is worth mentioning that when two devices of different types are connected in series with their sizes set, there is a one-to-one mapping between the voltage at the connection point of those devices and the current flowing through them. After the process parameters of the transistor are obtained, the transconductance and channel transconductance of the transistor can be known by combining its terminal voltages. Thus, there is a mapping between the transconductance, drain-source conductance of the transistors, and their bias condition.

Consequently, the sensor only needs to provide the terminal voltages of the transistors. The simplest way is to copy the circuit to calibrate and remove the components that do not affect the bias state of the transistor.

Similarly, the current of a resistor is determined by its terminal voltages after its size is set. When a resistor's current and terminal voltages are known, the model of the resistor, that is, the process parameters of the resistor can be inferred. When a resistor is connected in series with a device of a different type, there is a one-to-one mapping between its terminal voltages and process parameters.

Since capacitors affect the operation of the circuit only above a specific frequency range, considering the measuring circuits needed for capacitance measuring, the sensing of the capacitor-related process parameter is taken as an option to reduce the cost. Like resistors, the process parameters of a capacitor can be inferred from its capacitance when its size is set.

Based on these conclusions, we propose the procedure for constructing process-aware sensors and the method of selecting IMs:

1. Copy the core part of the circuit to calibrate (excluding the part providing biasing voltages).

2. If there is any capacitor, remove it. Consequently, the branch containing the capacitor is disconnected.
3. If a resistor in the circuit does not carry bias current, remove it and short both terminals.
4. If the sensor obtained after the above steps does not contain a resistor, add a resistor of the same type or select a resistor of the same type nearby as the resistor-related process sensor.
5. If any capacitor is deleted in the second step, add a capacitor of the same type as the capacitor-related process sensor.
6. If one of the constructed sensors or any part of the sensors belongs to the structure of two devices of the same type cascaded, one of the devices must be replaced by a device of a different type.
7. A dummy capacitor is measured to provide information about capacitor-related process parameters. Comparative experiments are done to evaluate the measurement's influence on the calibration results to decide whether to retain the dummy capacitor in the final calibration system.
8. Applying sensors with different sizes in multiple groups of designs and comparing the calibration results, the design that meets the requirements and has the lowest cost is selected.

It should be noted that the ground and power supply do not need to be selected as IM since they will not be perturbed by process variation.

Next, the factors that impact the mapping accuracy of the model are investigated.

4 Trade-off in Sensor Size and Calibration Results

To distinguish quantities in different parts, "non" is added as a subscript to the quantities related to the non-intrusive process-aware sensors, and "cir" is added as a subscript to the quantities related to the circuit to calibrate.

$$\mathbf{p} = f\left(\mathbf{p}_{\mathbf{r},\mathbf{cir}}, \mathbf{s}_{\mathbf{cir}}, \mathbf{tk}\right) \tag{4}$$

where $\mathbf{p}_{\mathbf{r},\mathbf{cir}}$ is a vector of process parameters influencing the circuit to calibrate.$\mathbf{s}_{\mathbf{cir}}$ is the vector of device sizes of the circuit to calibrate.

In practice, the circuit's process parameters and device sizes will fluctuate. We use $\mathbf{\Delta p}_{\mathbf{r},\mathbf{cir}}$ and $\mathbf{\Delta s}_{\mathbf{cir}}$ to represent the fluctuation, respectively.

$$\mathbf{p} = f_1\left(\mathbf{p}_{\mathbf{r},\mathbf{cir}} + \mathbf{\Delta p}_{\mathbf{r},\mathbf{cir}}, \mathbf{s}_{\mathbf{cir}} + \mathbf{\Delta s}_{\mathbf{cir}}, \mathbf{tk}\right) \tag{5}$$

Similarly, the factors affecting the sensor are divided.

$$\mathbf{m} = f_2\left(\mathbf{p}_{\mathbf{r},\mathbf{non}} + \Delta\mathbf{p}_{\mathbf{r},\mathbf{non}}, \mathbf{s}_{\mathbf{non}} + \mathbf{\Delta s}_{\mathbf{non}}\right) \tag{6}$$

(6) can be rewritten as

$$\mathbf{p}_{\mathbf{r},\mathbf{non}} = f_3\left(\mathbf{m}, \Delta\mathbf{p}_{\mathbf{r},\mathbf{non}}, \mathbf{s}_{\mathbf{non}} + \Delta\mathbf{s}_{\mathbf{non}}\right) \tag{7}$$

Assumes that the sensor and the circuit to calibrate are subjected to the same process variation,$\mathbf{p}_{\mathbf{r},\mathbf{cir}} = \mathbf{p}_{\mathbf{r},\mathbf{non}}$. Substituting (7) into (5) gives

$$\mathbf{p} = f_1\left(f_3\left(\mathbf{m}, \Delta\mathbf{p}_{\mathbf{r},\mathbf{non}}, \mathbf{s}_{\mathbf{non}} + \Delta\mathbf{s}_{\mathbf{non}}\right) + \Delta\mathbf{p}_{\mathbf{r},\mathbf{cir}}, \mathbf{s}_{\mathbf{cir}} + \Delta\mathbf{s}_{\mathbf{cir}}, \mathbf{tk}\right) \tag{8}$$

or, after removing fixed value, i.e. $\mathbf{s}_{\mathbf{non}}$ and $\mathbf{s}_{\mathbf{cir}}$, and taking out of f_1 the error terms:

$$\mathbf{p}_{\mathbf{cir}} \approx f_4(\mathbf{m}, \mathbf{tk}) + a \tag{9}$$

where $a = f_5\left(\Delta\mathbf{p}_{\mathbf{r},\mathbf{non}}, \Delta\mathbf{p}_{\mathbf{r},\mathbf{cir}}, \Delta\mathbf{s}_{\mathbf{non}}, \Delta\mathbf{s}_{\mathbf{cir}}\right)$.

The process variation and the device size fluctuations have brought deviations to the mapping in (3). In addition, those perturbations cannot be foreseen by the network.

As the sensor size decreases, this deviation will increase. There are two reasons for this. The first reason is that when the size of the sensor is reduced, its size is more susceptible to lithography inaccuracy. The trained network cannot sense this fluctuation, so the measurements cannot be mapped as correctly. Assume that the mapping between the measurements and circuit performance consists of three sub-mappings: mapping between the measurements and the sensor process parameters, mapping between sensor process parameters and the circuit process parameters, and mapping between the circuit parameters and the circuit performance. Here, the tuning knob setting is ignored for simplification. The second reason is that the reduction of the sensor size will enlarge the difference between the process condition of the sensor and the circuit. This is mainly due to random dopant fluctuation [28]. This phenomenon describes the random fluctuation of the number of dopant atoms in the MOSFET channel, which leads to the fluctuation of the main parameters of a transistor, such as the threshold voltage, subthreshold swing, drain current, and subthreshold leakage current. Even adjacent transistors will have different process parameters because of this effect. And this fluctuation is more severe in small-sized transistors, just as the short channel length is more susceptible to lithography inaccuracy.

When the sensor size is reduced, on the one hand, it is more difficult for the network to capture the sensor's process parameters; on the other hand, the difference between the process condition of the sensor and the circuit will become more prominent. Therefore, the size reduction makes the performance prediction less accurate in two ways. Consequently, there is a trade-off between the sensor size and the calibration result.

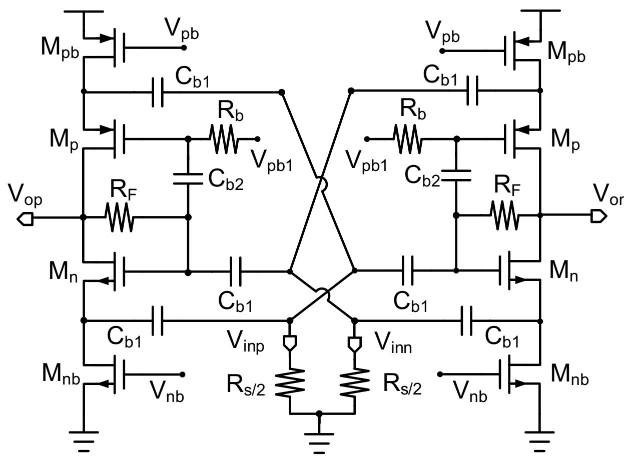


Fig. 2 The wideband inductorless low-power LNA with g_m enhancement and noise-cancellation

5 A Non-intrusive Self-calibration System for an Inductorless LNA

A non-intrusive self-calibration system for an inductorless LNA was designed to verify the method proposed in Section 3. The inductorless LNA under calibration is shown in Fig. 2 [24]. The cross-coupled push–pull and cascade structures are used for g_m and gain enhancements, respectively. Partial noise cancellation is realized through feedback from the output of one branch to the input of the other branch [24].

The amplifier consists of transistors, capacitors, and resistors. According to the design procedures proposed above, R_F and R_b in Fig. 2 are deleted since they carry no bias current. In addition, a resistor R_{bias} in the bias circuit is selected as the dummy resistor, as shown in Fig. 3. The bias resistor R_{bias} is located not far from the feedback resistor R_F. R_{bias} and R_F are of the same type, but their sizes are different. Using R_{bias} as the process-aware sensor can save chip area at the expense of more difference between the process parameters of the sensor and the circuit. After shorting both terminals of every resistor and deleting the resistors and capacitors in Fig. 2, sensor B is obtained. One end of the dummy capacitor added is grounded and the capacitor is not shown here. The IMs are marked with green words, as shown in Fig. 3. Subscript $M1$ denotes the input transistors and $M2$ denotes the current source transistors, and subscript $Di, (i = 1, 2, 3, 4)$ is used to distinguish drain voltages of different transistors. Ten voltages are chosen as IMs, including nine MOSFET terminal voltages and the voltage across the bias resistor expressed as $\mathbf{v} = [V_{M1,D1}, V_{M1,D2}, V_{M2,D1}, V_{M2,D2}, V_{M2,D3}, V_{M2,D4}, V_{M1,G1}, V_{M2,G1}, V_{M2,G2}, V_R]$. The capacitance of the Dummy capacitor is another IM.

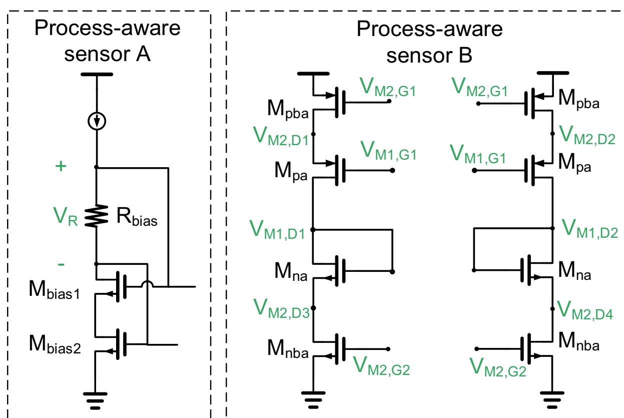


Fig. 3 The non-intrusive process-aware sensors

Nine kinds of experiments have been designed, which are marked with "ideal", "ref", "1", "1/2", "1/3", "1/6", "1/15", "1/30", and "before" respectively. In the experiments marked with "ideal", the knob settings meeting the requirements are selected by comparing the simulated performance parameters under different knob settings. Hence, the calibration is free of prediction error and yields the best result. In experiments marked with "1", "1/2", "1/3", "1/6", "1/15", "1/30", and "ref", the predicted performance is used for knob setting selection. In the experiments marked with "ref", the IMs are taken from the circuit to calibrate. Consequently, the predictions are not influenced by the device size variations in the sensors or the difference between the process parameters, which means $\mathbf{\delta s}_{non} = 0$, $\mathbf{\delta p_r} = 0$ in (26). Thus, the prediction deviation $\Delta\left(\mathbf{\delta s}_{non}, \mathbf{\delta s}_{cir}, \mathbf{\delta p_r}\right)$ is significantly reduced, leading to a minor standard deviation of prediction error. "1", "1/2", "1/3", "1/6", "1/15", and "1/30" denote six scaling factors. For example, in the experiments marked with "1", the size of sensor B is the same as the circuit to calibrate, while in the experiment marked with "1/2", the size of sensor B is only half the circuit. The size of sensor A is left unchanged as taking R_{bias} as the process-aware sensor does not increase the die area. In the experiments marked with "before", the circuits are left uncalibrated. The sizes of the devices in the sensors of different scaling factors are summarized in Table 1. The dummy capacitor is a copy of C_{b1} in Fig. 2. The reason why dummy capacitors of different sizes are not designed is that the introduction of capacitor measuring will not significantly improve the calibration results, which can be seen from the following simulation results.

According to the performance analysis in [24], the LNA's bias current and feedback resistors are chosen as the tuning knobs for performance adjustment. There are five different sets for each tuning knob, namely (1–30%)×8.3uA, (1–15%)×8.3uA, 8.3uA, (1+15%)×8.3uA, and (1+30%)×8.3uA for the bias current, and (1–30%)×2kΩ, (1–15%)×2kΩ, 2kΩ, (1+15%)×2kΩ, and (1+30%)×2kΩ for the feedback resistor. There are 25 different sets combined.

Table 1 Device sizes in sensors of different experiments (um/um)

Scaling ratio	1	1/2	1/3	1/6	1/15	1/30
M_{na}	63/0.03	31.5/0.03	21/0.03	10. 5/0.03	4.2/0.03	2.1/0.03
M_{pa}	42/0.03	21/0.03	14/0.03	7/0.03	2.8/0.03	1.4/0.03
M_{nba}	15/0.18	7.5/0.18	5/0.18	2.5/0.18	1/0.18	0.5/0.18
M_{npa}	30/0.18	15/0.18	10/0.18	5/0.18	2/0.18	1/0.18

6 Simulation Results and Analysis

The inductorless LNA and the sensors were designed in 22 nm CMOS technology and simulated at 27℃, and temperature variations are not considered. From a technical point of view, the calibration at different temperatures can be covered by networks trained using data generated at those temperatures. However, the amount of simulation needed to obtain the required training and testing data will be tenfold or even more if the variation is covered comprehensively. Considering this paper's emphasis is method research, only the circuit performance at 27℃ is calibrated.

The network was constructed and trained using Deep Learning Toolbox in MATLAB, and the training algorithm is Levenberg–Marquardt. Three performance parameters of the inductorless LNA, namely S11, gain, and NF, are calibrated. Each circuit performance parameter is predicted by a neural network to improve the prediction accuracy. Feedforward neural networks with only one hidden layer are used [19]. Moreover, after some trial and error, the number of hidden layer neurons is set to 12.

Eighty thousand samples for network training and evaluation and 20,000 samples for calibration systems validation are generated using Monte Carlo simulation. These samples simulate the performance of 3,200 and 800 dies in 25 different knob settings under the influence of global process variation and local process variation, respectively.

The trained networks are evaluated using criteria, namely the standard deviation of prediction error, average prediction error, and figure of merit [7]. The standard deviation of prediction error $\sigma_{\varepsilon,k}$ and average prediction error $\overline{\varepsilon}_k$ are defined as

$$\sigma_{\varepsilon,k} = \sqrt{\frac{1}{S-1}\sum\nolimits_{1}^{S}\left(P_k - \hat{P}_k - \overline{\varepsilon}_k\right)^2}, (k = 1, 2, 3) \tag{10}$$

$$\overline{\varepsilon}_k = \frac{1}{S}\sum\nolimits_{1}^{N}\left(P_k - \hat{P}_k\right) \tag{11}$$

where S is the size of the data, k is used to distinguish different performance parameters to calibrate as 1 for S11, 2 for NF, 3 for gain, P_k is the simulated circuit performance, and $\hat{P}_k$ is the predicted circuit performance. The definition of the standard deviation is a little different from the usually used one since the data is processed using MATLAB inherent function *std*. However, this difference will not influence the result because S is a large number. The standard deviation of prediction error tells how accurate the prediction is, and the average prediction error reflects the offset in the predicted performance.

The figure of merit FoM is defined as [8]

$$FoM_k = \frac{\varepsilon_{RMS,k}}{\sigma_k} \tag{12}$$

$$\varepsilon_{RMS,k} = \sqrt{\frac{\sum_{j=1}^{S}\left(P_{k,j} - \hat{P}_{k,j}\right)^2}{S}} \tag{13}$$

where S is the data size, $\varepsilon_{RMS,k}$ is the root mean square deviation of the prediction error, and σ_k is the standard deviation of the simulated performance parameters.

The input of the network consists of IMs and tuning knob values. In addition, the output of the network is the prediction of the circuit performance under different tuning knob settings. The difference between the predictions and the simulation results is statistically analyzed. After the networks are proven effective, they will be used for calibration. The optimal knob settings are selected based on the network predictions. Furthermore, the calibration system can be evaluated by comparing the simulated performance corresponding to the optimal settings with those corresponding to the default knob settings, which correspond to the performance without calibrations.

There are two kinds of calibrations defined here. One is partial calibration, and the other is chip calibration. In the partial calibration, only one performance parameter is calibrated, leaving the other two unconsidered. It is to select the knob setting corresponding to the best predicted performance. In the chip calibration, the LNA is qualified when all parameters are up to some criteria in the chip calibration. It is to select the knob setting corresponding to the minimum noise figure and simultaneously meets the S11 and gain criteria. The criteria are laid down according to the LNA performance at the typical corner.

The performance parameters of the LNA at typical corner and 27℃ are shown in Table 2. Its maximum gain is 21.5 dB, achieving a 3-dB flatness from 0.2 GHz to 6 GHz. Its S11 is below -8 dB from 0.2 GHz to 3 GHz, and its NF ranges from 2.55 dB to 3 dB from 0.2 GHz to 6 GHz. It consumes 0.52mW from a 0.8 V supply.

Figures 4, 5, 6 and 7 show the average prediction errors and standard deviations of the prediction error of the neural networks at 0.2 GHz, 1 GHz, 1.3 GHz, and 1.8 GHz,

Table 2 Simulated performance of the inductorless LNA to calibrate

Technology (CMOS)	BW_{3dB} (GHz)	Gain (dB)	NF (dB)	Frequency Range For S11 < -8 dB(GHz)	Supply (V)	Power (mW)
22 nm	0.2–6	21.5	2.55–3	0.2–3	0.8	0.52

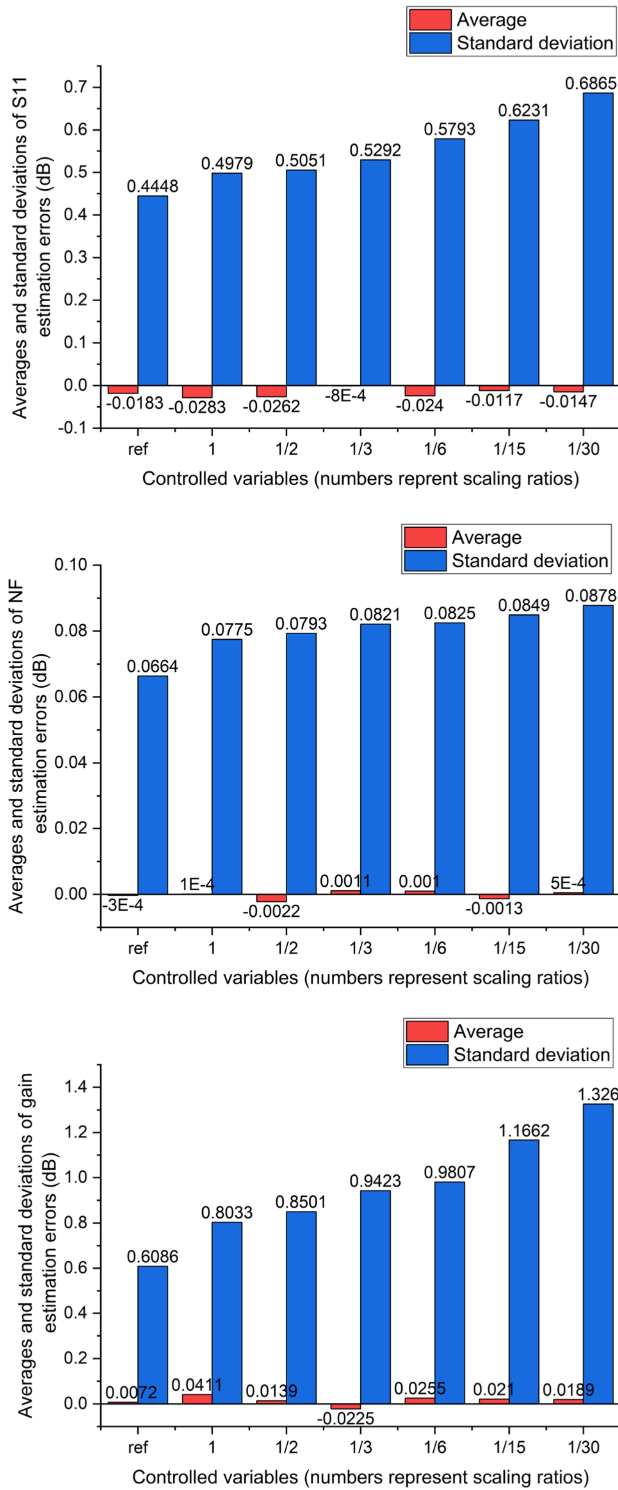


Fig. 4 The averages and standard deviations of estimation errors of S11, NF, and gain at 0.2 GHz

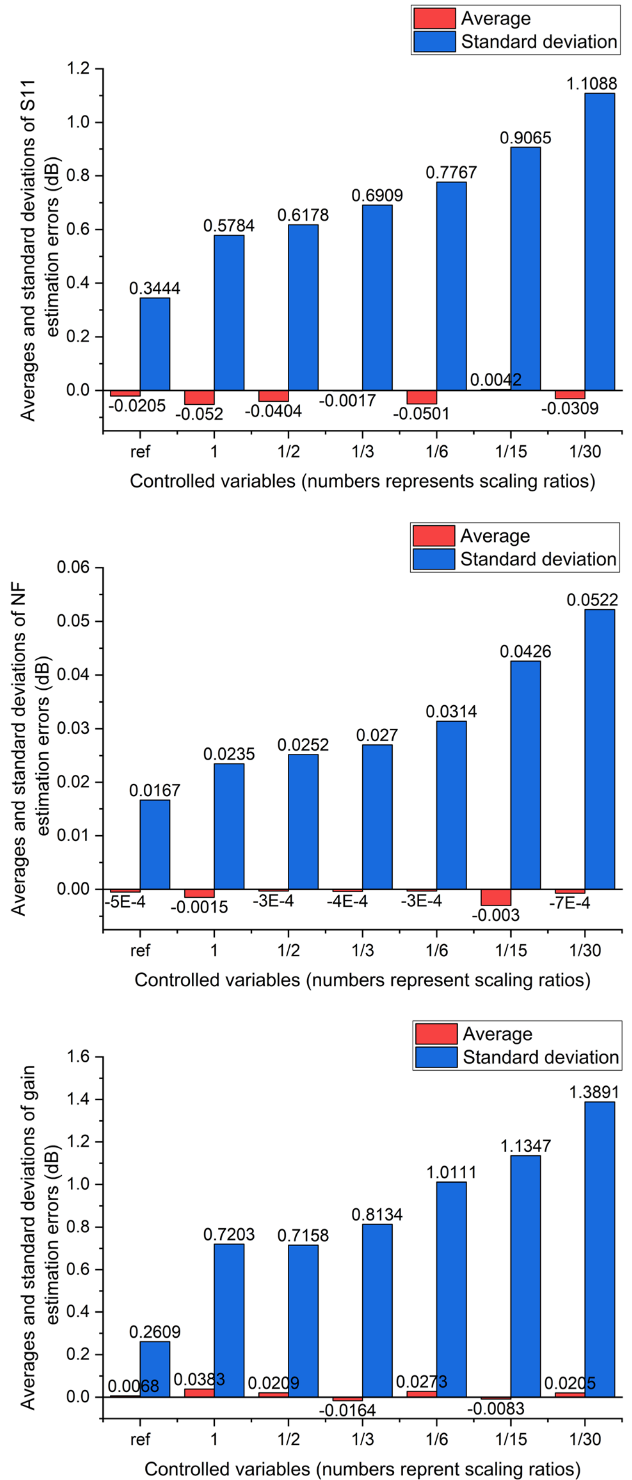
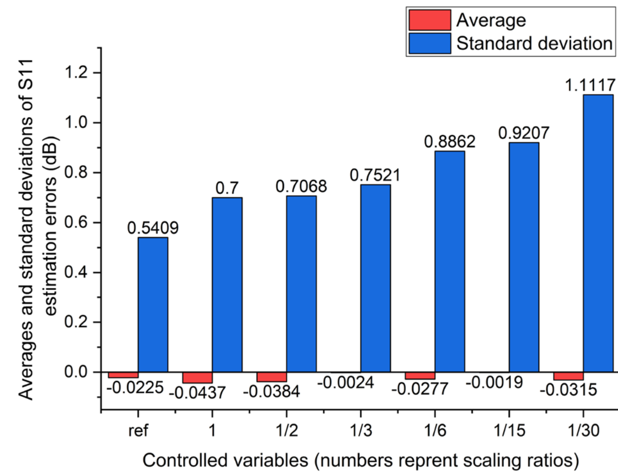
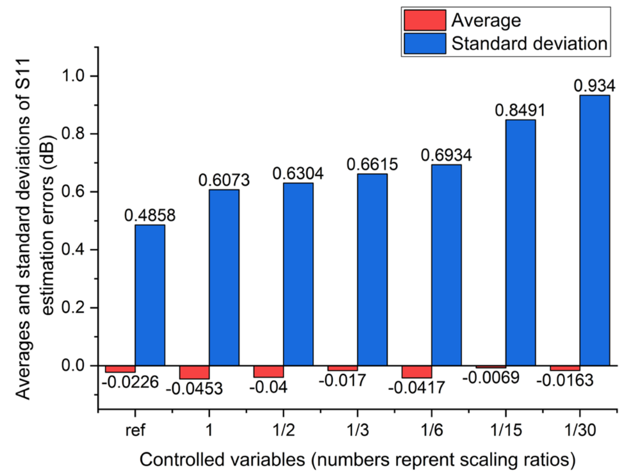
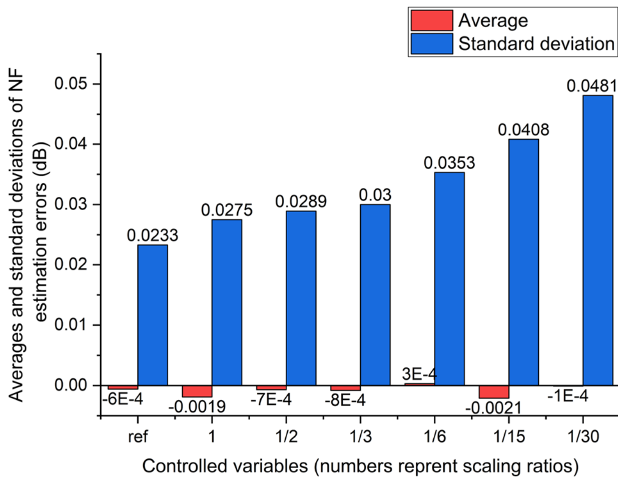
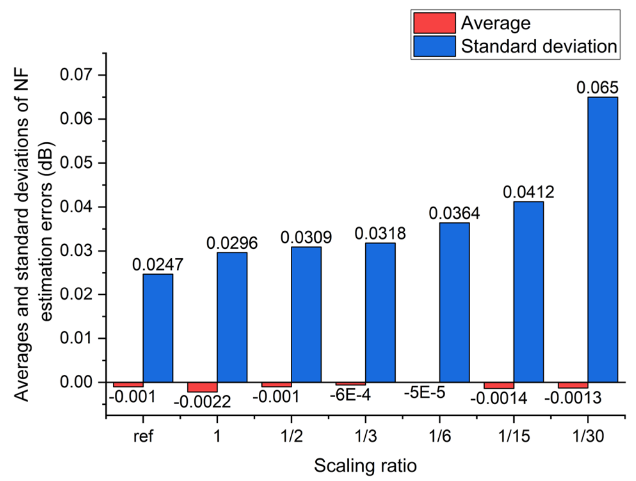


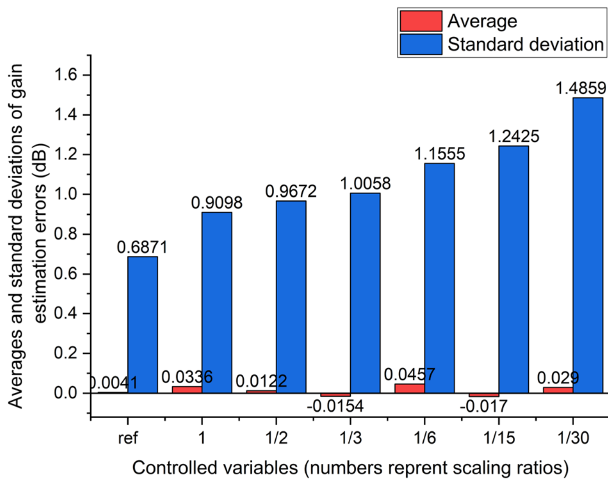
Fig. 5 The averages and standard deviations of estimation errors of S11, NF, and gain at 1.0 GHz











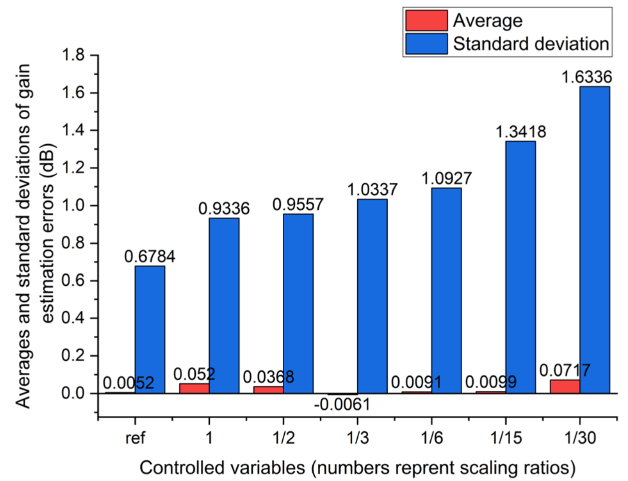


Fig. 6 The averages and standard deviations of estimation errors of S11, NF, and gain at 1.3 GHz

Fig. 7 The averages and standard deviations of estimation errors of S11, NF, and gain at 1.8 Hz

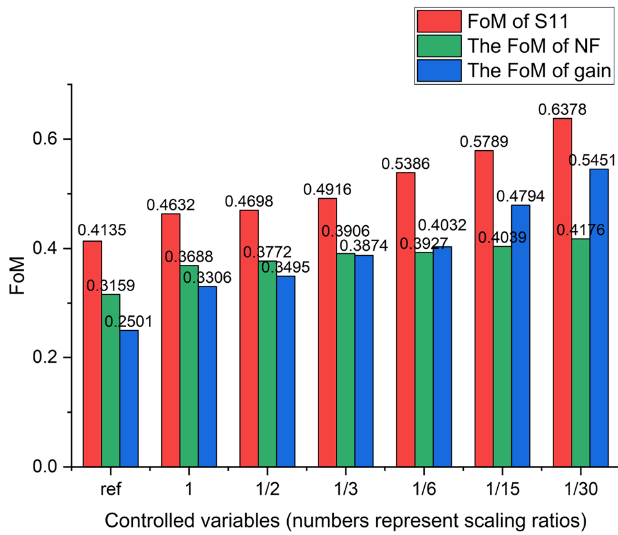


Fig. 8 The FoMs of estimation networks at 0.2 GHz

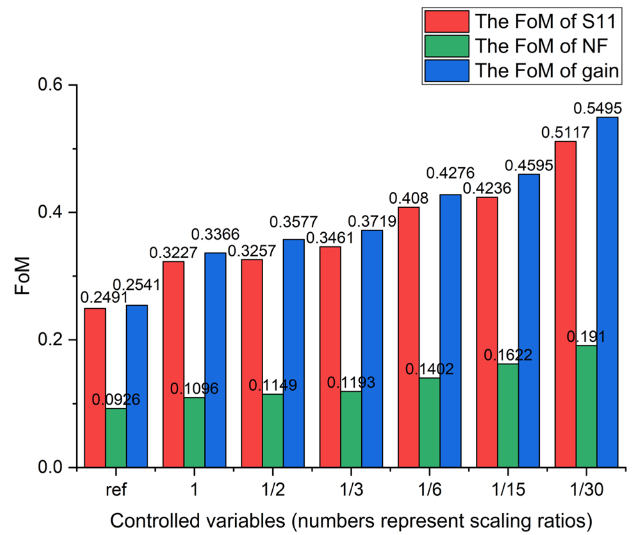


Fig. 10 The FoMs of estimation networks at 1.3 GHz

respectively. When the device sizes of the non-intrusive process-aware sensors gradually decrease, $\Delta \mathbf{s}_{\mathbf{non}}$ and $\Delta \mathbf{p}_{\mathbf{r,non}}$ increase. This increase will add to the rise of the deviation $a = f_5\left(\Delta \mathbf{p}_{\mathbf{r,non}}, \Delta \mathbf{p}_{\mathbf{r,cir}}, \Delta \mathbf{s}_{\mathbf{non}}, \Delta \mathbf{s}_{\mathbf{cir}}\right)$, increasing the standard deviation of the prediction error. As mentioned before, the results of experiments marked with "ref" are not influenced by the device fluctuations in the process-aware sensors and the difference between the process parameters. Thus, they show the best results. Meanwhile, the averages of the prediction errors do not show a similar relationship with the decreasing device sizes. However, the relatively small figures mean that the offset in the prediction is not a big problem.

Figure of Merit (FoM) considers the variation of the quantity showing the network performance comprehensively [8].

Figures 8, 9, 10 and 11 show the FoMs of neural networks in different experiments at different frequencies. An FoM below 1 is considered to be largely satisfactory [7]. The FoM increases as the scale ratio decreases. This increase reflects the prediction error increase because the standard deviation of the simulated performance is constant.

Figures 12, 13, 14 and 15 show averages of the performance parameters after the partial calibration in different experiments at different frequencies. The averages before the calibration are marked with stars. The averages are significantly improved by the partial calibration and deteriorate as the scale ratio decreases. Meanwhile, they are close to the "ideal" results, proving that our proposed design procedures are effective.

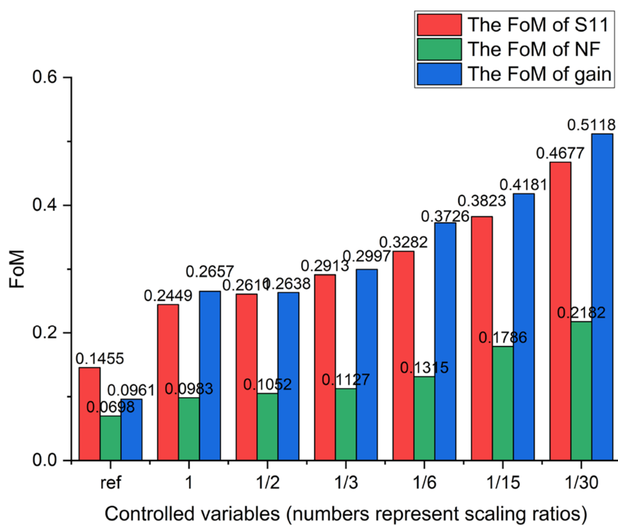


Fig. 9 The FoMs of estimation networks at 1.0 GHz

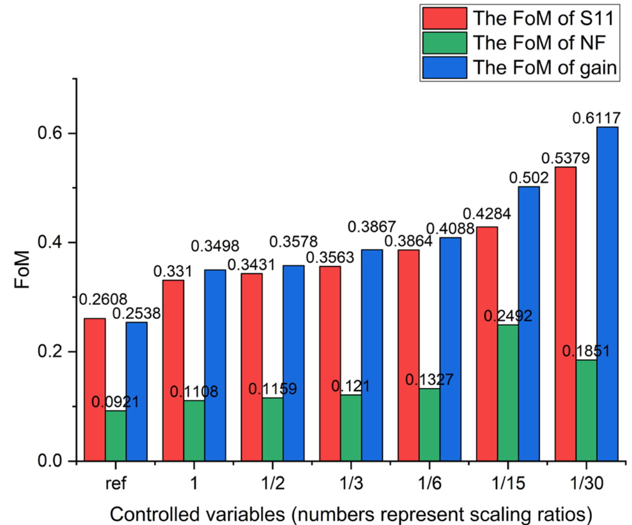


Fig. 11 The FoMs of estimation networks at 1.8 GHz

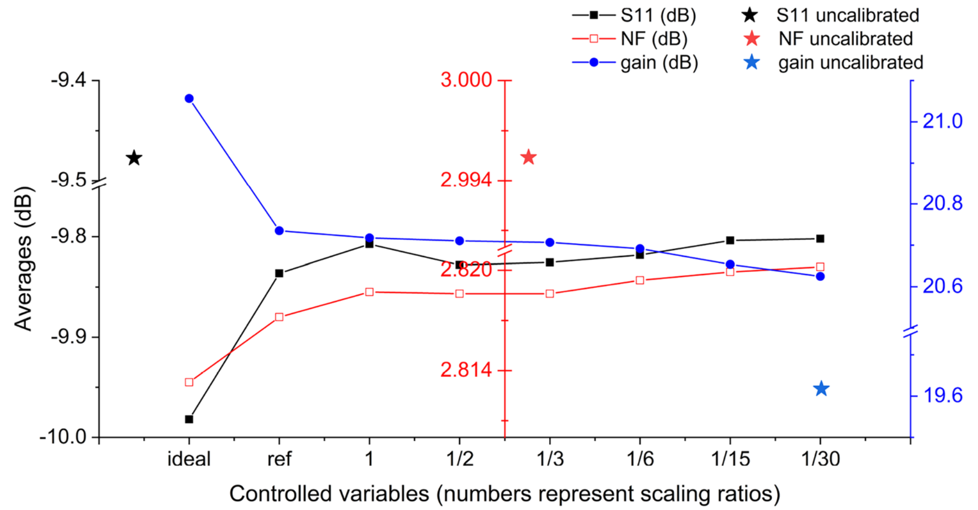


Fig. 12 The averages of performance parameters after the partial calibration at 0.2 GHz

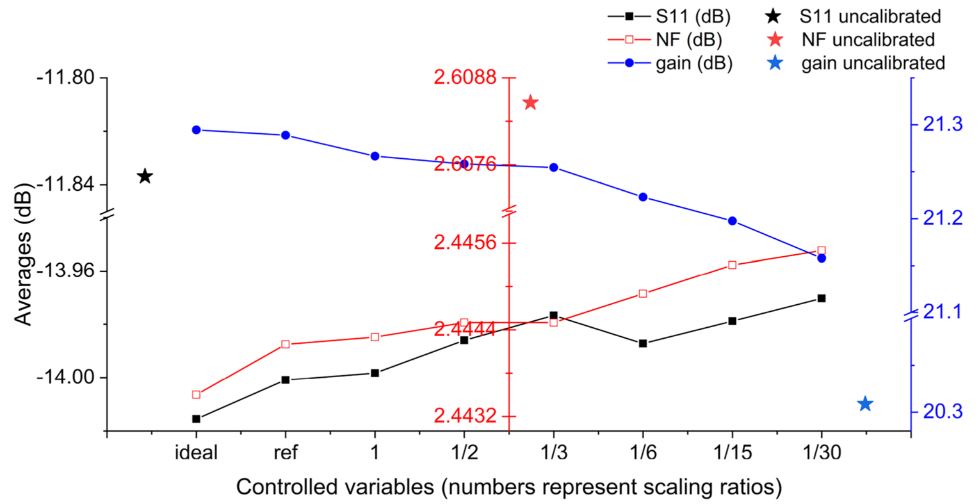


Fig. 13 The averages of performance parameters after the partial calibration at 1.0 GHz

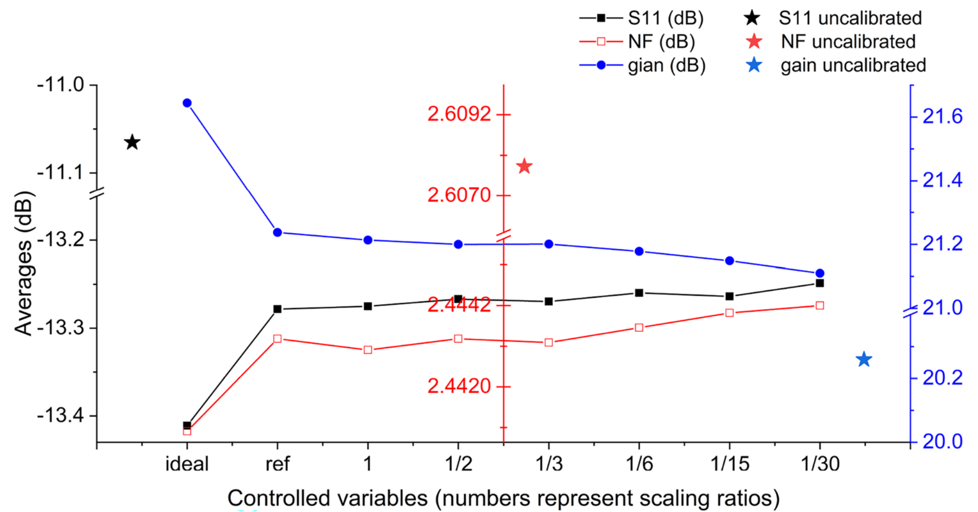


Fig. 14 The averages of performance parameters after the partial calibration at 1.3 GHz

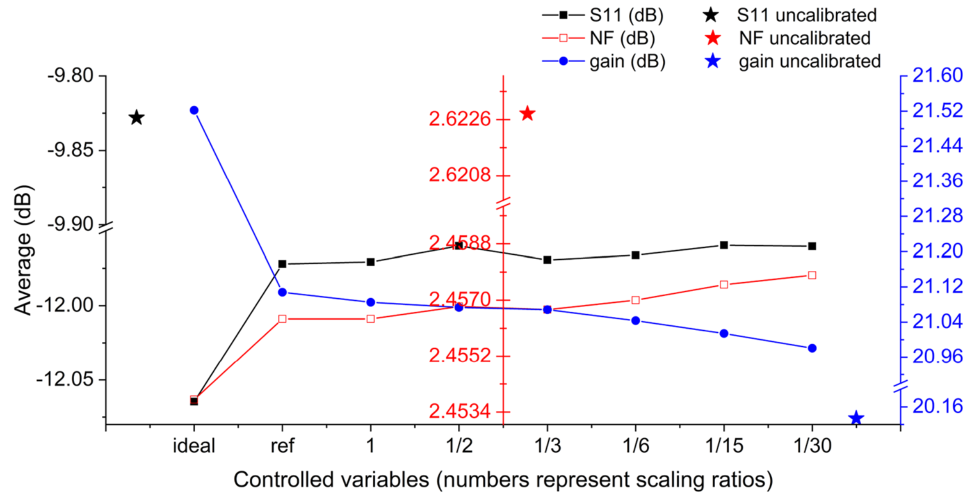


Fig. 15 The averages of performance parameters after the partial calibration at 1.8 GHz

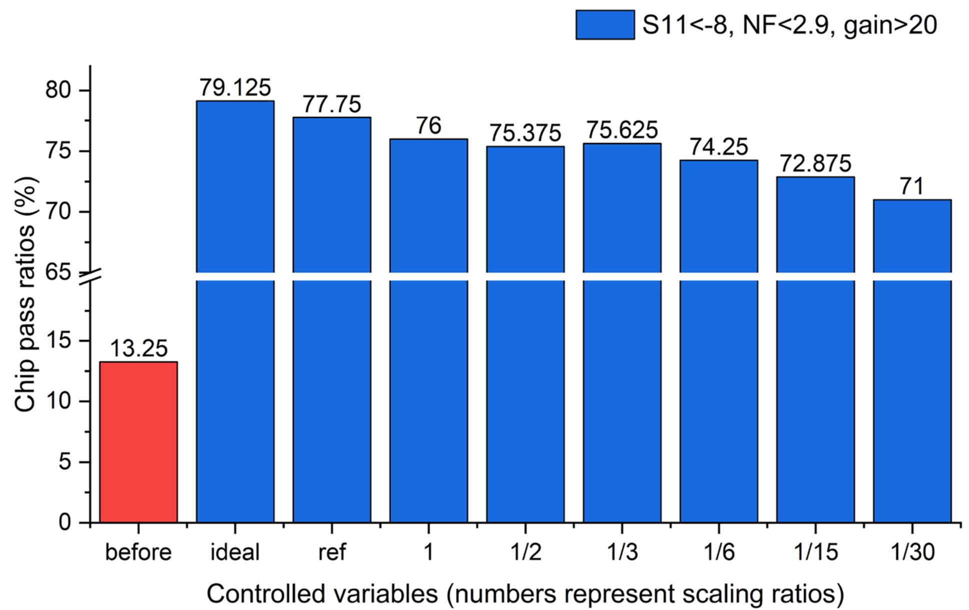


Fig. 16 LNA pass ratios after the chip calibration at 0.2 GHz

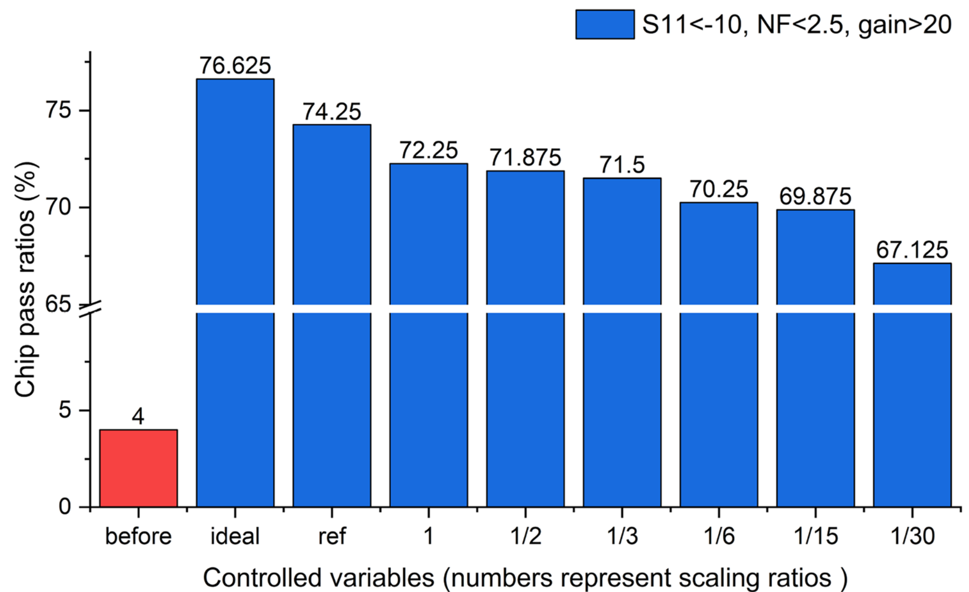


Fig. 17 LNA pass ratios after the chip calibration at 1.0 GHz

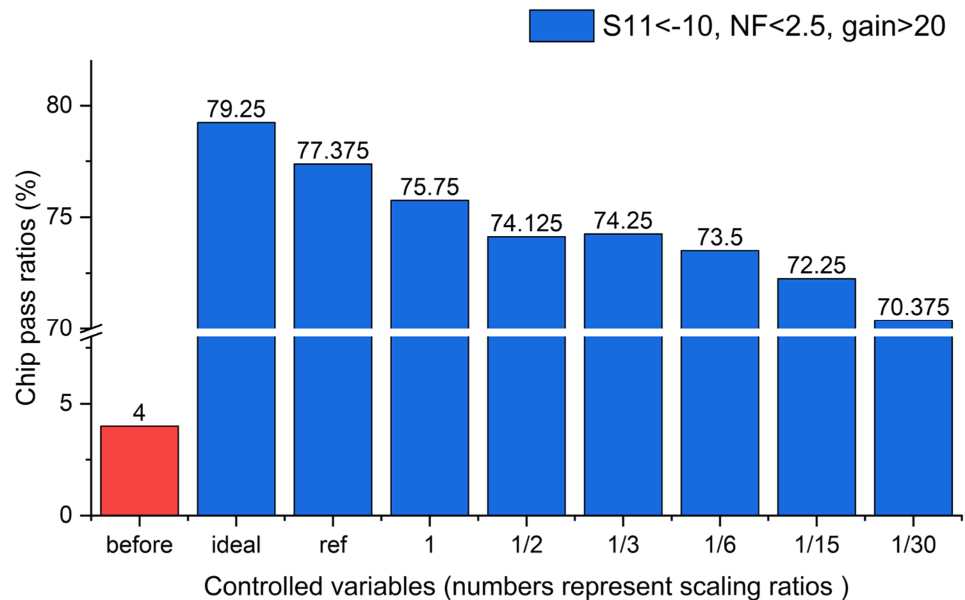


Fig. 18 LNA pass ratios after the chip calibration at 1.3 GHz

Figures 16, 17, 18 and 19 show the pass ratios before and after the chip calibration. The criteria for the performance parameters are shown in the legends. "ideal" corresponds to the best results, followed by the results corresponding to "ref". The pass ratios after the calibration decrease as the scaling ratios decrease. In Fig. 16, the pass ratio is 76% when the scaling ratio is 1. The pass ratio reduces by 5% when the scaling ratio reduces to 1/30.

Figures 17, 18 and 19 show similar situations. There is a gap of 1% to 2.5% between the chip pass ratios corresponding to "ref" and "ideal" and a gap of 3% to 4.5% between the chip pass ratios corresponding to "1" and "ideal", which proved that the sensor design procedure proposed in this paper are effective.

Figures 20 and 21 compare the calibration results at 0.2 GHz and 1.8 GHz obtained using a dummy capacitor placed near the LNA as a process-aware sensor with those obtained not using it. Although measuring the capacitor provides more information about the process parameters affecting the circuit to calibrate, the calibration results show that its influence is insignificant and ambiguous here. According to step 7 of the procedures, the dummy capacitor will be abandoned.

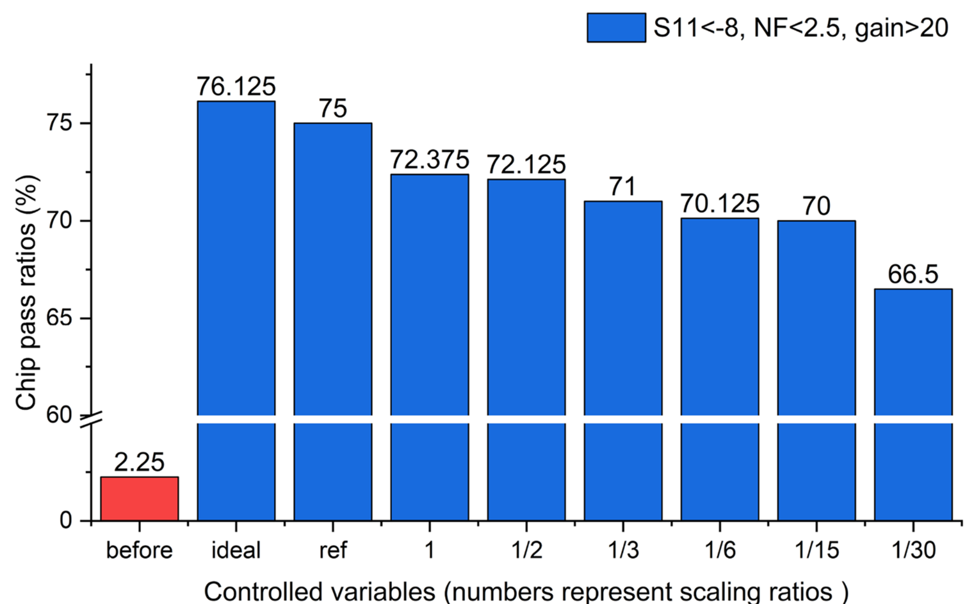


Fig. 19 LNA pass ratios after the chip calibration at 1.8 GHz

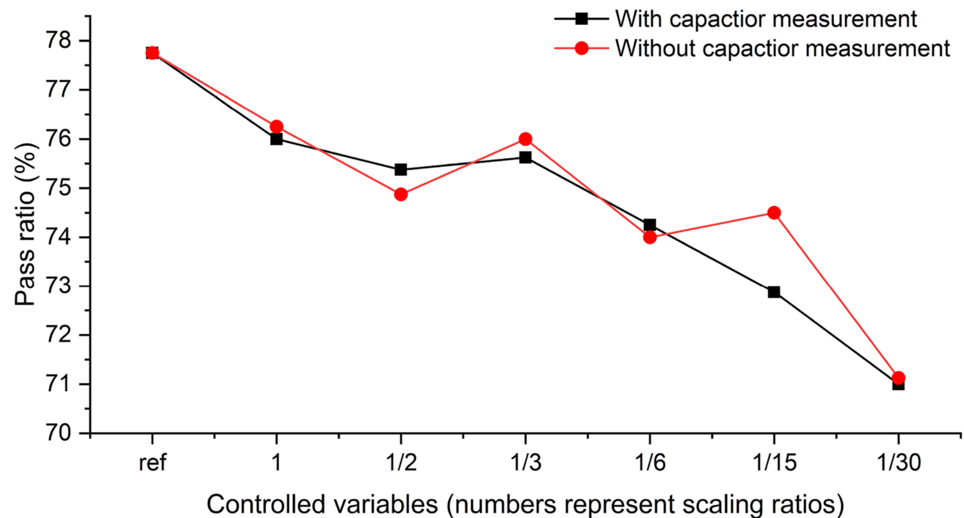


Fig. 20 The pass ratios of the LNA at 0.2 GHz with/without capacitor measurement

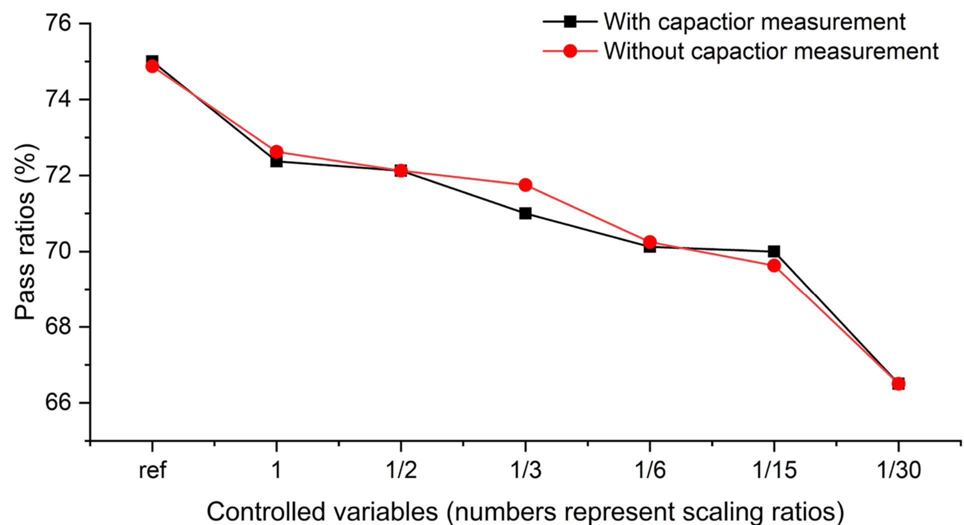


Fig. 21 The pass ratios of the LNA at 1.8 GHz with/without capacitor measurement

7 Conclusion

This study set out to investigate the model of alternate test. Results showed that the process parameters related to resistors and MOSFETs are a function of the terminal voltages. We proposed a straightforward design procedure for process-aware sensors based on these conclusions. Furthermore, this study has been the first attempt to examine factors affecting the mapping accuracy of the model. Moreover, the trade-off between the calibration results and sensor size was explored. However, this work was limited by the absence of verification for the case where capacitor behavior affects the circuit performance or the discussion of the case where inductor behavior affects the circuit performance. If we want to expand the scope of this analysis, we also need to consider the situation where the circuit performance is affected by full-custom passive components. Another obvious limitation was the lack of discussion of the layout's influence on the mismatch between the sensor and the circuit.

It is worth mentioning that the neural networks do not need much computing and storage resources. In addition, since modern transceivers are usually equipped with a certain degree of calculation capability and ADCs, the calibration system may be integrated into the object system with a low extra burden. Further research may verify this viewpoint.

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Data availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflicts of Interests The authors have no relevant financial or non-financial interests to disclose.

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