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Network-on-Chip and Photonic Network-on-Chip Basic Concepts: A Survey

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Abstract
Network-on-Chip (NoC) is one of the basic chip designs with advantages and challenges especially when the number of transistors increases and the data transfer rate across network is important. For these reasons, Photonic Network-on-Chip was proposed. These networks are important for intra chip communication. The data transfer with photonics between devices with long distance on the chip without any transfer rate loss is one of the most important advantages of Photonic Network-on-Chip. This paper reviews basic and fundamental concepts of Network-on-Chip and Photonic Network-on-Chip to understand their key points of designs and rules for implementation.

Keywords Network-on-Chip (NoC) · Photonic Network-on-Chip (PNoC) · Network topology · Architecture · Router

1 Introduction

The market demands for innovative technologies have induced a considerable evolution of integration capacities in recent platforms. In fact, semiconductor industry offers many powerful hardware chips. Downscaling of device features continues through 40 nm, 35 nm, 28 nm, and beyond. Power consumption is decreasing and GHz-range working frequencies are increasing [42, 43]. A chip with the cited advances will enlarge the intervention domain of engineers to solve many design issues. Like the hardware side of technology, the software side, which is represented by the Computer Aided Design (CAD) tools, has been dramatically innovated. This includes modeling, simulation, synthesis and implementation tools. Also, new design flows have emerged like the Co Design concept. In addition, many techniques were proposed by research community and some adopted by industry are like High Level Synthesis (HLS) or Model Based Design (MBD) [6].

As mentioned in the literature [10, 42], traditionally, a SoC is composed of some processing elements (processors, dedicated Intellectual Properties (IPs), etc.), few memory blocks and In/Out communication modules. The number of these On-Chip elements is continuously growing. Recent platforms are often Multi-Processor SoC (MPSoC) with multiple functionalities and a lot of options. For example we can cite recent personal computers, video games, smart phones and tablets. However, the growth of the On-Chip elements has provoked new issues like the communication between internal elements. In fact, classical buses could not assure a reliable connection between them. A new solution has to be found to face this problem. In 2002, the NoC paradigm was introduced by Luca Bennini and Giovanni De Micheli [7]. This proposal has resolved the intra-chip communication problem and data conversion issues.

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The NoC paradigm is important because it allowed design engineers to follow technology advancements and to integrate many cores on the same chip by overcoming the communication problems. Numerous studies have proposed NoC architectures and their enhancements.

We find relevant surveys and comparative studies in the literature on NoC proposals. Reference [9] details the NoC concept and discusses examples. Other references give detailed comparison between NoC architectures and performances or discuss the future of NoC related research [1, 2, 34]. Recent proposals are essentially based on more sophisticated architectures offering diverse advantages such as; the quality of service (QoS) [36] or globally asynchronous locally synchronous (GALS) architectures, which resolve the clocking difference problems inside an SoC [11, 33].

Technology advancements have also pushed researchers to reconsider their point of view about NoCs. Besides, some work has focused on developing 3D NoC architectures [46]. NoC tool developers have also anticipated these advancements and proposed tools dedicated to 3D NoC design and simulation [35]. However, other studies proposed a different approach by adding a bus to the NoC concept, while keeping some data transfer to classical buses. The purpose is often to reduce costs in terms of area and power consumption and of course without degrading the system performances in terms of throughput and latency [47]. Other researchers have applied the existing concepts like reconfigurability basically developed for SoCs to the Network-On-Chip. The term of ReNoCs which means Reconfigurable NoCs is mostly developed inside the research community and as a result, some initiatives were elaborated on this subject [25].

1.1 Introduction of PNoC and Related Work

Designing a vital communication infrastructure seems to be a basic inclination for incorporating multiple processing cores. As a result, a plethora of research can be found to stress the packet-switched Networks-on-Chip (NoC) design for general purpose chip multiprocessor (CMP) and application to specific systems-on-chip (SoC) [32]. Many studies have focused on the improvement of the NoC bandwidth and latency. This will affect the system application output. Yet, because packaging limitation poses strong limits on the maximum on-chip temperature in predictable future, optimization of power loss of a Network-on-chip seems to be a vital issue, especially with the growing number of cores on the chip. In fact, the restricted on-Chip power budget needs to be disseminated between computation and communication processes. Visibly, the decrease in power loss by the Network-on-Chip leads the power budget to be allocated to the cores and this in turn will fix the efficacy of the overall system [32]. Recent researches suggest data networks based on optical interconnections.

The effect of an important design model shift can be seen when vital technologies get together on substantial performance limits. Basically, the scaling in transistor speeds and integration compression cannot drive from the present homological multiples in computation output. Increasing the operating frequency of the local processors leads to more severe constraints on the chip design and associated power losses, which in turn reduces efficiency. In fact, we will witness an increase in performance within a few years in the processor cores on chip. This will result in the advent of a vital hindrance, namely, the universal intra chip communications substructure. Here, the most important step to be taken is the challenge in future systems to realize vast bandwidths and correct latency needs, especially when the number of processing cores also increases [4, 23].

To remove one of the basic hindrances in a chip multiprocessor (CMP), low latency, high data-rate, and on-chip interconnection networks are among key factors. A plethora of studies focus on intrachip global communication via packet-switched micro-networks. These present a shared medium that is pretty scalable and gives ample bandwidth to substitute common bus-based links [4, 36]. Yet, performance-per-watt is the most vital design metric for Network-on-Chip as well as chip multi processors. How NoCs are going to meet future communication bandwidths and latency needs within the power loss budget seems unclear. On the other hand, photonic interconnection networks provide a potentially factious technology resolution with low power loss and provides ultra-high throughput as well as minimal access latency. One main driver can be the expected decrease in power in intrachip communications. Without any need for repetition, the data can be transmitted end to end with a determinate photonic path and the basic power saving rises. In electronic NoCs, however messages are hindered, regenerated, and then transmitted to the inter router links [4, 36]. So, NoCs play a vital role in the intra chip multiprocessor core interconnection while larger communication bandwidth in the NoC is needed to consider the communication among processor cores with an increase in local clock frequency in CMP.

Also, the performance can be considerably high through the use of wavelength division-multiplexing method (WDM) [4, 5, 12, 21, 45]. Because waveguides are free from distance and data rate per bit, they cannot affect power consumption in waveguides and photonic switches. Various designs of photonic networks have been put forward lately and most of them show considerable improvements in comparison with their electronic counterparts [4, 27, 31]. It can be mentioned that photonic routers are key elements of Photonic Networks-on-Chips (PNoCs) and they are considered vital in case of performance and cost parameters [4, 18].

In the following parts of the paper we have reviewed fundamental NoCs and PNoCs concepts such as architectures,

topologies and layering in Sect. 2.1. In Sect. 2.2 methods of switching and routing are reviewed. In Sect. 3, PNoCchallenges and in Sect. 5 testing phase are explained and in the end concluding remarks are made.

2 NoCs and PNoCs Basic Concepts

In this part, we are going to review some fundamental concepts such as architectures, topologies and layering.

2.1 NoC Architecture

The NoCs typically consist of routers, network adapter (network interface) and connections [26, 34].

1. Router: directs the data according to the protocol selected. It contains the routing strategy [6].
2. Network Adapters: provide a bridge between the router and the element attached to them. Their main task is to separate calculation (IPs) of the communication (network). This consists of two operations which are protocol conversion and packages construction [6].
3. Connections: are the channels of transmission of data between the various circuit elements to the network [6].

2.2 NoC Topology

The topology of a network is the way in which routers, network adapters and connections are organized. There are several topologies that we can call regular or irregular [17, 41]. This classification is based on the distribution of routers in the network. Figure 1 shows some regular topologies such as, a) mesh, b) torus, c) ring, and d) fat-tree.

On the other hand, irregular topologies are composed of two or three regular topologies such as a mesh topology and ring, simultaneously [6].

In a mesh, nodes form a grid, as shown in Fig. 1(a). Expansion is easy for meshes. Little effort is needed when adding more nodes to an existing architecture. Nodes have different degrees according to their locations within the mesh. Corner nodes have degree of 2. Edge nodes have degree of 3. Inner nodes have degree of 4. Its strengths include: (1) Multiple paths between a pair of nodes and tolerance to link failure. (2) Easy to expand. Its limitations include: (1) Diameter can become too large. (2) Irregularity, less bandwidth for nodes at corners and edges [14].

A torus topology is obtained by adding direct connections to two end nodes in the same row or column of a mesh. A 16-node torus is shown in Fig. 1(b). Compared with mesh, its diameter is reduced. A regular torus has long wraparound links. By folding a torus, long wires can be avoided at the cost of doubling the wire length [14].

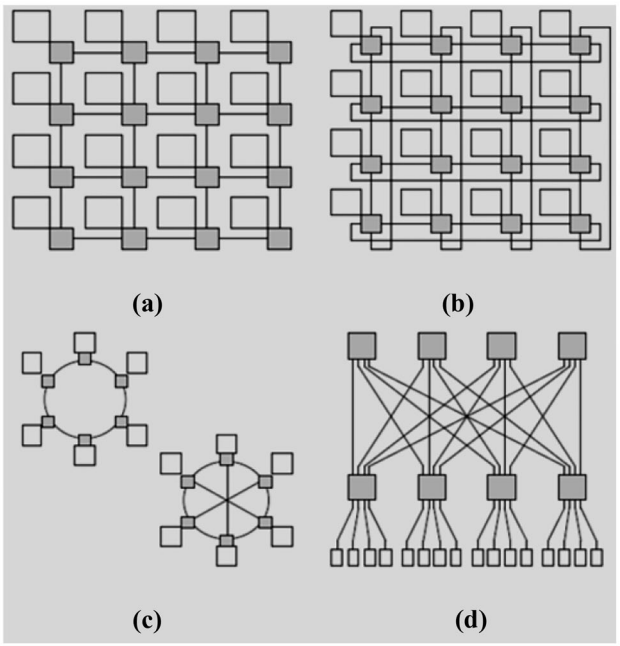

Fig. 1 Examples of regular NoC topologies [6]: **a** mesh, **b** torus, **c** ring, and **d** fat-tree

In a ring topology, all nodes are connected in a ring fashion, as shown in Fig. 1(c). Every node has two neighbors regardless of the size of the ring. Its small degree is preferable, but its diameter increases linearly with the number of nodes. Its strengths include: (1) Cable faults are easily located, which makes troubleshooting easier. (2) Moderately easy to install compared with other architectures. Its limitations include: (1) Expansion to the network can cause network disruption. (2) Even a single break in the cable can disrupt the entire network [14].

In a fat binary tree or fat-tree, only leaves are intellectual properties (IP), as shown in Fig. 1(d). Interior nodes are switches. When moving towards the root node, there are more links between a parent node and a child node. The number of inter-node links increases by order of 2 [14].

2.3 NoC Layering

The NoC function can be classified into several layers: application, transport, network, data link, and physical layers. A NoC router should contain both software and hardware implementations to support functions of the layers.

- Application Layer: At the application layer, target applications will be broken down into a set of computation and communication tasks so that the performance factors like energy and speed can be optimized. Placement of cores on a NoC has to be optimized to reduce the amount of total communication or energy but at the same time

recognizing the limitations of any one particular link. The task mapping and communication scheduling problem is an instance of a constrained quadratic assignment problem which is known as NP-hard. Given a target application described as a set of concurrent tasks with an NoC architecture, the fundamental questions to answer are (1) how to topologically place the selected set of cores onto the processing elements of the network and (2) how to take into consideration the complex effects of network condition, which may change dynamically during task execution, so that the metrics of interest are optimized. To get the best tradeoff between power and performance, application mapping and scheduling should be considered with several kinds of architecture parameters [40].

- Transport Layer: To prevent buffer overflow and to avoid traffic congestion, some management schemes should be applied to guide the transport of packets in a NoC. The transport layer addresses the congestion and flow control issues. Key performance metrics of a NoC include low packet delivery latency and high-throughput rate, and these metrics are critically impacted by network congestions caused by resource contentions. Accordingly, contention resolution is a key to avoid network congestions. One of the most crucial issues for the contention resolution is, under a premise of a deadlock- and livelock-free routing algorithm, to enhance the utilization efficiency of available network resources in order to come up with a better communication performance [40].
- Network Layer: Network topology or interconnect architecture is an important issue in this layer, which determines how the resources of network are connected, thus, refers to the static arrangement of channels and nodes in an interconnection network. Irregular forms of topologies can be derived by mixing different forms of communication architectures in a hierarchical, hybrid, or asymmetric way by clustering partition which may offer more connectivity and customizability at the cost of complexity and area. In addition, optimization of a topology which affects the connectivity of the routers and the distance of any one core to the other is difficult. Furthermore, the tradeoff between generality and customization that, respectively, facilitate scalability and performance is important. As future designs become more complex, the non-recurring costs of architecting and manufacturing a chip will become more and more expensive. A homogenous NoC is one where the cores and routers are all the same, while a heterogeneous NoC selects individual cores from an IP library and may have its communication architecture customized to suit the needs of an application. Since NoC designs must be flexible enough to cover a certain range of applications, most of the state-of-the-art NoC designs use a mesh or torus topology because of its performance benefits and high degree of scalability for two-dimensional systems, yet it may not achieve the best performance for a single application [40].
- Data Link and Physical Layers: The main purpose of data-link layer protocols is to increase the reliability of the link up to a minimum required level, under the assumption that the physical layer by itself is not sufficiently reliable. The emphasis on physical layer is focused on signal drivers and receivers, as well as design technologies for resorting and pipelining signals on wiring. In addition, as technology advanced to ultra-deep submicron (DSM), smaller voltage swings and shrinking feature size translate to decreased noise margin, which cause the on-chip interconnects less immune to noise and increase the chances of non-determinism in the transmission of data over wires (transient fault) [40]. Electrical noise due to crosstalk, electromagnetic interference (EMI), and radiation-induced charge injection will likely produce timing error and data errors and make reliable on chip interconnect hard to achieve. Error control schemes and utilization of the physical links to achieve reliability are the main concern of these layers. First, a credible fault model must be developed. Then, an error control scheme that is low power, low area, high bandwidth, and low latency must be designed. In NoC design, packet-based data transmission is an efficient way to deal with data errors because the effect of errors is contained by packet boundaries that can be recovered on a packet-by packet basis [40].

2.3.1 PNoCs Basic Elements

First we review some photonic elements used to design architecture and topologies.

2.3.1.1 PNoC Photonic Elements Waveguide, waveguide crossing, waveguide bending, microring resonator (MRR), and wavelength division multiplex can be mentioned as important photonic elements [18].

A. WDM photonic layer

First, we need to mention this can increase the bandwidth density of a links, it can be advantages. We need devices performing functions on individual frequencies in a waveguide without affecting other components. So, from Fig. 2 [22], we observe the following facts:

1. Data arrives to the sender side of the link, which must be worked up to the waveguides. MRR can also transfer photonic modulation clock rate, known as serialization. This stage requires buffers and circuitry which can convert between two clock domains [22].

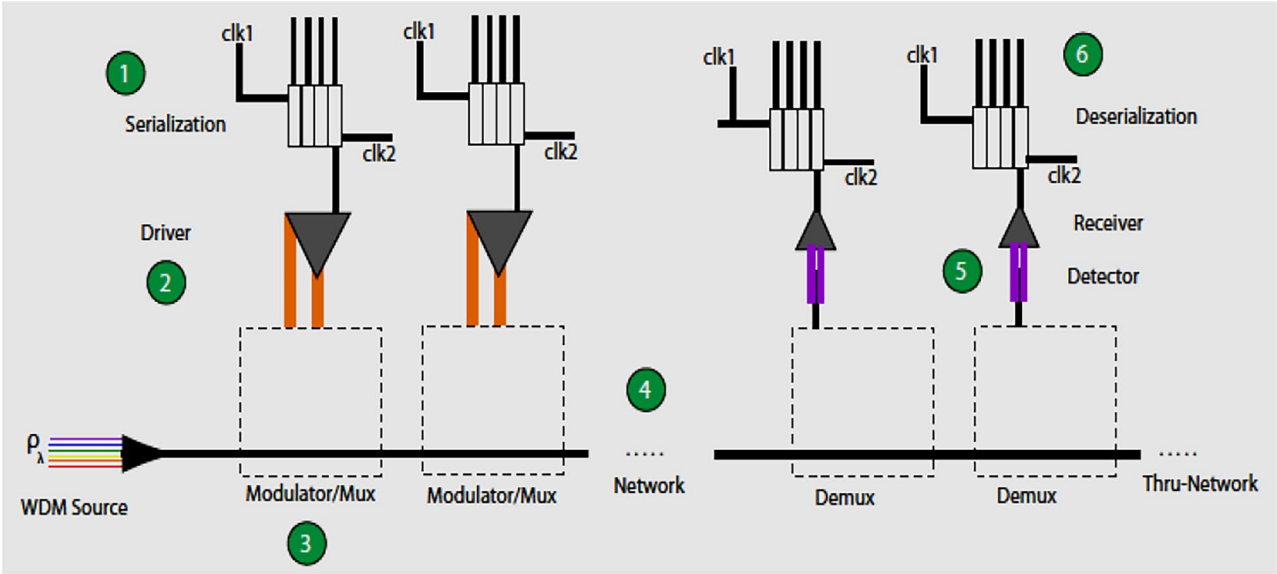

Fig. 2 Structure of WDM link [22]

2. Analog circuitry that drives 1's and 0's into the modulator, include amplifiers and wave-shaping circuits [22].
3. Modulators convert continuous-wave light of a specific frequency into light which carries the digital information. Many modulators set out serially along a waveguide can operate at their own wavelength in parallel. Usually, the continuous-wave source of light are off-chip lasers, which are multiplexed together and launched into the waveguide [22].
4. A network transparently switches or routes the information using filters or active switches, either wavelength-dependent or broadband [22].
5. Each wavelength is filtered out, and arrives to a detector which can absorb light, producing a current. The receiver converts the current to a voltage and amplifies it up to a level using digital circuitry. If some wavelengths are not filtered out and detected, they continue on to other parts of the network [22].
6. The data is ramped back down to the clock rate it started in, known as deserialization [22].

B. Waveguide and mirroring resonator

Waveguide takes photonic messages. Modulators are devices that convert electrical signals into optical ones. Detectors are used at the end of an optical communication link and convert optical signals back to electrical ones [4].

Microring resonator (MRR) can be used to determine between data change wave paths on with special resonant frequencies from one wave to another. MRR has two states: namely, an on state to transfer the signal and off state to pass the data [4, 18]. Parallel Switching Element (PSE) and Crossing Switching Element (CSE) are two basic components in Photonic Network-on-Chips used in photonic routers. A PSE is composed of one MRR and two waveguides. In this structure, waveguide is parallel to MRR. A CSE is like PSE but in this structure MRR location is the crossing of waveguide. Commonly, we have 4 ports involving input, drop, through, and add. When MRR is in the on state, the signal changes its paths and will be forwarded to the drop; otherwise the signal will continue its path and will be forwarded to the through port. Figure 3 presents these

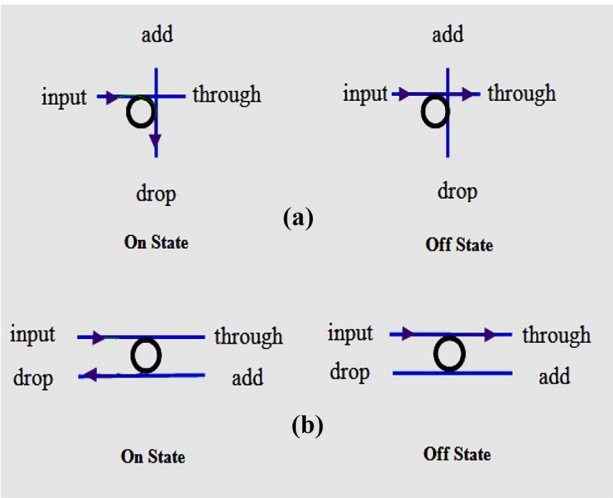

Fig. 3 CSE (**a**) and PSE (**b**) structures [4]

structures [4, 18, 30]. Figure 4 shows waveguide crossing and bending.

3 PNoC Electrical Elements

Electrical elements consist of wired communication and an electrical router. This router acts both as a controller and an arbitrator. Through the use of optical electrical interface handling serialization, deserialization, and O/E conversions, communications between electronic and optical domains can be enhanced. As the 5*5 electronic switching fabrics are composed of five input buffers and a 5*5 crossbar, four ports are connected to local processor cores, and one is connected to the O/E interface. The 5*5 Non-blocking crossbar allows five concurrent transactions if there is no contention for the same output port. Figure 5 shows the electronic switching fabric [4, 28].

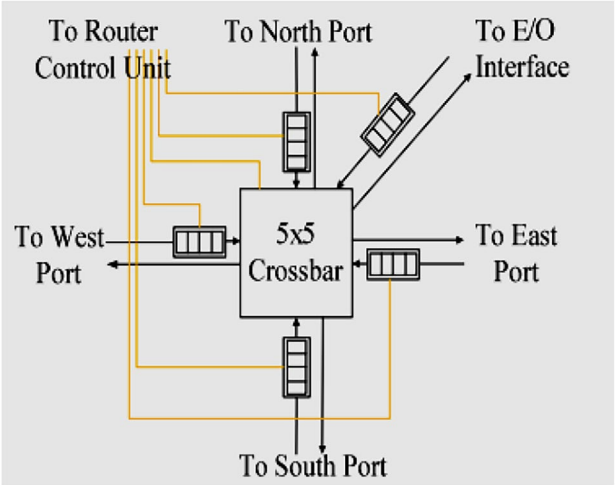

Fig. 5 Electronic switching fabric [28]

3.1 PNoC Topologies

Topology is a vital factor in photonic design since the router structure depends on it. Various topologies can be put forward for the design of PNoC, like: mesh, torus, torus NX, and square root. Some researchers also mention topologies fit for an application or application area [3].

3.1.1 Mesh

In Fig. 6, an orange rectangle is a Processing Element (PE) and columns are numbered 1, 1 to M, 1 and 1, N to M, N. Green circle is a 4*4 or 5*5 Non-blocking router. Interconnects are waveguides to transfer photonic data on photonic layer. The topology choice shows the attribute of entire system multiprocessor, where similar processing cores can be integrated as tiles over a single die. A 2-D regular topology such as a mesh or a torus can help communication needs of a CMP. These topologies fit well with the planar, regular layout of the CMP and the application-based nature of the traffic programs on the CMP can produce a different traffic pattern. Two-dimensional order topologies are most suitable for the making a hybrid network. The same reasons that made them favorite in electronic NoCs, namely their felicity to handle a large diversity of workloads and their good layout adaptability with tiled CMP chip, still apply in the photonic case. Further, high-radix switches are difficult to build with photonic switching elements so the low-radix switches as building blocks of mesh or tour network are better fit. Topological means can also be employed to overcome the absence of buffering in photonics [36].

An important merit of photonic implementations of meshes and torus concerns the nature of the guided waves. When two waveguides intersect at a right angle, the waves keep on going in original directions without any cross-talk. This allows construction of photonic NoC in a single layer and reduces the fabric [37]. The 2-D mesh topology has some beneficial attributes including a modular design, short interconnecting wires, and low-dimensional order routing algorithm such as XY [20]. The modeled electronic networks involve the mesh and torus topology. Torus offers a lower network diameter compared to meshes at the expense of longer links [38]. The mesh topology is used as a baseline for comparison. In contrast with other electronic network topologies, the mesh is simple to design due to its use of relatively low radix switches in a regular 2-D planar layout [8].

Fig. 4 Waveguide bending (**a**), Waveguide crossing (**b**) [3]

3.1.2 Torus

This topology looks like mesh, but it consists of longer links between nodes so that we can have various path selections. Figure 7 represents 4*4 torus structures. The

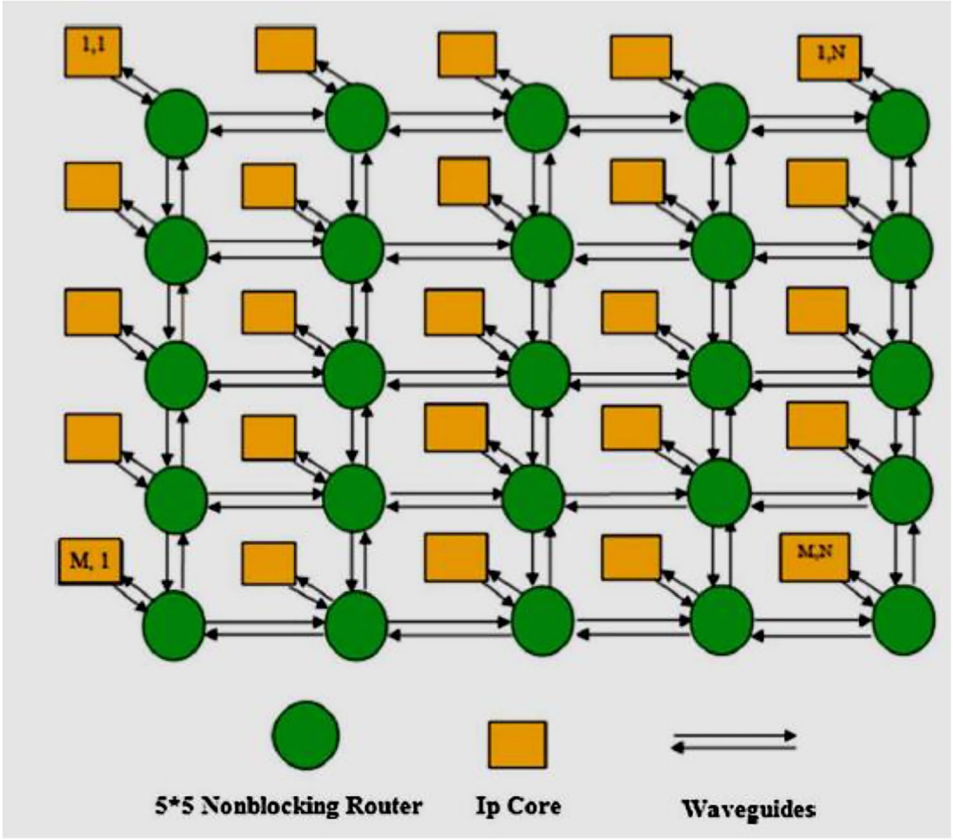

Fig. 6 The structure of 2-D Mesh topology [3]

waveguides composing the torus network are seen as thick lines, and the gateway access network for injecting packets to and ejecting packets from the network shown as thin lines. The blocks represent the following: Gateway switch (G), injection switch (I), ejection switch (E), and a 4*4 non-blocking switch (X) [13].

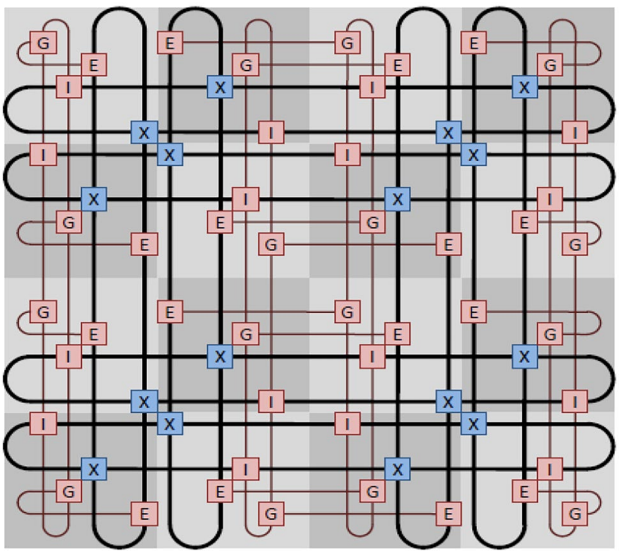

Fig. 7 4*4 torus structures [13]

3.1.3 Torus NX

The Torus NX topology is designed to keep the connectivity and scalability of the original Torus topology while decreasing the overall insertion loss [13]. The name of this topology which means torus, has no crossings and alludes to the strategy used in the designing of this network. Many design decisions were made in order to remarkably reduce waveguide crossings and to reduce the insertion loss overhead. In conflict with the Torus which required a complex access network to simplify injection and ejection from the network, Torus NX uses a new gateway design which splits the access point into two blocks for modulation and detection and circumvents adding any additional crossings to the torus through the use of the 1*2 PSE variant [13].

The modulation block enables a message to be injected north or south, while the detection block can receive signals coming from the east or west direction. This scheme is well suited for dimension-ordered routing which is the preferred routing for this topology. Torus NX also uses an optimized version of the 4*4 non-blocking switch. Figure 8 shows Torus NX structure [13].

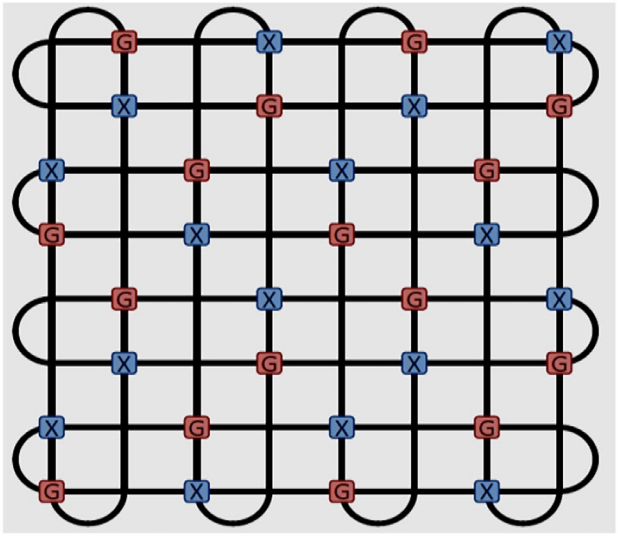

Fig. 8 Torus NX [13]

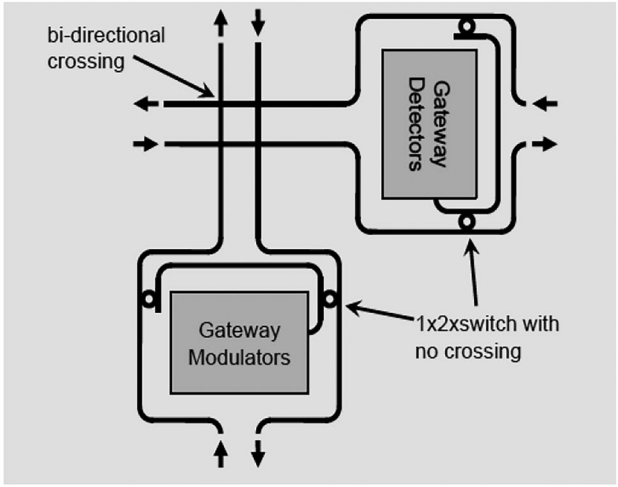

Fig. 10 Design for a photonic gateway with an integrated bidirectional crossing [13]

3.1.4 Square Root

The Square Root is built recursively beginning with a 2*2 quad, as shown in Fig. 9(a), has no waveguide crossings outside the 4*4 switches. A 4*4 Square Root is composed of four sets of quads, as shown in Fig. 9(b), by connecting quads through central switches and inter-quad express lanes. In a similar fashion, an 8*8 Square Root can be constructed from four 4*4 Square Roots. This recursive can build any size square topology with dimension that is any positive integer power of two [13]. Figure 10 shows the gateway structure.

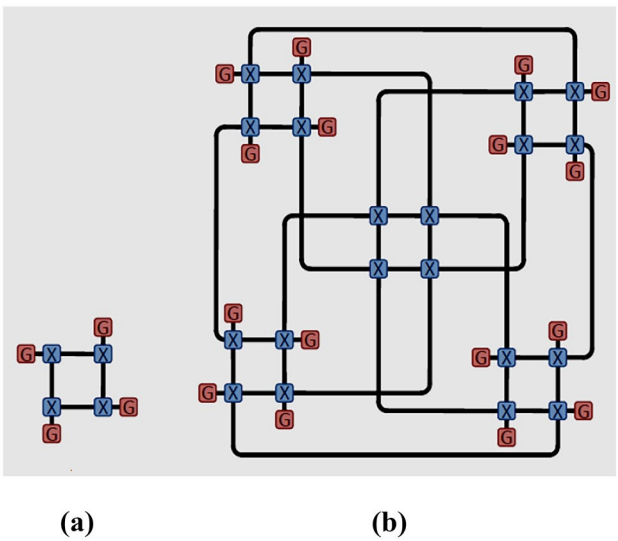

Fig. 9 Square Root [13]

3.2 PNoC Hybrid Architecture (3 layer architecture)

Photonic Network-on-chip has 3 layers as follows: Photonic plane topology (top layer) with lines illustrating waveguides and blocks representing photonic routers and gateways. Underlying the photonic plane is the electronic control plane composed of standard metal wires (yellow lines) and electronic routers (grey blocks). The electronic wires and routers are strategically placed so that the network quite mirrors the photonic version. The reason for this placement is to simplify the circuit-switching process. Each node of the processor has a connection to a gateway on the optical plane

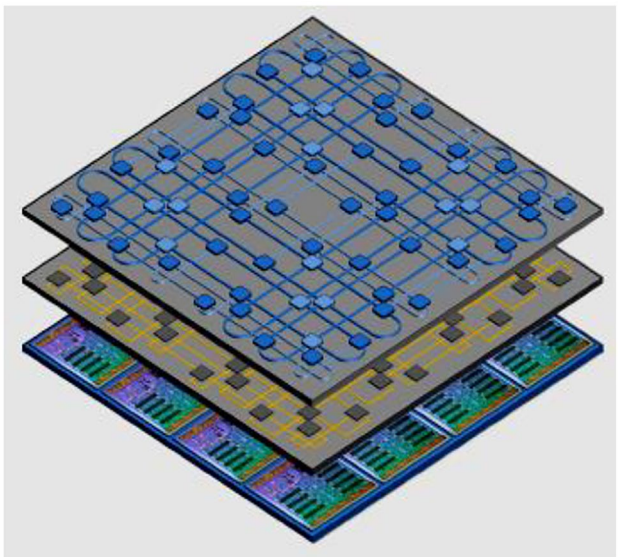

Fig. 11 3 layer architecture [13]

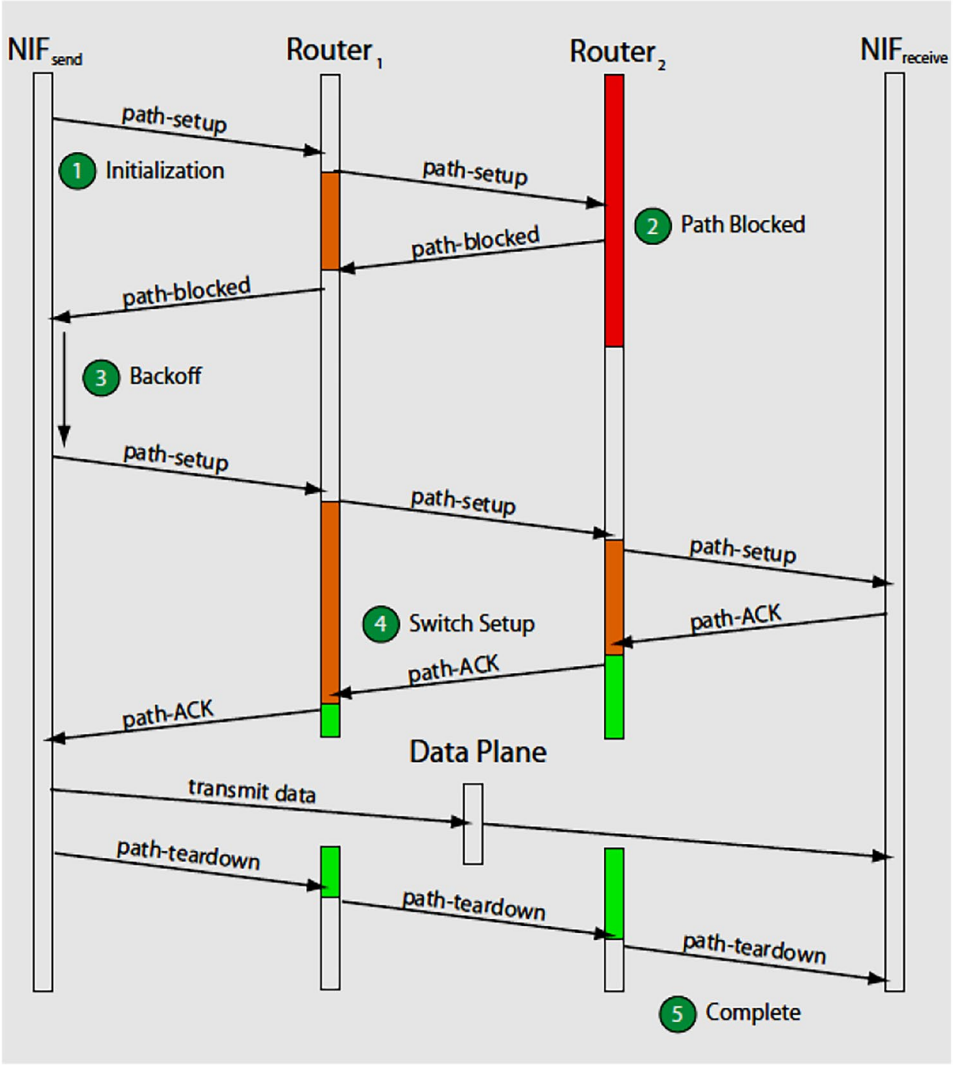

Fig. 12 Circuit switching phases for path reservation [22]

(for data generation and reception) and a connection to the control plane. So, the top layer is photonic layer, an electrical layer is in the middle and processing layer is the bottom [13]. Figure 11 shows this topology.

4 NoC and PNoC routing and Swithching methods

4.1 NoC Switching Method

Routing transfers data from source to destination with a clearly defined strategy. In the literature, researchers have classified the routing algorithms according to various criteria [6]:

1. A routing is called source routing if only the sender provides the path by which the data will flow; it is called distributed if the transit decision is taken locally at each node. We can also find a classification similar to the previous one except that it defines a more general routing strategy regardless of the source. When routing

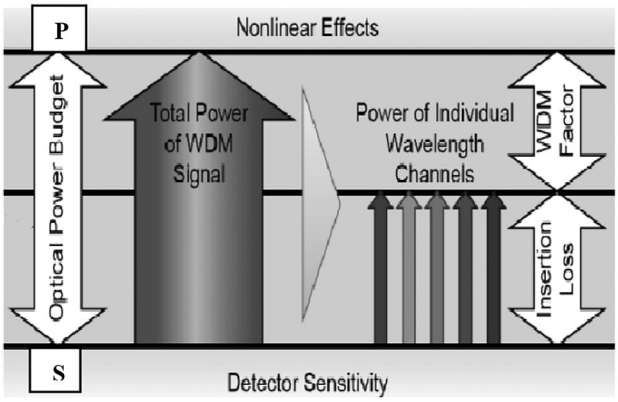

Fig. 13 Optical power budget [24]

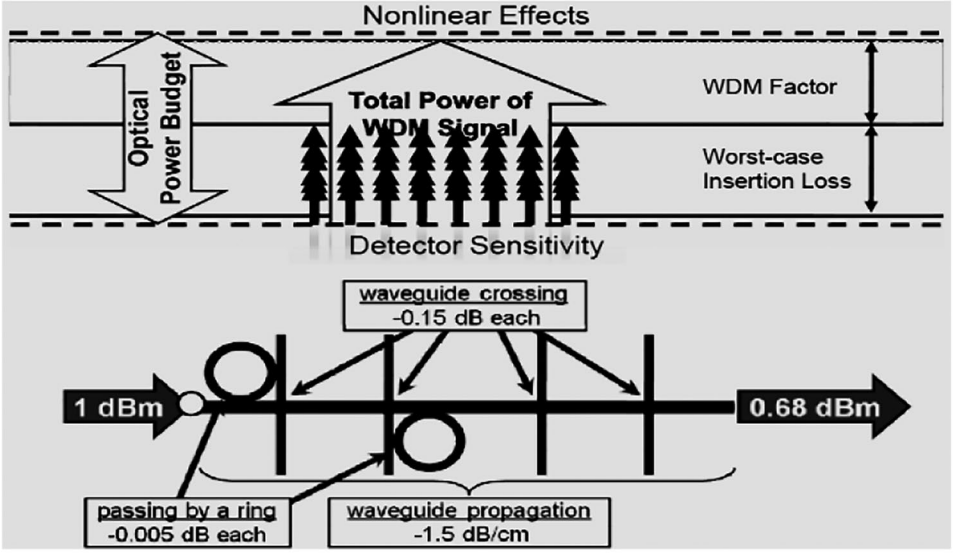

Fig. 14 Effect of Waveguide and Microring resonator loss [24]

decisions are identically distributed across the network, the routing is called centralized. If these decisions are taken locally, the routing is still called distributed [9]. As we can see the routing decision does not take the sender into account.

2. The routing is deterministic if the transit path is determined by the sender and the receiver only. The path between the same network correspondents is invariable. However, if the transit of data between two network elements can be achieved through multiple paths, routing is then called adaptive. This is possible due to the decisions taken locally at the nodes. The implementation of adaptive routing algorithms can generate complicated paths but can ensure a better flow of data within a NoC [6].
3. The routing is called circuit switching type when a circuit (a path) between the transmitter and receiver is reserved for the duration required to transfer data. It is called packet routing when the data to be transmitted is divided into packets containing a portion of the data and routing information. The packets may follow different paths to reach their destination [6]. A routing algorithm usually has one or more characteristics as mentioned earlier. For example, an adaptive routing is generally a packet switching routing [6].

The primary function of switches is to determine when and how the inputs of a router will be connected to its outputs [29]. There are several switching techniques that can point to store-and-forward, virtual cut-through and wormhole, among them:

1. Store-and-forward: the transferred data is split into packets and each packet contains routing information. When a packet reaches a node, it is entirely saved in a buffer and routing information is extracted to determine the appropriate output port.
2. Virtual cut-through: the routing information is contained in the first bytes of the packet. Instead of saving the entire package like store-and-forward, the packages are sent as soon as the output port is determined. In case this port is in use, the package will be saved in a buffer [26, 34].
3. Wormhole: the packets are split into sub-packets called flits (Flow Control Units). The control data are contained in the header flit. As a result, a single packet can be transmitted by different nodes. This will reduce latency, but may cause bottlenecks in the network.

4.2 PNoC Switching Method

Photonic Network-on-Chip has no photonic buffer. For this reason we should use circuit switching method. This method does not need any buffer and hence is appropriate for use in photonic Network-on-Chip. The steps for organizing or reserving an optical data path are as follows [22]. A processor node with a request for sending data must first create the photonic link using the electronic control plane. The node

Table 1 Configuration Parameters [4]

Simulation Parameters	Values
Message Size	1024 Bits
Max Packet size	32 Bits
Laser Power	10 db/m

Table 2 Parameters and Symbols for 5 by 5 of Crux Router [44]

Parameters	Symbols
Port i	P_i
Port j	P_j
Injection port	In
Ejection port	Eje
North port	N
South port	S
West port	W
East port	E

inserts a Path-Setup message, which includes the destination address in the header.

The Path-Setup message travels through the electronic network, tracing out a possible path for the optical message to take. At each router hop, the state of the associated photonic router is checked (contained within the logic of the electronic router). If the path is available for use, then a reservation is set for the specific path and the Path-Setup message proceeds towards the destination. If any resource is unavailable then a Path-Blocked message must be returned. The Path-Blocked message retraces the route of the Path-Setup message so that all reservations can be canceled. Once the Path-Blocked message reaches the source node, the node will be signaled to reattempt the transmission after some hold-off period [22].

If the Path-Setup arrives at the destination, the destination is marked indicating that a complete optical path on the photonic plane has been reserved, and a Path-Ack message is sent back. The Path-Ack retraces the same path to the source. At each hop, the previously determined reservation can be applied and suitable photonic devices are actuated. Before the Path-Ack proceeds, the newly activated devices are marked so that other Path-Setup messages cannot change them [22].

When the Path-Ack message reaches the source, the source knows that a complete optical path on the photonic data plane has been determined and can begin to transmit data. Once the last data bit has been sent, a Path-Breakdown message is immediately sent. Again, this message will trace out the same path as the original Path-Setup message so that previously allocated photonic devices are now free to be utilized by a future path request. Figure 12 shows these phases [22].

Table 3 Optical Loss Parameters and Symbols in question (2) [4]

Parameters	Symbols
Optical Loss in Router (x,y) from port i to port j	$L_{(Pi,\ Pj)}R(x,y)$
Router (x,y)	R(x,y)
Switch Loss in port i to port j	Switching (P_i,P_j)
Chip size (cm^2)	C_S
Network Size	M*N

5 PNoC Challenges

Recent notable advances in nanoscale silicon photonic integrated circuitry specifically compatible with CMOS fabrication have created new opportunities for leveraging the unique capabilities of optical technologies in the on-chip communications infrastructure. Based on these nanophotonic building blocks, photonic network-on-chip architecture can exploit the enormous transmission bandwidths, low latencies, and low power dissipation, enabled by data conversion to optical domain [36]. PNoCs are one of the important implementation for chip design, exploiting the progress and evolution of hardware. On the other hand, this network has notable challenges, one being optical loss in the photonic layer. Also, we want to efficiently transfer optical data from source to destination in case there were more than one path to choose. In this case, we should have a standard to choose the path. For this reason, we consider optical loss factors to find the path with least optical loss. To understand this challenge clearly, optical power budget is reviewed. The optical power budget of a photonic network evaluates the amount of Waveguide Division Multiplexing similarity and insertion loss that can be permitted. Many currently proposed photonic interconnection networks consider off-chip lasers to provide optical sources which are then coupled into the chip where they are modulated, routed, and received [3].

Optical amplification in an on-chip environment is not easily done in a CMOS platform. For this reason, the power received at the photo-detectors must remain above a certain lower threshold to ascertain suitable detection of data bit streams. This limitation can be partially overcome by

Table 4 Additional optical Loss Parameters, Symbols and values in Eq. (2) [4]

Parameters	Symbol	Values
Loss in waveguide crossing	L_{WC}	0.15 dB [26]
Loss in waveguide bending	L_{WB}	0.005 dB/90° [26]
Loss in MRR when On state and optical data drop in to MRR	L_{DRon}	0.5 dB [26]
Loss in MRR when Off state and optical data pass by MRR	L_{PRoff}	0.005 dB [26]

Table 5 Routing Algorithm Pseudo codes [4]

Routing Algorithm		
Phases	**Pseudo codes**	**Comments**
Phase 1	Assign values of M, N	Dimension of topology
Phase 2	Determine source and destination nodes	With running each traffic patterns algorithm
Phase 3	Running each turning model algorithm at each router	To locate suitable port
Phase 4	Running Circuit-switching simultaneous phase 3	For reserve path between each router
Phase 5	Repeat phase 2 and phase 3 again	-
Phase 6	Path reservation end	When receive destination node
Phase 7	Repeat phase 3 to phase 6	For each other two paths
Phase 8	Evaluate Optical Loss at each router	Each router at each paths
Phase 9	Evaluate Optical Loss at each path	Summing Optical Loss values which are gain phase 8
Phase 10	Compare values of phase 9 to determine low optical loss	Which is called Best-case loss
Phase 11	Choose Best-case loss path to transfer Optical data	-

increasing the optical power that is injected into the chip. However, this also sets an upper threshold due to nonlinearities of the silicon material which may potentially distort the signal. Distortions are caused by nonlinearities within silicon which contribute additional insertion losses and can also cause unwanted shifts in the resonances of ring resonators. This limitation is labeled as nonlinear effect in Fig. 13. The difference in the two thresholds is called the optical power budget [24].

As shown in Fig. 13, the optical power budget affects the design choices of a given network architecture by restricting the sum of the Waveguide Division Multiplexing factor and the network insertion loss. The Waveguide Division Multiplexing factor measures the power difference between an entire Waveguide Division Multiplexing signal and its elemental wavelength channels. This factor needs to be accounted for the nonlinearity threshold determined by the total power in the waveguide while the detector sensitivity depends on the power in the individual wavelength. The remaining portion of the optical power budget must accommodate the worst-case insertion loss that an optical message could experience in the network. Figure 14 shows an example of the calculation involved in determining the insertion loss for an optical signal being injected into a small network segment at 1 dBm [24]. The signal is ejected at 0.24 dBm after propagating across a 0.1 cm distance, passing by two ring resonators, and entering four waveguide crossings. The total loss for this example is 0.76 dB. For a full-scale photonic network, all valid optical paths need to be examined to determine the highest-loss path. The relationship between the various device limitations and system-level metrics is summarized in Expression (1) [24]:

$$P - S \geq ILmax + 10\log n10 \quad (1)$$

where P is the power threshold, we limit the optical power and S is the detector sensitivity. The optical power budget is P—S. The worst-case optical path in terms of insertion loss is ILmax and n specifics the number of wavelength channels being used. P, S, and ILmax are explicit in decibel units.

While it may be desirable to maximize the number of wavelength channels used to increase bandwidth through similarity and to create scalable photonic networks at the cost of higher insertion losses, Expression (1) shows an essential limitation. From an architectural standpoint, P and S are essential design restrictions inflicted by the photonic devices. Therefore, a designer must strike a balance between the desired link bandwidth and the desired complexity of the network [24]. Reducing optical loss causes some noticeable point such as: n (number of wavelength channels) is increased and we can maximize the

Table 6 Comparing Optical Loss (%) [4]

Optical Loss (%)	**Madbench**	**Bitreverse**	**Random**	**Torn ado**	**Cactus**	**Paratec**
West-first	0.17	0.18	0.20	0.23	0.27	0.28
Odd–even	0.28	0.32	0.35	0.41	0.48	0.50
Negative-first	0.39	0.43	0.53	0.51	0.54	0.67
North-last	0.55	0.57	0.59	0.62	0.67	0.77

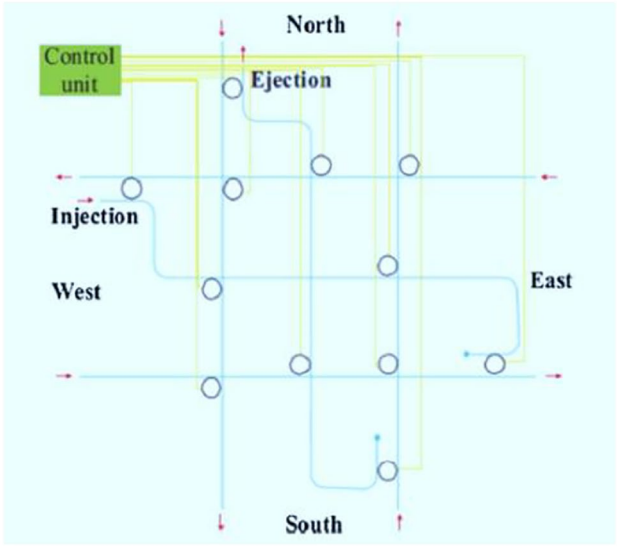

Fig. 15 Crux router [44]

optical data sent. On the other hand, delay and optical power are decreased [4].

6 Testing

This section discusses testing for optical loss as expressed by Eq. (2) [4]. Optical loss is simulated from configuration parameters (Table 1), routing algorithm (Table 5), turning models, mesh topology, CRUX router Fig. 15. And traffic patterns. Simulation results (MATLAB and CLAP) are shown Table 6 and Fig. 16. Simulation parameter tables, routing algorithm pseudo codes and experimental results are presented in detail in paper [4, 19, 39].

$$\begin{aligned} L_{(P_i,P_j)}^{R(x,y)} &= \sum_i^j \text{Switching}(P_i, P_j) \\ \text{Switching}\left(P_i, P_j\right) &= L_{WC} * L_{WB} * L_{DRon} * L_{PRoff} \end{aligned} \tag{2}$$

In Eq. (2), $L_{(P_i,P_j)}^{R(x,y)}$ is optical loss in router (x,y) from port i to port j, Switching (Pi,Pj) is Switch loss in port i to port j; this variable is evaluated with multiplication of L_{WC} which is waveguide crossing loss, L_{WB} is waveguide bending loss, L_{DRon} is loss in MRR when On state and optical data drop in to MRR and L_{PRoff} is loss in MRR when Off state and optical data pass by MRR [4, 18].

Tables 2, 3 and 4 shows that West-first turning model [16] with Madbench, Bitreverse, Random, Tornado, Cactus, and Paratec traffic patterns [19, 39] has the lowest optical loss percentage compared with other turning models. Also, it shows that Paratec traffic pattern holds the highest optical loss percentage compared with other traffic patterns. This depends on the location of the nodes either in the edge or inside the topology. It also depends on our turning models clockwise and counter-clockwise a prohibited turn [15, 16]. At traffic patterns it can depend on their algorithm steps and which mechanisms are used or how nodes are determined and their communications [19, 39].

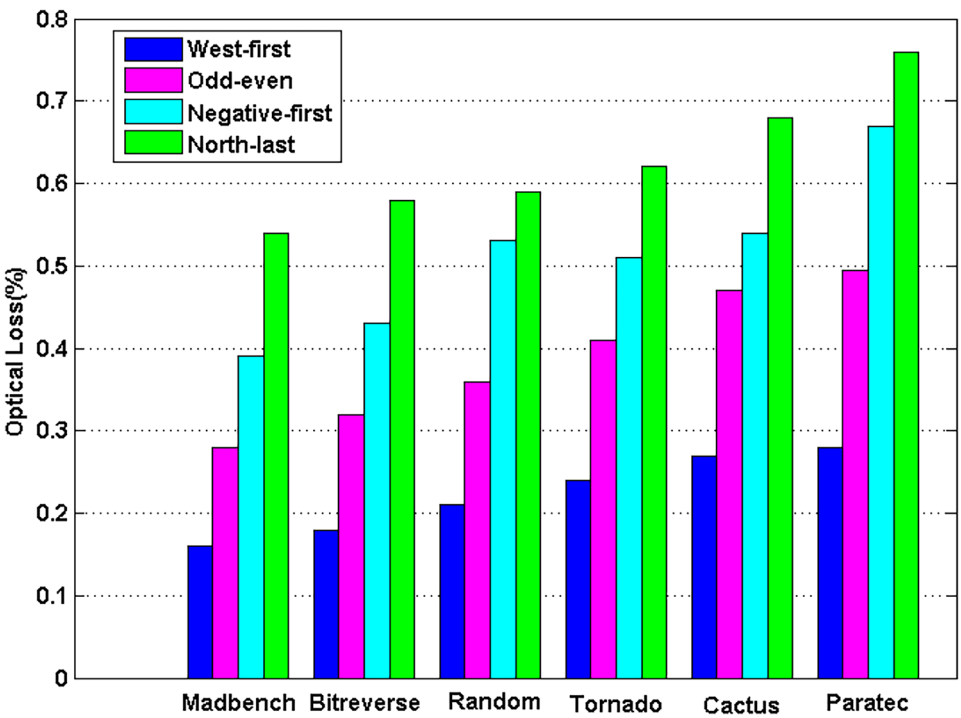

Fig. 16 Optical Loss percentage with four turning models and different traffic patterns [4]

7 Conclusion

Through this paper we review some basic and fundamentals concepts of NoCs and PNoCs networks such as: architecture, topology, electrical and photonic elements, routing, layering and switching methods, and PNoC challenges such as optical loss. In these systems, pre-fabrication testing based on the type of final application is essential and has been discussed in Sect. 5. NoCs and PNoCs involve many techniques requiring theoretical and experimental studies; in this paper we try to note some basic definitions relevant to these networks.

Data Availability Statement The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of Interest The authors declare that they have no competing interests.

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