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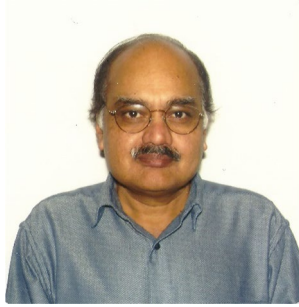
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Ujjwal Guin is currently an Assistant Professor in the Department of Electrical and Computer Engineering, Auburn University. He received his Ph.D. degree from the University of Connecticut in 2016. He is actively involved in Hardware Security and Trust, Supply Chain Security, Cybersecurity, and VLSI Design and Test projects. He has developed several on-chip structures and techniques to improve integrated circuit security, trustworthiness, and reliability. He is a co-author of the book, *Counterfeit Integrated Circuits: Detection and Avoidance*. He has authored several journal articles and refereed conference papers. His projects are sponsored by the United States Secret Service, National Science Foundation (NSF), Air Force Research Laboratory (AFRL), and Auburn University. He serves on the SAE International G-19A Test Laboratory Standards Development Committee and G-32 Cyber-Physical Systems Security Committee. He currently serves or has served on technical program committees of reputed conferences, such as, DAC, HOST, VTS, PAINE, VLSID, GLSVLSI, ISVLSI and Blockchain. He is a Senior Member of IEEE and a Member of ACM.



Yashwant K. Malaiya received the M.S. degree in physics from Sagar University, Sagar, India, the M.Sc.Tech. degree in electronics from BITS-Pilani, Pilani, India, and the Ph.D. degree in electrical engineering from Utah State University, Logan, UT, USA. He was an assistant professor at SUNY-Binghamton during 1978-82. He then joined the Computer Science Department, Colorado State University, Fort Collins, CO, USA, where he has been a Professor since 1990. He has widely published in the areas of fault modeling, reliability, testing, and quantitative security risk evaluation as well as social history and demography. He served as the General Chair of IEEE International Symposium on Software Reliability Engineering (ISSRE), Denver in 1993 and 2003. He has served as a member of the program committee and currently serves as a member of the ISSRE Program Board. He also served as a general chair of IEEE Asian Test Symposium, Shanghai, 1999, International Conference on VLSI Design (VLSID 1993), and 24th ACM/IEEE International Symposium on Microarchitecture (Micro-24).

He cofounded the IEEE International Workshop on IDDQ Testing in 1995 (later known as DBT) and served as its first General Chair. He has contributed the concepts of Detectability Profile (1984), Antirandom testing (1995), Coverage based defect detection model (1994) and the Alhazmi-Malaiya (AML) Vulnerability Discovery Model (2005). His Antirandom testing paper was included in “Most Influential Papers - The 30 Years of ISSRE” in 2019. His 1980 paper on delay faults was selected for the “25th Anniversary Compendium of papers” from the International Test Conference, 1994. He co-edited the IEEE CS Technology Series books “Software Reliability Models, Theoretical Developments, and Evaluation and Applications” in 1990, and “Bridging Faults and IDDQ Testing” in 1992. He served as the chair of IEEE-CS Technical Committee on Microprogramming and Microarchitecture (1988-92), and a member of executive committee of the IEEE CS Technical Activities Board (1988-98) and Conference and Tutorials Board (1994, 2000, and 2001). He has supervised PhD and MS students in Computer Science, Electrical Engineering and Systems Engineering. He has served in ABET for accreditation of Computer Science programs in USA and overseas. He has developed and taught new courses in Fault-tolerant Computing and Quantitative Security. Dr. Malaiya is a recipient of the IEEE Third Millennium Medal and the IEEE Computer Society Golden Core Award.

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