High Fault Coverage Built-In Self-Test for 3rd Generation Mobile Phone User

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ABSTRACT – On-chip Built-In Self-Test (BIST) based implementation on RF devices especially on cellular mobile phone has been proposed. In this approach, high-level functional test can be done with one complete test path. Central baseband processor roles as Test Pattern Generator (TPG) as well as Output Response Analyzer so that it can generate test patterns through the complete path over the transceiver components and read the output back. In order to compensate the fact that a component level diagnosis is impossible with functional test if there are multiple components cascaded, we adopted the solution from one of the recent study which utilized embedded sensors to observe the each component behavior. Finally combining it with the functional test through the transceiver path brings a high fault coverage rate as well as an efficient test strategy for the mobile phone user.[1]

1. INTRODUCTION

Extensive data usage in 3rd-Generation (3G) technology leads us to the situations that mobile phone can be a critical device. Most users will demand a reliable phone which has no faulty because of the activity they would do with the mobile device. For example, in the near future, having a multimedia mobile phone will let us download and listen to mp3 music files. Due to the characteristic of the mp3 file, if there were errors in the downloaded mp3 file the music would not play properly or sometimes it would not even be opened. The mobile phone manufacturer as well as the consumer needs to be ensured that every transmittion of multimedia data is reliable.

Most of the testing and verification process is being done in the manufacturing process or before it comes out to the market. However, due to frequent use of the mobile device there should be a test function built in to the mobile phone itself so that the users can easily test the mobile phone device to make sure the device is always capable of extensive data service without having any errors or performance weakness. The standard test requirements for present mixed-signal chips are complex and it needs of measurements considering specific specifications[2], however, the objective to this project is to invent and develop a easy test method and add-in the functionality which could be built into the mobile device so that user can easily test their phone themselves. Built-In Self-Test (BIST) approach has been choice because of the characteristic that it does not need external hardware to test the device. Thus user can always make sure the phone works as it should be and by users test their mobile device frequenly, it can prevent wrong data to be sent or received. The approach will ensure customers to satisfy with the product and it altermately shows a trusty business solution.

In this paper, we describe the development of on-chip test by the central DSP processor of a mobile phone baseband modem. We begin with an overview of the cellular network in Section 2 and an overview of the loop back BIST on transceiver of RF devices which has been proposed in study [3] and study [4] are described in Section 3. This is followed by a new proposed BIST approach through this work in Section 4. Experimental plan to implement and verificate the suggested approach is presented in Section 5 and conclude in Section 6 by summerizing the work done and analizing the innovating factor of the work as well as describing the weakness and strongness of the approach.

2. OVERVIEW OF CELLULAR NETWORK

The 1st Generation (1G) technology came out with the first cellular phone network which only has voice service over the air. Most of base stations were in an analog mode. When moving to the 2nd Generation (2G) network, the voice capacity increased and it started to have data service but with a limited bandwidth. With the data service, one can send text message to another and such. The significant change from 1G to 2G is the change from analog to digital. From 2G network, base stations started to have capability to transmit voice in a digital form. Finally 3G network came out with the increased voice capacity and with the extensive data service such as video streaming, location based services, and on-line gaming [1]. In terms of the cellular phone technology, most of the 2G network was adopting Time Division

[1] This work was advised by Dr. Vishwani Agrawal through the class project of ELEC6970 in Auburn University, AL. Experimental supplies such as RF-evaluation boards and its accessories were provided by Dr. Richard Jaeger from Auburn University, AL

Multiple Access (TDMA) in case of U.S., while the 3G network is mostly Code Division Multiple Access (CDMA) or even Wide-CDMA (W-CDMA) which has more bandwidth than the conventional CDMA so that it can support more extreme quality and quantity of the video streaming more quickly and efficiently. TDMA allows a number of users to access RF channel without interference, by allocating unique time slots to each user within each channel. CDMA is more in digital technology which enables every communicator to be allocated the entire channel all the time by having different code domain (or code identity) than the others.

Base-stations are located each cells as shown in figure 1 and one cellular phone user will be accessing one base-station and each base-stations are connected so that the user can talk to another user who are in a different cell region.

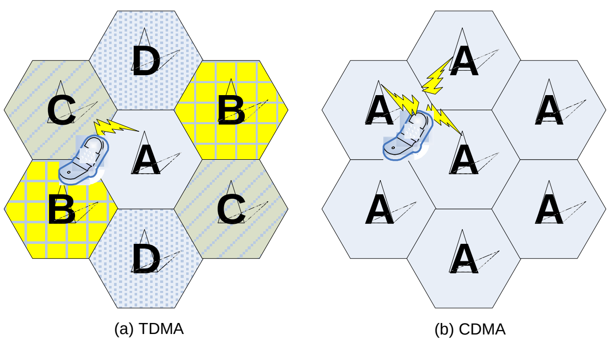

Figure 1. TDMA basestations vs CDMA basestations

Trouble shooting could be easily done with the analog testing on 2G network. For example, one power meter could test and diagnosis most of the problems on 2G network. Within 3G network, however, needs to be tested in fairly complicated method. With 3G CDMA, every basestations are distinguished by different code domain, not by its frequency like we see in TDMA. Thus one phone interacts with multiple base stations with synchronized frequency. It shows that testing the 3G base-stations (or network) would not be easy as testing 2G base-stations and thus testing 3G network requires considering the significantly more base stations which requires field technicians to scan multiple neighboring base stations for interference that may affect other network performance.

Testing problem also rises on the mobile device level. With extensive data service that 3G has, higher quality testing is required to 3G enabled devices than the 2G enabled devices. First reason is because, while voice can tolerate signal disruption and loss, similar problems could critically harm data transactions. Next reason is due to the expectation from mobile users who like to have faster data transaction rate as well as stable signal with high quality.

The object in order to apply the project idea was chosen to be a smart phone from one of the CDMA cell phone company. Samsung model name SPH-I500 has been chosen to be the initial object to be investigated. Note that most of the cell phones with the same technology would have very similar structures and interfaces between each component. The plan was to investigate the specific model and abroad the knowledge to adapt and apply to general CDMA devices. As shown in figure 2 below, there are three types of major processors and couple of components that are consists the mobile phone system of SPH-I500.

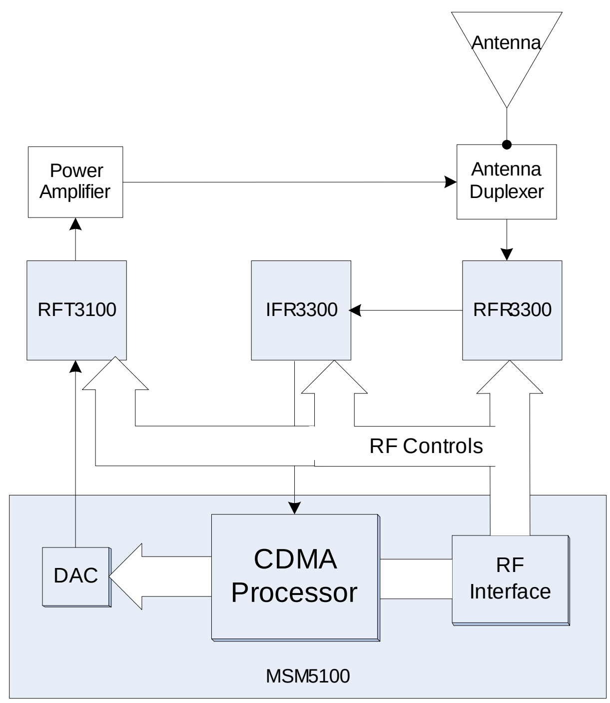

Figure 2. CDMA Wireless Mobile Solution Diagram

One complete solution on a (Radio Frequency) RF communication usually consists of a baseband modem, an analog-baseband-to-RF upconverter, an Intermediate Frequency) IF-to-baseband down converter and a RF-to-IF down converter. Each component enables signals to be travel along each other by adjusting its input signal property.

Mobile Station Modem 5100 (MSM5100) is the main modem that enables the wire communications and it consists of CDMA processor, RF interface controller, DAC and variety of peripherals. The MSM5100 device performs baseband digital signal processing. It is the central interface device in the mobile unit, connecting RF and baseband circuits as well as memory and user interface features [1]. RFT3100 baseband-to-radio frequency transmit processor gives the full conversion from analog baseband to RF so that the power amplifier can take the RF signal to the antenna to be sent outside [1]. RFR3300 is needed when RF signal come in through the antenna. It performs downconversions from RF to IF and let IF signal pass to the IFR3300 which is IF-to-baseband processor and it already includes low pass filter and ADC in most cases. Most of RF-to-IF downconverter integrates low noise amplifiers (LNA), and mixers for downconverting from RF to IF[1].

3. OVERVIEW OF LOOP-BACK BIST ON RF DEVICES

Previous study has been found which suggested a functional test on RF-transceiver front-end using BIST approach. It aimed at spot defects of production in CMOS process[3]. Since high level functional testing does not necessarily require diagnosis, the loop-back approach is used by activating one path throughout the RF transceiver. The technique is used having the advantage that all the functional front-end blocks are under test, and their sensitive nodes are not affected by external equipment, neither much extra test circuitry is put on a chip[3]. Especially aiming CMOS RF ICs for functional test very applicable since they are frequently subjected to spot defects that can severely degrade the performance or result in chip malfunction[2].

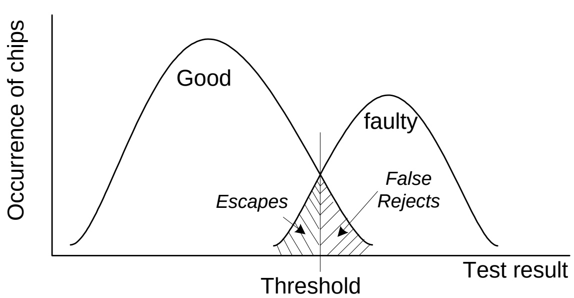

Figure 3. Illustration of Test Pass/Fail Threshold by Parameter Tolerances

As shown in figure 3, by testing various parameter could distinguish most of faulty chip but there are still region around threshold that could escape from detection and vice versa. The functional testing comes into play in this case for guarantee of specification compliance that could avoid false rejects of good ICs. However, large number of the test escapes happens as well in the functional testing and usually it can be overcome through burn-in technique [3].

With functional test, number of critical spot defect models has been investigated. As shown in Figure below, high density CMOS technology tends to have more spot defects. CMOS LNA spot defect model is shown in figure 4 and it results the relation ship that could represented by the following:

$$\Delta NF_{LNA} \propto N_{Ro} \propto R_o \qquad \cdots (1)$$

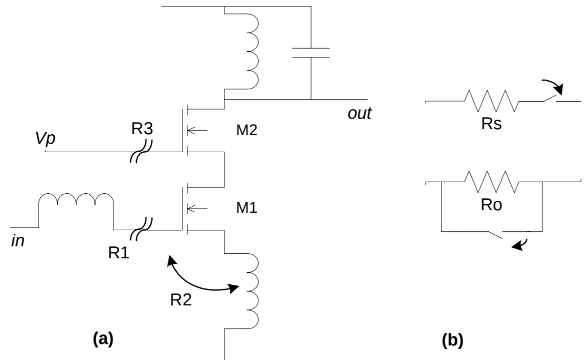

Figure 4. (a) Possible Spot Defect Sites in CMOS LNA Circuit, (b) Models of Resistive Bridge and Break [3]

Where ΔNF_{LNA} is increase the noise figure in LFA, N_{Ro} is the noise imposed by R_o transforms to the output with the same gain. The relationship from (1) shows that for large R_o, change on NF_{LNA} would be significant, resulting the gain to be degraded.

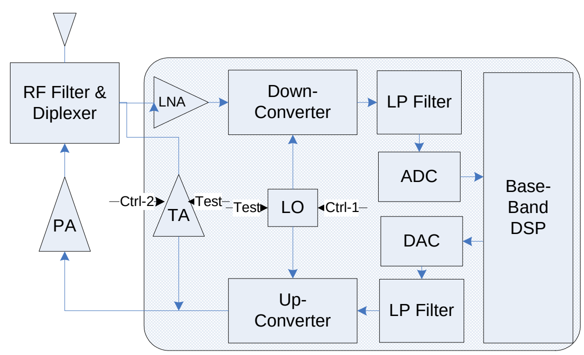

Figure 5. Block Diagram of General RF Application Transceiver with BIST Control Signal 'Test' [3]

To enable BIST the test amplifier (TA) is inserted to make a isolated loop back path to the baseband DSP with out interfering with outside RF signal from the antenna. The approach mainly targets on-chip RF front-end, not the complete transceiver [3]. With BIST approach, baseband processor could serve both as a test pattern generator and output response analyzer. The test loop consists of both the transmitter and receiver path and they are closed by TA [3]. Looping through shorter path such as baseband processor -> DAC -> ADC -> baseband processor could be realized as well [3]. Significant thing in this approach is almost zero overhead if the TA is a low power variable gain amplifier that could be powered down in normal mode of operation [4]. Another important BIST controller component is the frequency synthesizer (LO) which in test mode it support Tx to operate at the carrier frequency of the receiver because in normal Tx signal may require different frequency than carrier frequency.

4. PROPOSED BIST APPROACH

There is no need for structural-component level testing for this application that is mainly because the test is for mobile user not manufacture and users do not have capability to fix themselves. Only functional test is needed on front-end of the device which includes transceiver and amplifier. Easiness of the test is mainly from the simple BIST control logic that signal 'BIST start' will initiate the test and user will see the phone response with 'Test fail/pass' indicator.

The insight of the BIST approach is to activate one critical path that includes most of the subcomponents that need to be test as a whole. The central base band modem will generate test pattern and it will loop back to the modem. The modem has ability to process data analysis on output response from circuit under test (CUT) as well as generating various test patterns to the CUT. As shown in figure 6, the path will include critical components to be test for extensive data transactions.

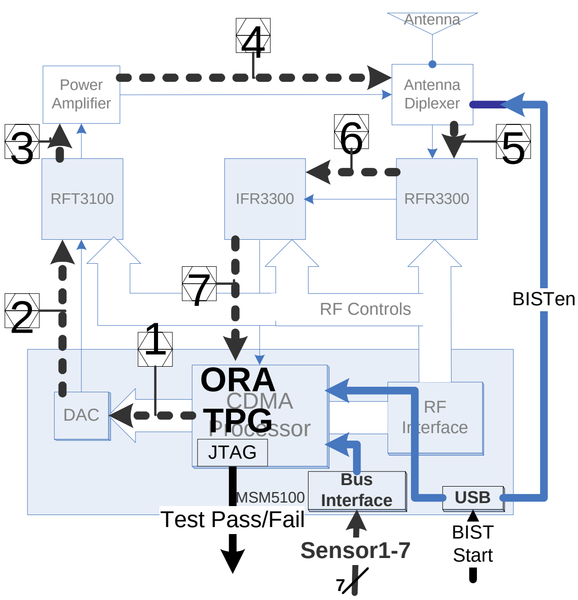

Figure 6. Newly Suggested RF BIST Path

First give a BIST-start signal using the USB interface and let the test pattern to be generated from CDMA processor to the baseband-to-radio frequency transmit processor (RFT3100). The pattern goes through the power amplifier and Antenna diplexer. Having diplexer that has capability of transfer signal from transmitter to RF receiver (RFR3300), it can route the test pattern back to CDMA processor by bypassing IF (Intermediate Frequency)-to baseband processor (IFR3300). Finally the CDMA processor determines whether the test passed or failed by comparing with expected result. User can see the test pass/fail signal. It is the CDMA processor being test pattern generator and output response analyzer. The major draw back of this approach is due to the fact that diagnostics in an individual component level are impossible. However, by inserting embed sensor between each component and observe the expected sensor output, the problem can be solved [6]. In addition, adding sensors makes the power amplifier and the antenna diplexer to be in one test path since they are observable through sensors. This will give us both high-level functional and deep-level component specification test.

Note that number of assumptions has been made. First, antenna diplexer has to be newly designed to have ability to route Transmit (Tx) signal back to Rx processors. Control signal 'BIST enable (BISTen)' should be involved in this case to switch antenna diplexer input from antenna to internal Tx signal. Second assumption is the reliability of the sensors that would be inserted in between each component. Then the Sensor outputs can be used to verify the system as well as specification verification on individual components [6]. Note that each sensor is in different kind. For example sensor number 1 and 2 should be in different kind since sensor 1 takes digital input but sensor2 takes analog input.

In order to diagnosis and generate 'Test pass/fail' signal to the user, central processor will read in all seven sensors through a general bus interface. By looking up the expected result in the processor memory, it can diagnosis the faulty point resulting an accurate test.

By observing output response values of one high-level path over transceiver and 7 embedded sensor values gives significant improvement fault coverage in a short amount of time.

5. EXPERIMENTAL PLAN

In order to realize the BIST model, figure shown in 7 has been analyzed and scaled up on the evaluation board level as shown in figure 9. Newly built circuit consists of essential components that are in figure 6. One component that is being developing is BIST-compatible duplexer/diplexer which has been proposed in last Section. Central CDMA processor in figure 6 is realized using one of the DSP evaluation boards that has DAC, ADC and USB interface built in.

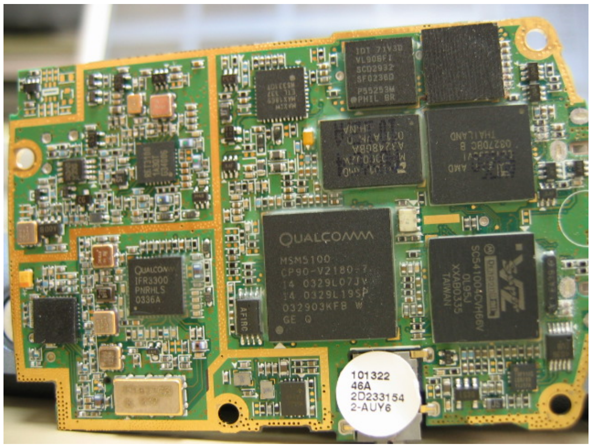

Figure 7. Typical Cellular Phone Board (8.3cm x 5.2cm)

Figure 8 illustrates the basic component to be used in order to implement actual RF circuit in a big scale.

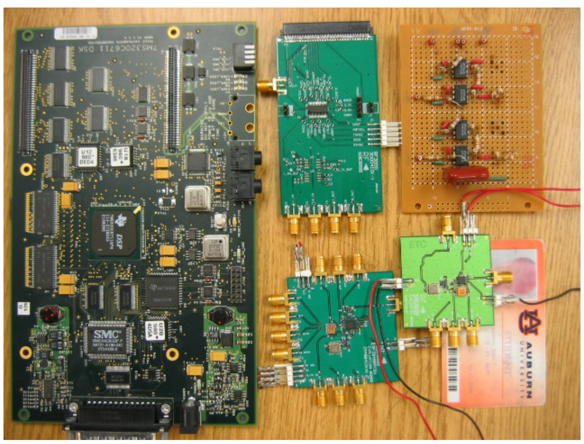

Figure 8. Actual RF component in evaluation board level (21cm x 26.5cm)

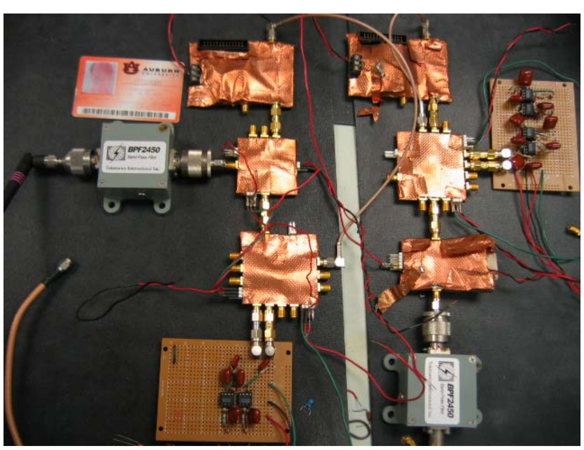

Figure 9. Implementing complete transceiver

As shown in figure 9, since antenna duplexer/diplexer was not implemented yet, both Tx and (Receiver) Rx implemented separately so that each one has its own antenna. Note that each RF evaluation board has wrapped with copper tape to prevent interference from the external noise.

Finally as suggested earlier, figure 10 shows the loop back path starting from DSP evaluation board (not shown in the picture) to DSP evaluation board itself by replacing two antennas with one wire.

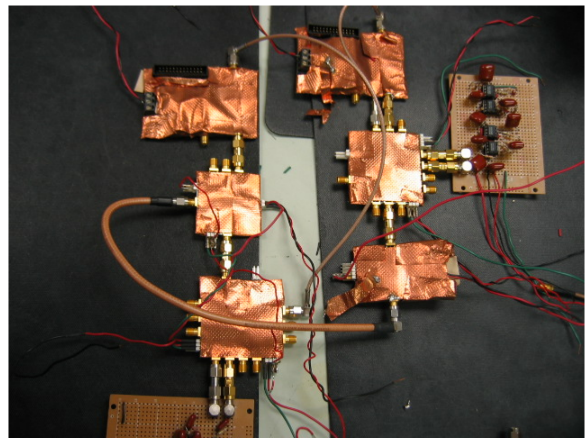

Figure 10. After Connect the Transmitter Output and Receiver Input by Replacing their Antennas with One Wire.

6. EXPECTING EXPERIMENTAL RESULT

Expecting result of the project will have the both aspects of work from [3] and [6]. When the functional test is done, output should be observed though JTAG interface so that we can scan out the ORA results after each test phase. The value then be read and analyze through the bit-error rate (BER) analyzer to characterize the good and bad transceiver circuit. Since it is hard to inject faults into the chip itself, RF simulator will be used to implement identical design and through the simulator we can inject faults to be compared to the expected results as shown in figure 11.

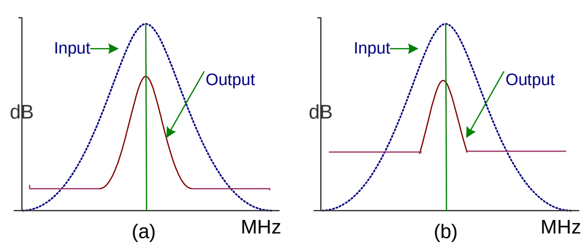

Figure 11. Expected Output for Good Transceiver (a), and of Faulty Output (b) due to Increased Noise Floor.

7. SUMMERY AND CONCLUSIONS

In this work, we proposed an improved BIST approach for the general RF mobile device. By testing complete transceiver at once will give us the highest level testing mechanism so that mobile users can test their phone in fairly fast and it may not be costly to the manufacturers as well. More accurate test can be done when embedded sensor outputs are analyzed by central mobile processor.

Thorough experiment have not been completed in this project due to the fact that accessing to the hardware resources are costly to graduate student, and the author's lack of thorough understanding in RF area. However, having the functional test and component specific measurement test together, with having modem processor that is capable of analyzing two kinds of data at the same time, innovative way of test mobile phone has been proposed because it gives even higher fault coverage and time savings than doing just one kind of test. Loop back BIST shown in [3] did not have high fault coverage and work in [6] had to use external test equipment to generate the test patterns which made it semi-BIST and all of these disadvantages from the earlier work had been solved by merging two method together. In addition, the new approach adds power amplifier and antenna duplexer/diplexer into the test path which were excluded in study [3] so that complete transceiver would be under one test path. Some drawbacks of the new approach seem to be found such that implementing right sensors for every test point takes lots of trial-and-error sequence. Implementing new duplexer/diplexer could be a major barrier due to the complexity of analog design itself. Currently, the new merged design is being implemented in hardware without the antenna duplexer/diplexer.

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