Comparison of power consumption of 4-bit binary counters with various state encodings including gray and one-hot codes

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***Abstract*—This study examines the power consumed by various 4-bit binary counters with different state encodings. The encodings considered are binary encoding, gray encoding and one hot encoding. The circuits are synthesized as CMOS gates and the transition power consumed in these circuits is analyzed, by hand calculations. The results show that counters with gray encoding consume less power than one-hot and binary encoding. It is also shown that one hot encoding consumes more power than binary encoding.**

I. Introduction

A COUNTER is a sequential logic circuit commonly used in the design of digital circuits such as processors. It is a finite state machine that moves through a predefined sequence of flip-flop states after every clock pulse. The predefined sequence of states is specified by their state encoding. In a binary encoded counter the states are given by the binary values of integers with the initial state being 0 and the ending state being the binary value of the number 2^n-1, where n is the number of flip-flops used. A gray code is designed in such a way that there is only one bit that changes from one state to the next. The number of states is given by 2^n, where n is the number of flip-flops or bits that define a state. A 4 bit gray code sequence is given by 0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 1100, 1101, 1111, 1110, 1010, 1011, 1001, 1000, and then back to 0000. The gray code used in this study is a one that has 16 states i.e., a 4 bit gray code counter. Another type of encoding considered in this study is a one hot encoding, which consists of n bits/flip-flops for n states where only one of them is a 1 in each of the n states. The one hot encoding counter considered for the study is of 16 states and consists of 16 flip-flops. These circuits are synthesized and their transition power consumption is estimated. Other components are not considered in this study. These gates are implemented as synchronous sequential circuits i.e., the circuits are allowed to change the state only at particular intervals of time specified by a clock pulse.

The transition power in a cmos circuit is the energy that is dissipated during a transition from a 0 to a 1 or a 1 to a 0 per one second. This constitutes a major section of the overall power dissipated in a CMOS circuit. The energy dissipated per transition by a CMOS gate is given by is given by the equation $\frac{1}{2}CV^2$ where C is the load capacitance at the output node of the gate. The total dynamic power is estimated by calculating the number of transitions that the circuit undergoes in one second, which in a synchronous circuit depends on the clock frequency at which the circuit operated and the activity factor. The activity factors of each gate and the load capacitance are calculated in order to estimate the power consumption of the counters in terms of the parameters in a technology so that comparison can be made between them.

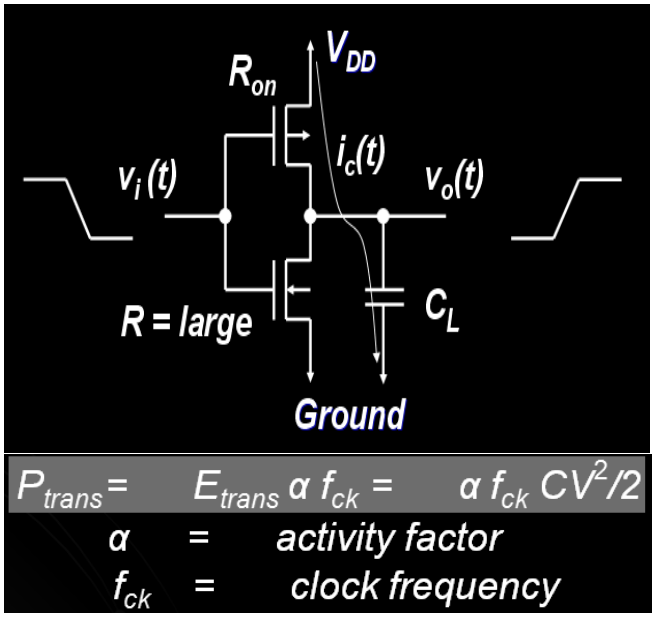


Figure 1:Fig. 1 CMOS Gate transition power

II. Circuit Synthesis

A. Binary and Gray code Counter Circuit:

The Binary counter and gray code circuit consists of 4 flip flops and the combinational logic circuit synthesized with NAND and NOT gates. Both the circuits differ only by their combinational logic blocks and both start from state 0000 by switching the reset signal to a high (logic 1).

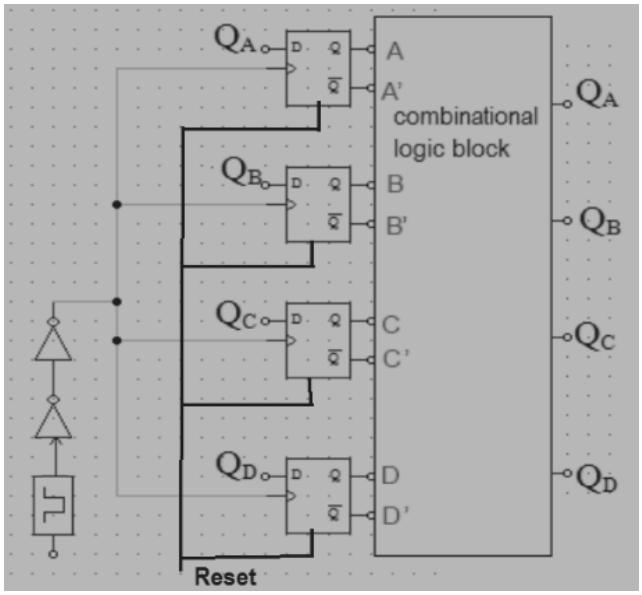


Figure 2: Binary and gray code counter circuit

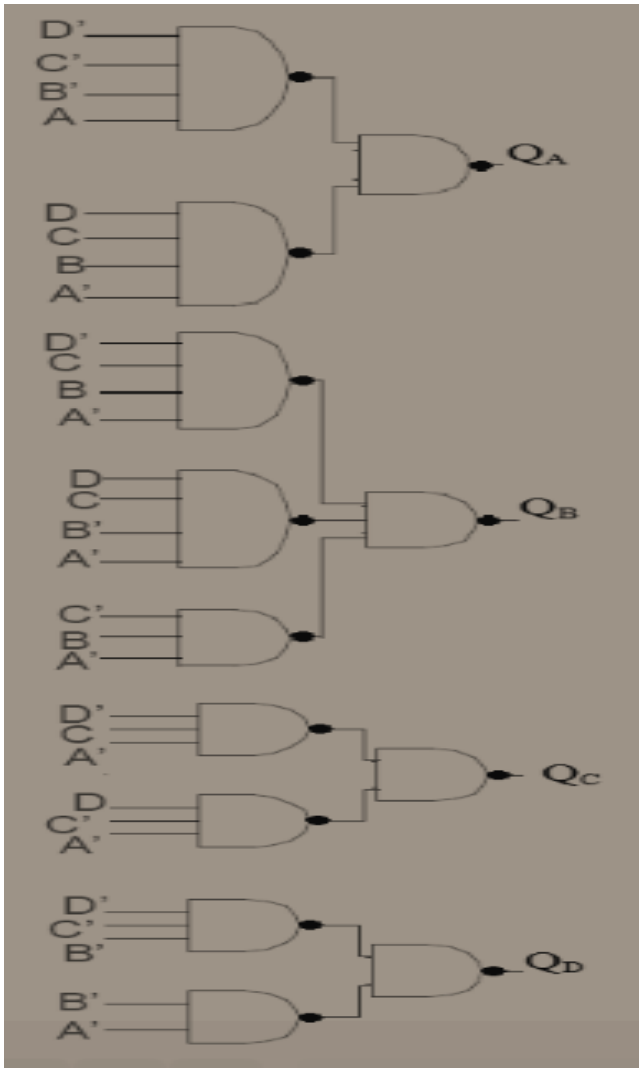


Figure 3: Conditional Logic block of binary counter

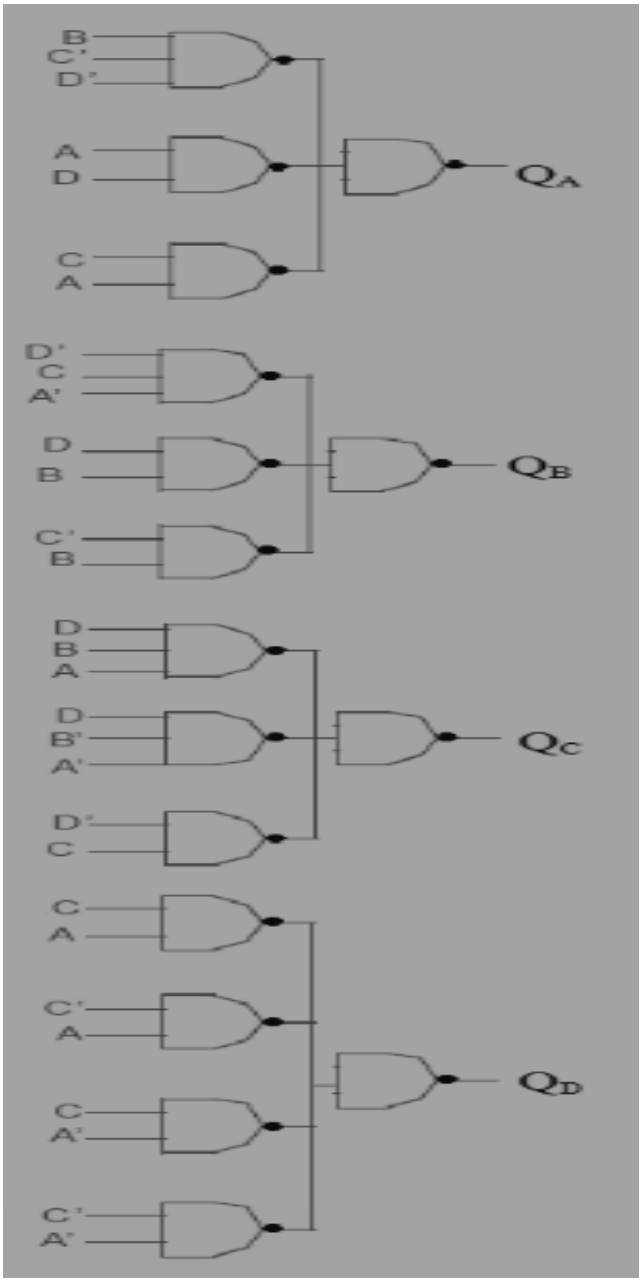


Figure 4: Combinational Logic block of Gray counter

B. One Hot Encoding circuit:

The one hot encoding circuit consists of 16 flip-flops and has no combinational logic gates. Each flip-flop's output is connected to the output of the other flip-flop. The circuit is reset to the initial state where the first flip-flop is 1, by giving a set (to logical 1) signal to the first flip flop and a reset signal to all other flip flops. The circuit also consists of 4 times as many flip-flops as the binary and gray code circuits. Since they all get the same clock, it might result in clock skew. In order to avoid it, an additional 4 clock drivers which are made of 2 inverters connected back to back are used. This improves the clock signal drive and reduces clock skew with careful design of the clock network.

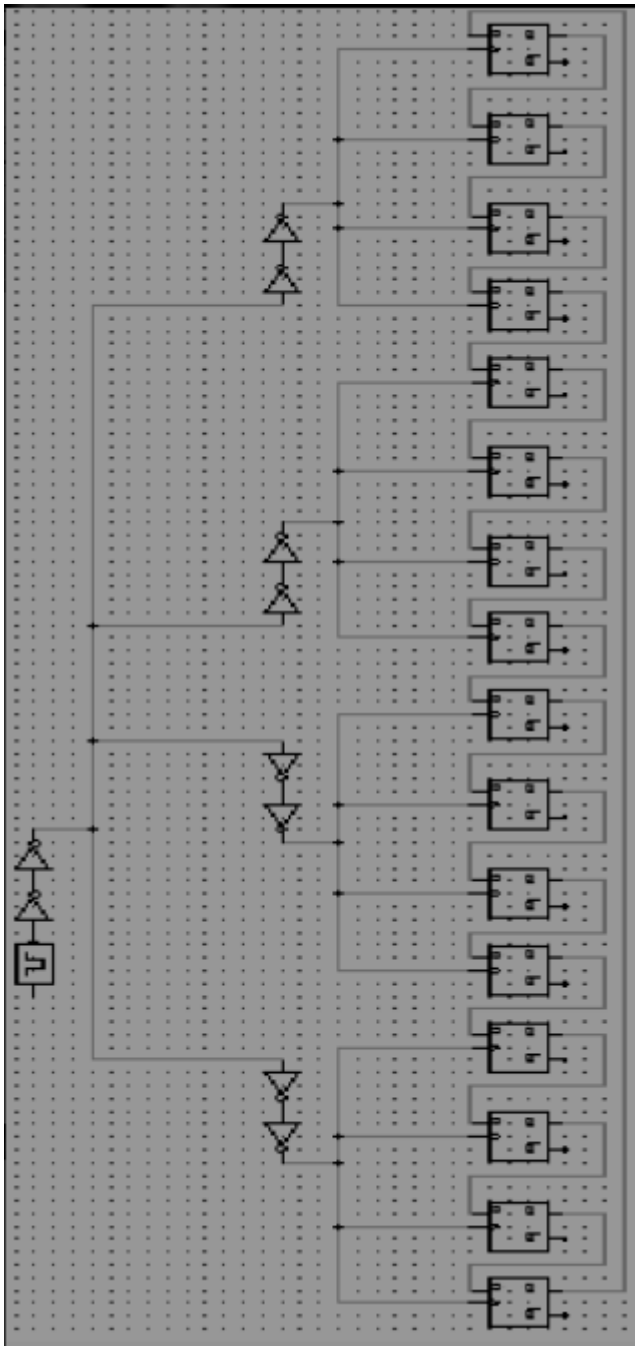
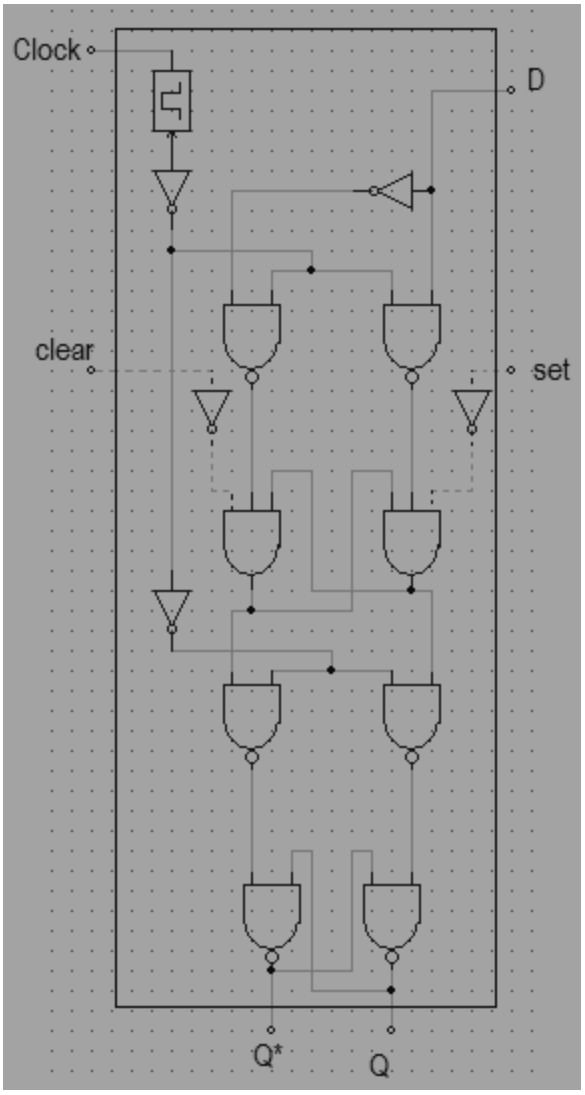


Figure 5: One hot encoding circuit

C. *D Flip-Flop circuit:*

The D flip flop circuit is also implemented with NAND and NOT gates. It is implemented in a master slave configuration to make the flip-flop switch at the rising edge of the clock signal. It is provided with either a set or reset signal. It does not have both the signals since only one of the 2 signals is needed. In binary and gray encoding all flip-flops need only reset signal but in one hot encoding, the first flip-flop has only the set signal where as the rest all of them have only the reset signal. The figure 6 shows a flip-flop used in a one hot encoded circuit and the reset and set signals are shown by dotted lines indicating that only one of them is used. Two inverters are provided to the clock to implement the master slave configuration.



III. Power Analysis

Power in a CMOS gate is given by $\frac{1}{2}\alpha f C V^2$ where f is the frequency, α is the activity factor, V is the voltage and C is the load capacitance. V and f are constant for each gate, but α and C may vary. Estimating these values for each gate will give the power.

A. *Estimation of activity factor:*

The activity for each gate is obtained by recording all the transitions that happen in the circuit as the circuit passes through all the 16 states. The numbers of transitions that a gate makes are tabulated. All the gates in the clock distribution network have an activity factor of 32.

B. *Estimastion of load capacitances*

The load capacitance in a CMOS circuit is due to various capacitive effects such as the gate to channel capacitance, gate source to substrate capacitance, drain to substrate capacitance and Miller capacitances like gate to source and gate to drain capacitances. Since the gates used are basic CMOS gates like NAND and NOT, these capacitive effects depend on the

number of inputs and outputs to a gate. Hence, the number of inputs and outputs can give an estimate of the capacitances.

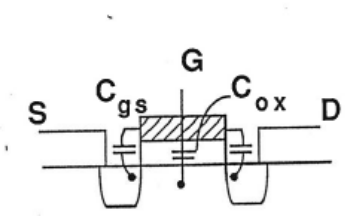


Figure 6: Showing gate to source cpacitance and gate to channel capacitance (shown as Cox)

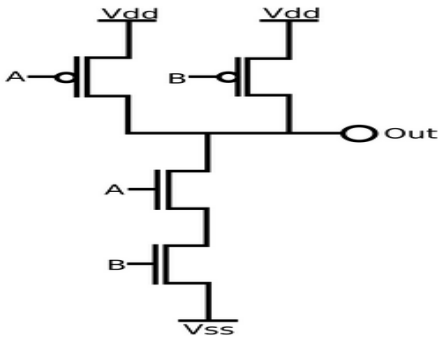


Figure 7: CMOS NAND gate

Most of the load capacitance is the parallel combination of gate capacitances due to fan-outs and the source to substrate as well as drain to substrate capacitance due to fan-ins. These components can be denoted as (fin+1)*Cin + 2*fout*Cout, where fin is the number of inputs to the gate and fout is the fan-out at the output of the gate. Cin is multiplied with fin+1 because the pull up circuit of the CMOS NAND gate will have fin number of transistors in parallel and these fin number of transistors will contribute to the load capacitance. Whereas in the pull down stage only one transit will contribute to the load capacitance, since the transistors in pull down circuit are in series. In total fin+1 transistors will contribute their capacitive effects. In figure 7 there are two inputs and hence 2 transistors are in parallel and contribute their capacitance effects to the load capacitance. Therefore 2 inputs contribute to 2+1=3 miller capacitances. Similarly, if the gate has only one fan-out, the output node acts as an to input to a single gate and will thereby be connected to 2 transistor gates, one in pull up and the other in pull down stage of the gate. Therefore the total number of transistors that contribute to the gate capacitances are fout*2. Since an Inverter can be considered as a NAND gate with only one input the same formula applies to the inverter.

The values of the co-efficients of Cin and Cout as calculated by the above given formula and the corresponding α values for all are tabulated as shown in the following table. The values are tabulated such that the activity factor is multiplied by 16, which is the number transitions at every gate when the gate goes through all the 16 states. This is done in order to get whole number. The final results are computed by dividing with 16 since all he terms have a 16 in them. Certain rows combine the gates with the same activity factor α.

logic circuit in gray code counter				
α *16	cin	cout	α *cin*16	α *cout*16
2	3	2	6	4
4	3	2	12	8
2	4	2	8	4
2	3	2	6	4
4	3	2	12	8
4	4	2	16	8
4	3	2	12	8
2	4	2	8	4
2	4	2	8	4
2	3	2	6	4
2	3	2	6	4
2	3	2	6	4
2	3	2	6	4
2	4	4	8	8
2	4	4	8	8
4	4	4	16	16
8	5	4	40	32
flip-flop circuit in gray code counter				
α *16	cin	cout	α *cin*16	α *cout*16
2	33	46	66	92
2	33	38	66	76
4	33	46	132	184
8	33	42	264	336
Clock distribution network in gray counter				
α *16	cin	cout	α *cin*16	α *cout*16
32	4	10	128	320
Logic cirucit in Binary counter				
α *16	cin	cout	α *cin*16	α *cout*16
2	5	2	10	4
2	5	2	10	4
2	4	2	8	4
2	5	2	10	4
2	5	2	10	4
4	4	2	16	8
4	4	2	16	8
2	3	2	6	4
4	4	2	16	8
2	3	4	6	8
4	4	4	16	16
8	3	4	24	32
16	3	4	48	64

Flip flop circuit in binary counter				
α *16	cin	cout	α *cin*16	α *cout*16
2	33	44	66	88
4	33	42	132	168
8	33	44	264	352
16	33	40	528	640
Clock network in binary counter				
α *16	cin	cout	α *cin*16	α *cout*16
32	4	10	128	320
Flip flop circuit in one hot counter				
α *16	cin	cout	α *cin*16	α *cout*16
16	33	32	528	512
Clock network in one hot counter				
α *16	cin	cout	α *cin*16	α *cout*16
32	20	50	640	1600

IV. Results and Concusion

The final results are shown in the table below:

	GRAY	BINARY	ONE HOT
combinational 16*α*cin component	184	196	0
combinational 16*α*cout component	132	168	0
flip-flop 16*α*Cin component	528	990	528
flip-flop 16*α*Cout component	688	1248	512
clocking circuit 16*α*cin component	128	128	640
clocking circuit 16*α*cout component	320	320	1600
total 16*α*Cin component	840	1314	1168
total 16*α*Cout component	1140	1736	2112

Usually the Value of Cin is taken to be equal to the value of Cout. But in practice Cout could be more than twice of Cin. SO the table shows values when Cout is both equal to and twice that of Cin :

	if Cout is equal to Cin		
	GRAY	BINARY	ONE HOT
power*16 coefficients	K* 1980	K* 3050	K* 3280
power	K* 123.75	K* 190.625	K* 205
	if Cout is twice of Cin		
	GRAY	BINARY	ONE HOT
power*16 coefficients	K* 2227.5	K* 3431.25	K* 3690
power	K* 139.21875	K* 214.453125	K* 230.625

In the above table, K is specified by the technology used.

We can conclude from the last row of the table that the gray code counter consumes the least power, followed by binary and then one hot encoded counter. One hot code counter might consume a little less power and become less power hungry than binary, if the clock distribution network in properly designed with less number of buffers and if clock gating is used.

References

[1] Dr. Vishwani D. Agrawal, Spring 2015 slides: ELEC6270 Low Power Design of Electronic Circuits.