Ring oscillator design in 32nm CMOS with frequency and power analysis for changing supply voltage

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***Abstract* — A 19-stage ring oscillator was designed and simulated using 32nm CMOS technology. The supply voltage was varied from 0.075V to 1.2V in order to examine the frequency and power consumption of the circuit. The measured frequency had a range of 19.7MHz to 15.3GHz and the power consumption varied from 0.338uW to 54.0mW. As expected, the frequency and power consumption increased with increasing voltage supply.**

Index Terms – ring oscillator, CMOS inverter, 32nm CMOS technology

I. Introduction

Oscillating signals are seen in all different types of electrical systems. An oscillating signal can be used as a clock signal in order to synchronize the operations of a digital electronic system. These signals can also be used in radio and communication systems [1]. Electronic oscillators are designed in order to create these signals. There are two main types of oscillators, linear/harmonic and nonlinear/relaxation.

A ring oscillator is a type of relaxation oscillator that contains an odd number of inverters creating a non-sinusoidal signal alternating between a high and low voltage [2]. The output of the last inverter is connected to the first inverter; the name "ring" oscillator comes from this detail. Ring oscillators are interesting for many reasons including its simple design, low operating voltage, and its low power consumption [1]. The last reason is especially important; by lowering the power consumption of the clock signal, the power consumption of the whole digital system is lowered. Changing the supply voltage can vary the power consumption of the ring oscillator, although this will also change the frequency of the circuit.

II. Design

LTspice was used to design and simulate the ring oscillator. The design contains 32nm CMOS transistors as the inverting delay gates. First, the CMOS inverter was designed as a symbol with 4 inputs/outputs (Vdd as supply voltage, In, Out, and DGND as digital ground). The spice model for the 32nm NMOS and PMOS, 32nm_MGK.txt, was included from ASU's predictive technology model website [3]. A schematic of the inverter is included in figure 1.

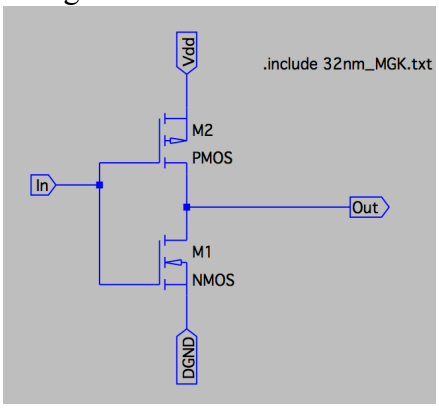

Figure 1: CMOS inverter

A symbol was created for the CMOS inverter so it could be easily duplicated. A single inverter was simulated in order to verify its performance. As shown in figure 2, the input of the inverter was connected to a voltage source (Vin) that varies from 0 to 1V. The supply voltage is set to 1V and the output voltage (Vout) is measured for the changing Vin shown in figure 3. As the input voltage increases, the output swings from a high voltage to a low voltage verifying the design of the inverter. Changing the supply voltage will cause the Vout to change its max value; for example, if the Vdd is set to 0.5V then the Vout will swing from 0.5V to 0V.

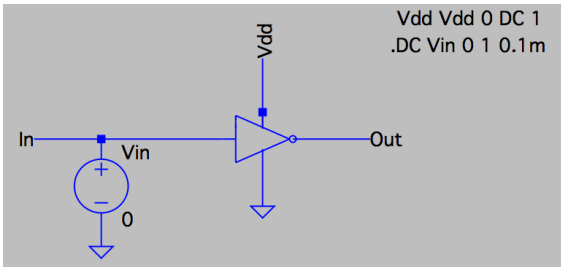

Figure 2: CMOS inverter circuit

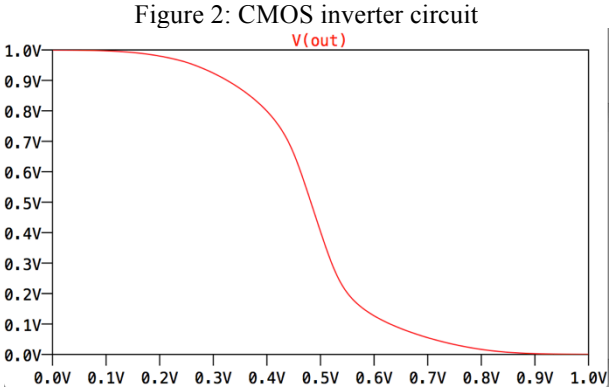

Figure 3: Vout vs. Vin of the CMOS inverter

Next the ring oscillator is design with 19 inverting gates. The output of the last inverter is connected to the input of the first inverter. The supply voltages (Vdd) are connected and assigned a changing value. The DGNDs are connected to ground and the output is labeled as Out. The schematic of the ring oscillator is shown in figure 4. The value, 19, for the number of gates was chosen because it needed to be an odd number and large enough to cause a delay when obtaining output voltages.

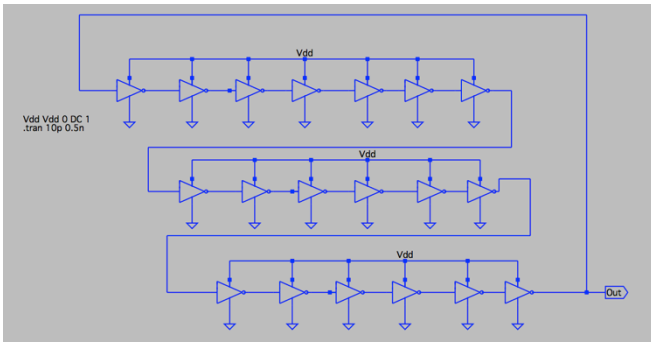

Figure 4: 19-stage Ring Oscillator

III. Simulation

The circuit was simulated in LTspice at first to check the oscillatory behavior. The supply voltage was set to 1V and the output was captured in figure 5. The figure shows the output alternating between 0 and 1V as expected. Once the circuit showed correct operations, the supply voltage was varied from 0.075V to 1.2V. This range was chosen because lower voltages would not produce an oscillating signal and higher voltages would produce a signal without reaching maximum voltage.

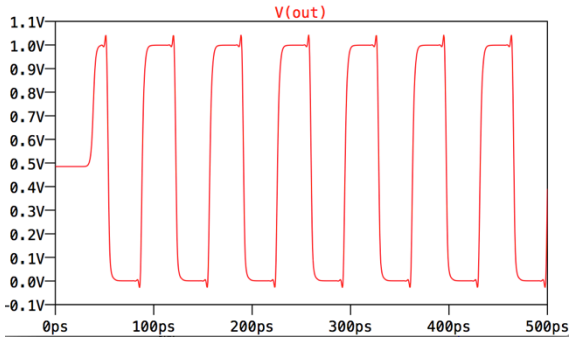

Figure 5: Ring oscillator output

Calculations for frequency and power consumption were then made for these Vdd values. Frequency is related to delay by equation 1, so the delay of one oscillation was measured for each Vdd value. Figure 6 shows the measured values of frequency and delay with changing Vdd. The frequency range of this simulated ring oscillator is 19.7MHz at 0.075V to 15.3GHz at 1.2V.

$$frequency = \frac{1}{delay} \qquad (1)$$

Vdd	Frequency (GHz)	Delay (ns)
1.2	15.3	0.065
1.1	14.9	0.067
1	14.3	0.070
0.9	13.3	0.075
0.8	11.97	0.084
0.7	10.0	0.100
0.6	8.79	0.114
0.5	6.22	0.161
0.4	3.46	0.289
0.3	1.30	0.769
0.2	0.23	4.348
0.1	0.0303	33.00
0.075	0.0197	50.76

Figure 6: Measured frequencies and delays

Vdd (V)	I (A) RMS	P (uW) one gate	P (mW) total
1.2	2.37E-04	284.4	5.4036
1.1	2.03E-04	223.3	4.2427
1.0	1.74E-04	174.0	3.3060
0.9	1.25E-04	112.5	2.1375
0.8	1.02E-04	81.92	1.5565
0.7	6.95E-05	48.65	0.9244
0.6	4.20E-05	25.20	0.4788
0.5	1.72E-05	8.60	0.1634
0.4	6.70E-06	2.68	0.05092
0.3	2.50E-06	0.75	0.01425
0.2	3.83E-07	0.0766	0.001455
0.1	4.10E-08	0.0041	7.79E-05
0.075	2.37E-08	0.00178	3.377E-05

Figure 7: Measured power consumption

Typically the power consumption of a CMOS inverter is calculated using equation 2 [4]. In this simulation, the load capacitance of the inverter was unknown so equation 3 was used instead. The RMS value of the current from the power supply was recorded at each voltage level.

Equation 3 gives the power consumption of a single CMOS inverter therefore the value is multiplied by the number of gates, 19, to obtain the power consumption of the entire circuit. Figure 7 shows the measured values for the RMS current and power consumption of one gate and the whole circuit. The power consumption of the ring oscillator varied from 5.4mW at a Vdd of 1.2V and 33.8nW at a Vdd of 0.075V.

$$Power = C * Vdd^2 * f \qquad (2)$$

$$Power = I(rms) * Vdd \qquad (3)$$

IV. Analysis

The simulation showed in figure 8 that voltage supply has a negative correlation with delay and a positive correlation with power consumption. These results agree with what was expected based on low power design concepts. Power consumption of a CMOS inverter is dependent on the supply voltage as shown in equation 2. Although frequency is also a factor and shows an increase as the supply voltage decreases, the overall power consumption is lowered due to the square of this lower supply voltage. The delay is also dependent on the supply voltage as shown in the alpha power law, equation 4 [5]. The delay will increase as Vdd decreases.

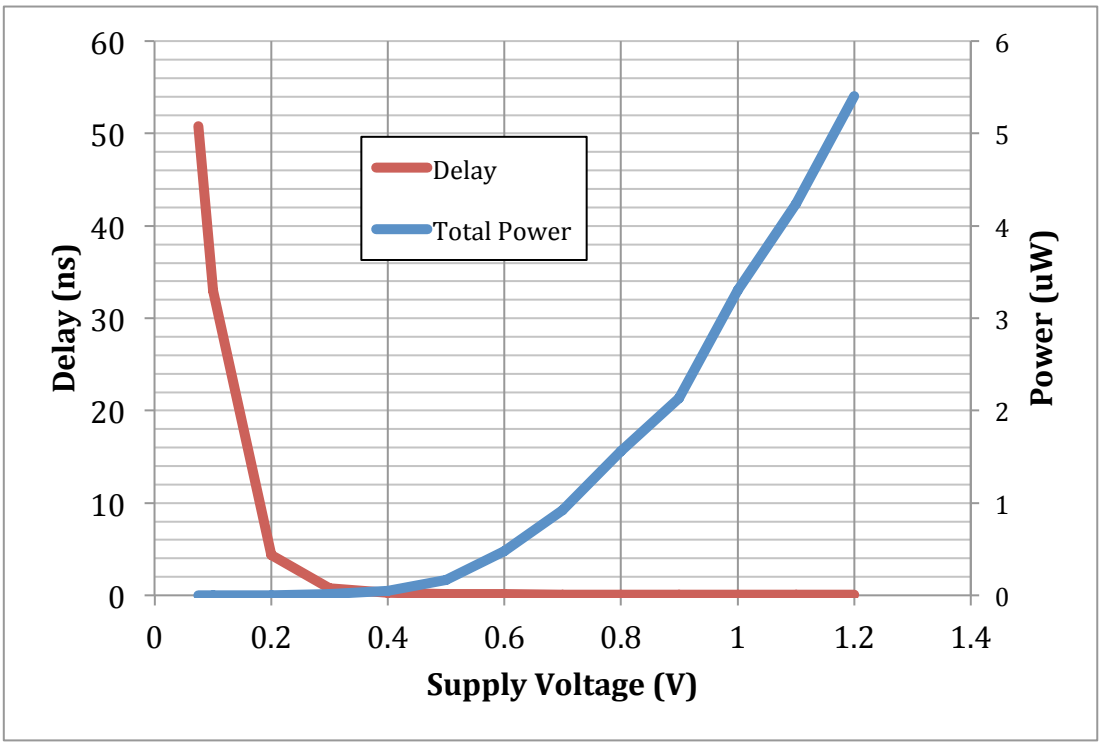

Figure 8: Delay and Power consumption vs. Supply voltage

$$delay \propto \frac{Vdd}{(Vdd - Vth)^{\alpha}} \qquad (4)$$

The effects of the supply voltage on the performance of the circuit are important to note when operating this ring oscillator. In order to lower the power consumption of the circuit, the supply voltage should be lowered, but lowering the voltage too much will cause a significant increase in delay. By choosing the right supply voltage, the ring oscillator can achieve great power savings with a small delay increase.

Figure 9 shows a clearer picture of the results from 0.2 to 0.6V. By looking at the graph, 0.4V seems like the optimal supply voltage value. Compared to a supply voltage of 1V, a Vdd value of 0.4 produced a power savings of 98% and a delay increase with a factor of 4.4. If the operators were more concerned with the delay instead of the power savings, the supply voltage would be set to 0.5V to achieve a power savings of 95% and a delay increase by a factor of 2.3.

The supply voltage could be further reduced to 0.075V and still operate correctly. This would provide a power savings of 99.9% but would also cause the delay to increase by a factor of 726, which would be unreasonable.

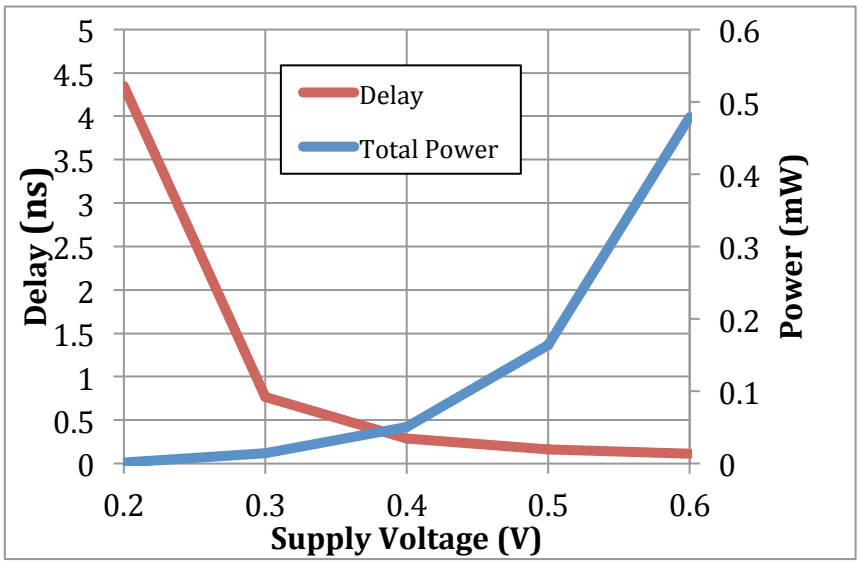

Figure 9: Delay and Power consumption for Vdd of 0.2-0.6V

V. Conclusion

A 19-stage ring oscillator was designed using 32nm CMOS technology and simulated in LTspice. The frequency, delay, and power consumption were measured for various supply voltage values. As the Vdd increased, the frequency and power consumption increased and the delay decreased. The frequency's range was measured to be from 19.7MHz to 15.3GHz. The optimal voltage supply was around 0.4 and 0.5V. These voltage levels would provide, respectively, a frequency of 6.22GHz and 3.46GHz, a delay of 0.16ns and 0.29ns, and a power consumption of 0.16mW and 51µW.

More research could be pursued in the future to lower the power consumption of the ring oscillator further. Different CMOS technologies, for example 22nm, could be investigated for frequency and power consumption. Also, other oscillators might consume less power while still maintaining a high frequency.

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