Effects of temperature and structural geometries on a skyrmion logic gate

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***Abstract*—We design a SkyMDILogic gate and use it as a model system to study the geometrical and thermal effects. We particularly focus on the effects of temperature and structural defects. Micromagnetic simulations are used to study the skyrmion movement and characterize the relevant properties. We also construct an equivalent circuit model to calculate the energy consumption and logic operations at different temperatures. We find that temperature significantly affects the stability of a skyrmion. At elevated temperatures, the skyrmion propagation is more robust against the pinning effect of structural defects. Our results highlight the effects of thermal and structural defects, which remained largely unexplored in previous logic gate designs.**

***Index Terms*—Spintronic logic, skyrmion logic gate, skyrmion memory, thermal fluctuations**

I. Introduction

Magnetic skyrmions represent a realizable topological magnetic texture in real space and can work as an ideal candidate for implementing novel logic designs and magnetic memories [1–3]. Skyrmions have been observed in various magnetic systems lacking inversion symmetry [1, 4]. They arise from the competition between Dzyaloshinskii-Moriya interaction (DMI) and perpendicular energy interactions, such as Heisenberg exchange, or a combination of various uniaxial anisotropy energy terms, or dipolar interaction in magnetic materials [5]. Skyrmions have many interesting properties, including nanometer diameters for high-density storage, room temperature stability, current-controlled motion, topological charge, and symmetry protection against large defects. Various logic and memory devices have been proposed based on the unique properties of skyrmions [5–10]. Many of these devices rely on the linear motion of skyrmions from the input to the output. Such skyrmion motion suffers from transverse deviation due to the skyrmion Hall effect and requires extra components to facilitate desired skyrmion propagation [9]. Recent findings show that such issues can be overcome by exploiting the interconversion of skyrmion-magnetic domain walls at the joining part of narrow and wide nanowires. This technique offers advantages such as lower driving electrical currents and higher speeds [11, 12]. Moreover, a recent study has shown that a skyrmion can be generated at a gigahertz (GHz) frequency through skyrmion-domain wall pair interconversion [5]. However, the effects of thermal and structural defects on the performance of skyrmion logic gates remain largely overlooked [13].

In this work, we design a logic gate based on skyrmion-magnetic domain interconversion (SkyMDILogic) and use it as a model system to study the dependences of skyrmion stability and velocity and skyrmion stability on elevated temperatures, structural defects, electrical current density, and magnetic damping. We also carry out circuit simulations at different temperatures. Our work paves the way to engineer skyrmion devices for practical computing applications. The primary contributions of this paper are summarized as follows:

- *Identify the impact of temperature on skyrmion propagation and logic gate performance.*
- *Demonstrate the SkyMDILogic performance with co-existing structural defects and temperature effects.*
- *Estimate the energy-delay product (EDP) of SkyMDILogic through temperature-dependent circuit simulations.*
- *Study the effects of current density and magnetic damping on the skyrmion propagation velocity and stability.*

In the following sections, we discuss the device structure and basic operation principles, the characterization of the SkyMDILogic properties, circuit modeling, and device performance evaluation.

II. Device Structure and Basic Operations

As shown in Fig. 1(a), the SkyMDILogic device comprises several components as follows: (1) The bottom section of the device is a specially-designed nanotrack that is patterned out of a bi-layer structure consisting of a CoFeB magnetic layer with perpendicular magnetic anisotropy (PMA), and a Pt heavy metal (HM) layer. The layers are chosen such that the strong DMI required for stabilizing skyrmions is realized. The dimensions of the device are annotated in Fig. 1(b). Two NMOS transistors, T_A and T_B, are used to generate skyrmion propagation currents at the input terminal. (2) A skyrmion initialization section, consisting of a magnetic tunnel junction (MTJ1) and a PMOS transistor T_{Init}, is used to create a skyrmion at the beginning of the logic operation. (3) At the output terminal, a second MTJ (MTJ2) and a PMOS transistor (T_{Read}) are used near the end of the device to sense the skyrmion.

The design principle of SkyMDILogic is inspired by the dynamic CMOS logic family. The device illustrated in Fig. 1(a) works as a two-input AND gate. The logic operation is performed in three separate phases as follows: Phase I is the

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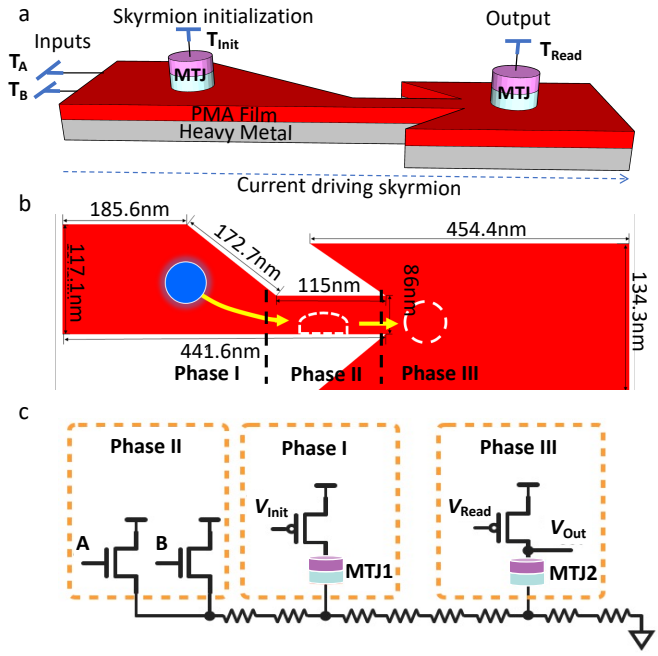

Fig. 1: A two-input AND SkyMDILogic gate structure and circuit model. (a) 3D view of the SkyMDILogic device structure. In the figure, the red/grey layers are perpendicular magnetic anisotropy (PMA) film/heavy metal (HM) film, respectively. MTJ1 is to nucleate a skyrmion and MTJ2 is for sensing the skyrmion. The pink and light blue layers in the MTJs represent a pinned magnet and MgO tunneling layer, respectively. T_A and T_B are both NMOS transistors for two-terminal inputs. T_{Init} is a PMOS transistor to generate skyrmions. T_{Read} is a PMOS transistor for skyrmion detection. (b) The geometry of the nanotrack and skyrmion-magnetic domain interconversion and propagation processes. (c) Resistive model and device operation phases. The resistors in series at the bottom represent the resistances of the heavy metal layer.

skyrmion nucleation phase (Skyr-Nuc Phase). If a voltage V_{Init} is applied to the T_{Init} transistor such that $V_{Init} < V_{Th}$, where V_{Th} is the threshold voltage of T_{Init} and since T_{Init} is a PMOS transistor, current flows into MTJ1 and a skyrmion is created in the nanotrack. This initiates the logic process, which is similar to the precharge phase in the dynamic logic of CMOS gates.

Phase II is the skyrmion propagation phase (Skyr-Prop Phase). Two input voltages are applied to the two input NMOS transistors T_A and T_B (the outputs of other gates can be used as inputs for cascading). Depending on the applied input voltages, currents can flow from T_A and T_B into the HM layer. If the summation of the two currents exceeds the threshold for skyrmion propagation, the skyrmion (created in Phase I) will travel from the input terminal, through the bridge, to the readout terminal due to the spin Hall effect. As the skyrmion propagates longitudinally along the nanotrack, it also experiences a transverse motion due to skyrmion-edge repulsion from the sloped upper boundary [6, 9]. As demonstrated in Fig. 1(b), this repulsion force pushes the skyrmion down and squeezes it into a magnetic domain and through the bridge, as indicated by the broken-line circles. After the magnetic domain passes the bridge, it gradually nucleates back into a new skyrmion and moves toward MTJ2 [5].

Phase III is the skyrmion detection phase (Skyr-Det Phase). For skyrmion detection, a PMOS transistor T_{Read} is connected to MTJ2. T_{read} can be used for readout and logic cascading [14]. During the non-reading time, V_{Read} remains HIGH and the PMOS T_{Read} is turned off, therefore the output voltage V_{Out} is LOW (Logic "0") due to the low MTJ magnetoresistance ($R_{MTJ,LOW}$ = 1 kΩ). During the Skyr-Det Phase, V_{Read} is LOW, thus, the PMOS T_{Read} is turned on. The output node voltage is detected by the presence of a skyrmion beneath MTJ2. If no skyrmion is present, then the pull-down nodes will still exhibit a low resistance, leading to a LOW (Logic "0") output. On the contrary, if a skyrmion arrives at the output, it will be detected by MTJ2. By setting the magnetization direction of the pinned magnet to be the opposite direction to that of the skyrmion, a high magnetoresistance ($R_{MTJ,HIGH}$ = 3 kΩ) can be expected. This will lead to a HIGH output voltage at the output node V_{Out}, representing logic "1". The Skyr-Det Phase is similar to the evaluation phase in CMOS dynamic logic. The three phases are shown in Fig. 1(c), which will be discussed in Section IV circuit modeling.

To analyze the dynamic behaviors of skyrmions in our design, we performed micromagnetic simulations using Object Oriented Micromagnetic Framework (OOMMF), which is a public micromagnetics program developed at the National Institute of Standards and Technology [15]. In the OOMMF simulations, an HM/PMA-magnet bilayer device was used, with a configuration that is similar to previous studies [6, 9]. Table 1 summarizes the parameters used in the simulation, which we have adopted from Ref. [9]. The current-induced skyrmion motion is modeled by the Landau-Lifshitz-Gilbert equation with spin-transfer torque terms as shown below [16]:

$$\frac{d\mathbf{m}}{dt} = -|\gamma|\mathbf{m}\times\mathbf{H}_{eff} + \alpha(\mathbf{m}\times\frac{d\mathbf{m}}{dt}) + |\gamma|\beta\varepsilon(\mathbf{m}\times\mathbf{m}_p\times\mathbf{m}) - |\gamma|\beta\varepsilon'(\mathbf{m}\times\mathbf{m}_p) \quad (1)$$

where $\mathbf{m}$ is the magnetization, $\mathbf{m}_p$ denotes the electron polarization direction, α is the Gilbert damping constant, γ is the gyromagnetic ratio, $\beta = |\frac{\hbar}{\mu_0 e}|\frac{J}{tM_s}$, and ε and ε' are functions of $\mathbf{m}$ and other constants. In our simulation, we consider an interfacial DMI at the HM/PMA-magnet interface. For the simulation, the corresponding DMI extension module has been added to the OOMMF software [17].

Table 1. Device Simulation Parameters

Parameter	Value
Gilbert damping factor	0.25
Spin Hall Angle θ_A	0.4
Saturation magnetization M_s	5.8×10^5 A/m
DMI Constant D	3.5 mJ/m^2
Perpendicular magnetic anisotropy K_u	0.9×10^6 J/m^3
Exchange stiffness A_{ex}	1.5×10^{-11} J/m
Mesh Size $d_x \times d_y \times d_z$	2 nm × 1 nm × 1 nm
PMA Film Resistivity	1.7×10^{-7} Ω·m
HM Film Resistivity	1.06×10^{-7} Ω·m
MTJ HIGH Resistance	3 kΩ
MTJ LOW Resistance	1 kΩ
Nucleation Time	5 ps
Propagation Time	3 ns
Read Time	3 ns
Nucleation Current	565 μA
Driving Current	70 μA

The AND gate operations are illustrated by the micromagnetic simulation graphs in Fig. 2. Two inputs, A and B, each equaling either logic "1" or logic "0", are applied to the input NMOS transistors T_A and T_B. Here, a logic "0" input means applying zero voltage (V_{Low}), and logic "1" input means applying a high voltage (V_{High}) to turn on the transistor. When an input transistor is turned on, it provides a current with density $J = 1 \times 10^{11}$A/m^2. Fig. 2(a) shows the time evolution of the skyrmion motion for three input cases: (1) A = "0", B = "0"; (2) A = "1", B = "0"; (3) A = "0", B = "1". In all of these cases, the electric current density is below the threshold $J_{prop} = 2 \times 10^{11}$A/m^2 required to drive a skyrmion to the output. The repulsion from the sloped upper boundary exerts a strong Magnus force on the skyrmion, squeezing and pushing it toward the bottom of the structure, as shown in Figs. 2(a_1-a_4). However, the skyrmion remains at the entrance of the bridge location when the operation is finished. In these cases, no skyrmion is detected at MTJ2; thus, the output reads a low magnetoresistance and stays LOW, with a corresponding output logic signal "0". Fig. 2(b) shows the case when A = "1" and B = "1". In this case, the total current density is 2×10^{11}A/m^2, which equals J_{prop}. Thus, the current is strong enough to drive the skyrmion to MTJ2, resulting in the logic signal "1". The total time for skyrmion propagation is t = 3 ns.

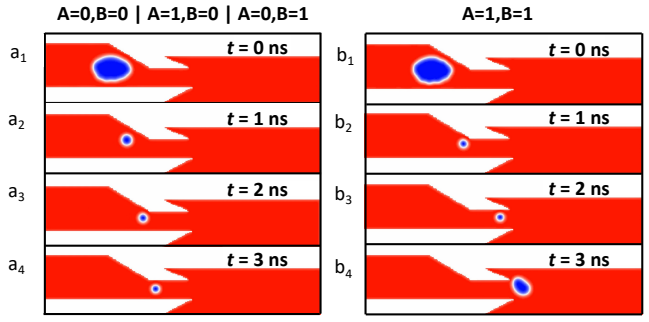

Fig. 2: Micromagnetic simulations of the AND logic gate. (a_1-a_4) For the three cases (1) A = "0," B = "0," (2) A = "1," B = "0," and (3) A = "0," B = "1," the skyrmion does not reach the output, thus output C = "0." (b_1-b_4) When A = "1," B = "1," the skyrmion reaches the output, thus C = "1."

It should be noted that our design can be used to realize other logic operations as well. Fig. 3 shows a sketch of the NAND gate comprising an AND gate cascaded with an inverter. The operation of the AND gate is illustrated above. The inverter works similarly to the AND gate, except that the pinned magnet in MTJ4 at the output of the inverter has the same magnetization as the skyrmion. Thus, a low magnetoresistance can be expected when a skyrmion appears. In this regard, a HIGH V_{Out1} signal leads to a LOW V_{Out2} signal, and vice versa. Since the NAND gate is a universal gate, all other gates can be constructed using a combination of NAND gates.

III. Characterization of SkyMDILogic Skyrmion Properties

We start by investigating the effects of temperature on the shape and stability of the skyrmions. Fig. 4. shows the temperature dependence of the skyrmion stability and skyrmion

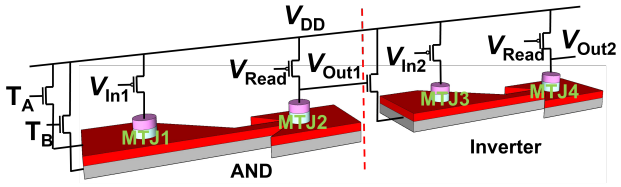

Fig. 3: NAND gate comprising an AND gate cascaded with an inverter.

propagation velocity. The velocity is calculated as $v_{skrymion}$ = propagation distance/propagation time. In Fig. 4(a), the damping constant is 0.25, the current density $J = 2 \times 10^{11}$A/m^2, and the driving current pulse is 3 ns. From the results, the following was observed. First, the skyrmion maintains the circular shape at lower temperatures but deforms into a U-shape magnetic domain above 142 K (Fig. 4(a)). The stabilization of the skyrmion depends on the balances of different energies, such as exchange energy, anisotropy energy, thermal energy, etc. Higher temperatures can lead to spin perturbations and destabilize a skyrmion [18, 19]. To improve the working temperature range, we have carried out simulations with different parameters. We have found that if both the anisotropy constant K_u and the DMI constant D are increased (e.g. $K_u = 1.1 \times 10^6$ J/m^3, $D = 3.8$ mJ/m^2 at 300 K), the skyrmion can be stabilized at a higher temperate, as shown in Fig. 4(b). While temperature strongly affects the skyrmion stability, the skyrmion propagation velocity is largely unperturbed by temperature, as shown in Fig. 4(c). Thus, we conclude that increased temperatures can hinder the expected behaviour of our design, but not its performance (i.e. propagation velocity). Our results highlight the importance of temperature considerations in designing skyrmion-based logic gates.

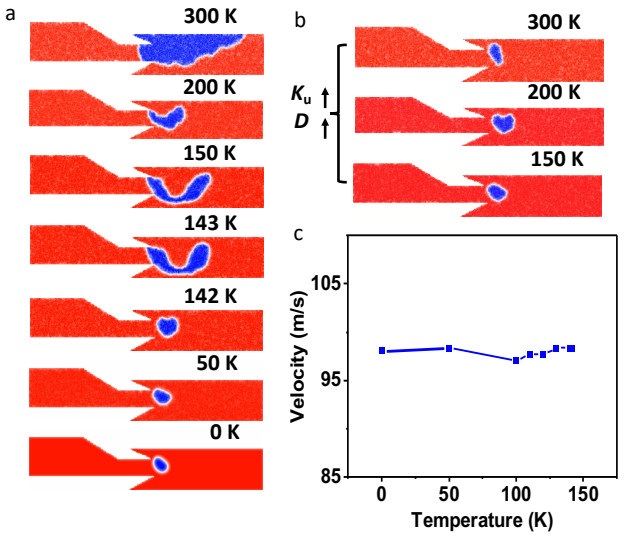

Fig. 4: (a) Skyrmion movement and shape evolution at different temperatures. (b) Stabilization of the skyrmion at higher temperatures. (c) Dependence of the skyrmion propagation velocity on temperature.

Next, we introduce several structural defects (notches) into SkyMDILogic to study their effects on the skyrmion propagation at different temperatures. Fig. 5 shows the simulation results of structural defects on the logic gate functions at 0 K, 100 K and 142 K, respectively. In Figs. 5(a_1,b_1,c_1), a top-

notch in the middle of the bridge is studied. In this case, the skyrmion tends to move up in the bridge due to the skyrmion Hall effect. This makes it move toward the top notch and gets pinned by it. At T = 0 K, the skyrmion disappears at the bridge boundary at t = 3.2 ns. At 100 K and 142 K, the skyrmion still exists, though it does not have enough energy to get depinned from the top notch. In Figs. 5(a_{2-3},b_{2-3},c_{2-3}), notches are introduced into the bottom boundary of the bridge structure. At T = 0 K, the skyrmion is again not able to pass the bridge to the output due to the significant notch pinning effect (Figs. 5(a_{2-3})). As T increases to 100 K, the skyrmion can overcome the strong notch pinning effect and move toward the output region (Figs. 5(b_{2-3})). At T = 142 K, as shown in Figs. 5(c_{2-3}), the raised temperature adds more energy to the skyrmion and drives it further. The results shown in Fig. 5 indicate that an elevated temperature can help overcome the structural defects and increase the propagation velocity due to more energy being generated from thermal fluctuations, which facilitates the skyrmion propagation process in the presence of defects.

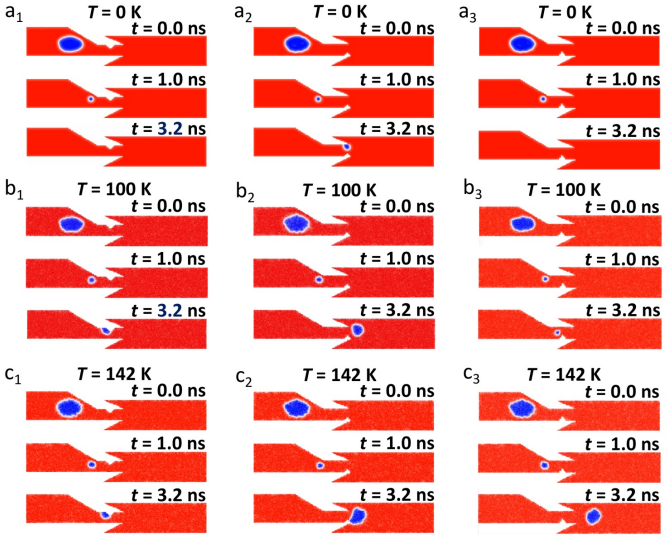

Fig. 5: Effect of geometrical defects on skyrmion movement and shape evolution at (a) 0 K, (b) 100 K, and (c) 142 K.

We then study how geometrical variation affects the skyrmion propagation in the AND gate. Fig. 6 shows simulations of skyrmion propagation in structures with different upper boundary slope angles and bridge lengths. Figs. 6(a_{1-2}) show the effect of the input slope angle change. Compared to the original design, where the input slope angle is 30°, reducing the input slope angle by 10° lowers the propagation velocity slightly (Fig. 6(a_1)). This is a result of the more gradual squeezing of the skyrmion into the bridge. As shown in Fig. 6(a_2), the 10° increment leads to the annihilation of the skyrmion at the entrance of the bridge due to skyrmion-edge interaction [20]. Figs. 6(b_{1-2}) show the effect of the output slope angle change. Reducing the output slope angle by 5° leads to the annihilation of the skyrmion. The reduction of the output slope angle shortens the distance between the input and output sloped structures, thus, leading to a stronger skyrmion-edge interaction to impede its movement. On the other hand, as the output slope increases by 15°, it pins the skyrmion at the right end of the bridge. Figs. 6(c_{1-4}) study the effect of the bridge length. As one can expect, when the length increases (reduces), the skyrmion needs more (less) time to propagate through the bridge. Based on our simulations, we see a linear relationship between the skyrmion propagation time and bridge length as shown in Fig. 6(d). Therefore, the bridge length significantly affects the propagation time.

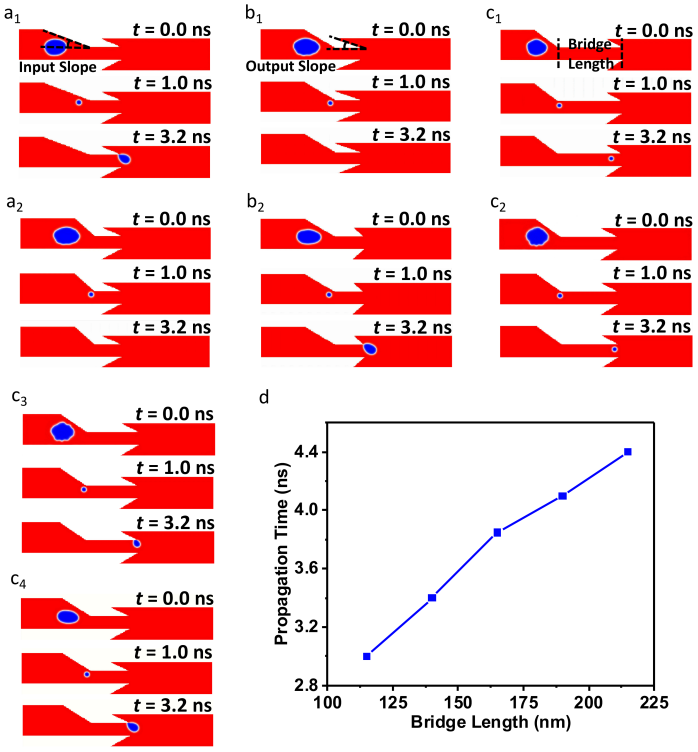

Fig. 6: Skyrmion propagation with different geometrical parameters. (a) Effect of input slope angle by -10° (a_1) and +10° (a_2). (b) Effect of output slope angle by -5° (b_1) and +15° (b_2). (c) Effect of bridge length (c_1 = 215 nm, c_2 = 190 nm, c_3 = 165 nm, c_4 = 140 nm). (d) Skyrmion propagation time vs. bridge length.

After that, we analyze the effects of varying the input current density and the PMA magnetic damping constant on the shape of the skyrmion in our AND gate. Fig. 7 shows the skyrmion movement and evolution as a function of driving current density, respectively. In Fig 7(a), the driving current pulse was set to 1 ns. The damping constant was set to the default value of 0.25. One can see that (1) a higher current density moves the skyrmion further, and (2) the skyrmion evolves into multiple magnetic domains beyond $J = 5 \times 10^{11}$A/m^2. This sets the maximum current density that is allowed in the SkyMDILogic device. Fig. 7(b) plots the skyrmion propagation velocity as a function of current density. The results indicate that the velocity of a skyrmion evolves with the current density; a higher current density will lead to a faster skyrmion motion, which is consistent with previous studies [21].

Similarly, we discuss how the damping constant α affects the skyrmion propagation velocity. Fig. 8 shows the skyrmion movement and evolution images as a function of damping constant. Fig. 8(a) shows the skyrmion movement and evolution with different damping constants at a fixed current of 2×10^{11}A/m^2 pulsed for 1.4 ns. One can see that when α = 0.1, the skyrmion is pinned at the end of the bridge. Our other

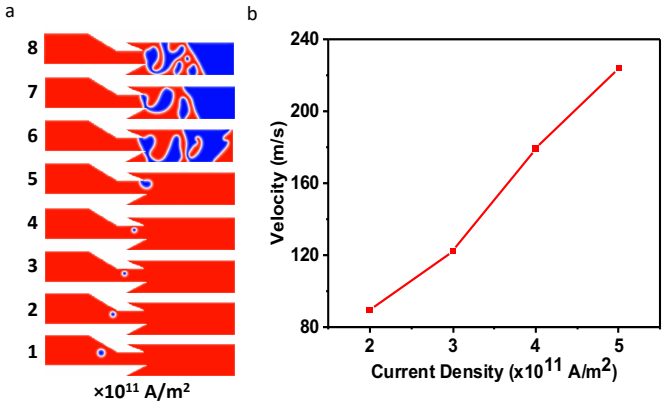

Fig. 7: (a) Skyrmion movement and shape evolution at different current densities. (b) Dependence of skyrmion propagation velocity on current density.

simulations show that the skyrmion can propagate through the bridge when $\alpha \geq 0.2$. Our results in Figs. 8(a,b) suggest that an operational sweet spot for α must be chosen for the successful propagation and reconstruction of the traveling skyrmion. α must be high enough to stabilize the skyrmion but low enough to allow for the skyrmion propagation through the bridge at reasonable velocities.

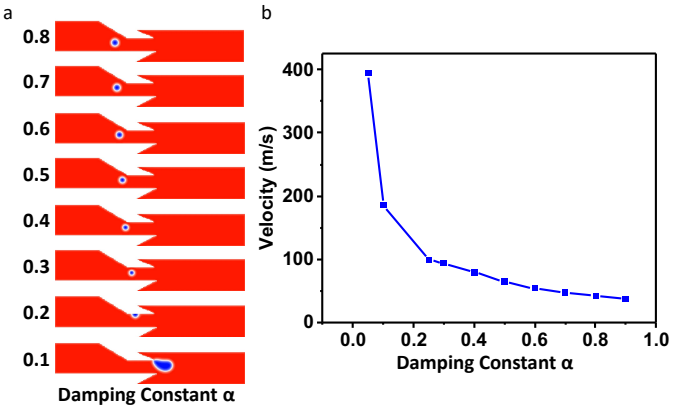

Fig. 8: (a) Skyrmion movement and shape evolution at different damping constants. (b) Dependence of skyrmion propagation velocity on damping constant.

Thus, in future skyrmion-based logic gate designs and manufacturing processes, careful consideration of geometrical parameters, structural defects, operational current densities, thermal effects, and the magnetic damping constant must be taken to ensure optimal operation speeds and device stability. A resistive circuit model representation of our device will help determine what operation speeds and power consumption can be reasonably expected from our design and will be discussed in the following section.

IV. Circuit Modeling and Performance Evaluation

To evaluate the timing and energy performances for SkyMDI-Logic, we build an equivalent circuit model, illustrated in Fig. 1(c), as proposed in Ref [22]. The different device parameters, including resistances of MTJ and nanotrack, the timing (skyrmion nucleation and propagation times), as well as the required current densities for skyrmion nucleation and propagation were all extracted from the OOMMF simulations discussed in Sections II and III. The circuit simulation parameters are listed in Table 1. These parameters, along with the geometry of the proposed device, were converted into equivalent circuit element values for SPICE simulations. Table 1 lists all the parameters used. For transistor modeling, we adopt a 16 nm HP predictive technology model (PTM) [23] for our implementation.

From the OOMMF simulations, the critical current density required for skyrmion nucleation is found to be 5×10^{11}A/m^2 for Phase I (Skyr-Nuc Phase). Combining the geometry information of the proposed device, this is equivalent to a critical current of $I_{\text{sky-nuc}} = 565$ μA needed to nucleate a skyrmion by MTJ1. Though the nucleation time in MTJ1 is 1.5 ps from the OOMMF simulations, during the circuit simulation, a longer V_{Init} pulse is recommended; therefore, a 5 ps nucleation current pulse was used, activating the PMOS T_{Init} and ensuring skyrmion nucleation through MTJ1.

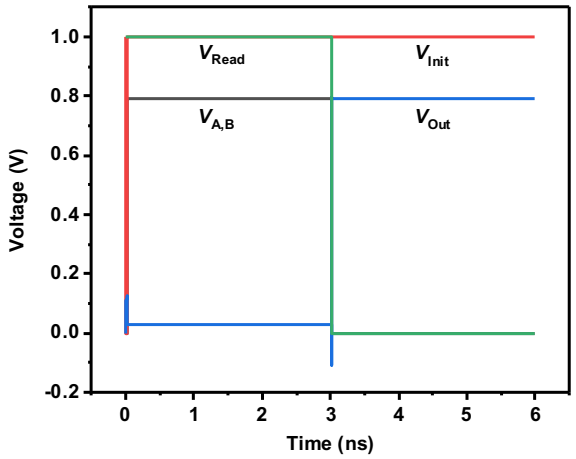

Fig. 9: Transient simulation results of SkyMDIlogic AND gate voltage waveforms.

In Phase II (Skyr-Prop Phase), the two input voltages V_{A} and V_{B} are pulsed for $t_{\text{Skyr-Prop}} = 3$ ns to ensure sufficient time for the skyrmion to propagate from the MTJ1 site, through the bridge, and into the MTJ2 site. As discussed in Section II, each input of the AND gate provides $J = 1 \times 10^{11}$A/m^2; this leads to a total driving current of $I_{\text{Skyr-Prop}} = 140$ μA (each input contributes 70 μA) in the nanotrack.

In Phase III (Skyr-Det Phase), V_{Read} is turned to LOW for $t_{\text{Read}} = 3$ ns, activating PMOS and ensuring the detection of the skyrmion, as well as passing the result to the input of the next gate. Once the skyrmion successfully reaches MTJ2 (or without a propagating skyrmion due to LOW inputs), V_{Read} was set to LOW and turned on the PMOS transistor for reading. If a skyrmion is present (absent) underneath MTJ2, V_{Out} reads HIGH (LOW), as discussed in detail in Section II. V_{Init}, V_{A}, V_{B}, and V_{Read} signals are summarized in Fig. 9.

It should be noted that the output voltage of the AND gate should be appropriate for cascading to a consecutive logic gate input, i.e. the NMOS transistor input of the next gate. As a result, this HIGH voltage should be high enough to ensure the ON current for the next stage NMOS transistor for input signals. Moreover, to ensure the skyrmion propagation in the gate of the next stage, the skyrmion detection time in

the detection phase (Skyr-Det Phase) should be at least equal to the skyrmion propagation time. Taking those conditions into consideration, we use 3 ns for the propagation current in the SPICE simulation of the AND gate. Fig. 10 shows the nucleation and propagation current profiles.

The above discussion summarizes reasonable operation times and parameters for the SkyMDILogic and its equivalent circuit, as well as the optimization procedures for the MTJs. We considered the circuit modeling at 50 K. It is found that the modeling results vary by 2-3 % between 0 K and 142 K. Taking into consideration the resistances, transistors sizing, and pulse widths, a conservative estimation of our AND gate delay is approximately 6 ns. As mentioned previously, we used a 16nm HP PTM model to simulate the circuit in the SPICE simulation. The power consumption of this AND gate is 170 μW and the energy consumption is 1.24 pJ (in a 6 ns window). The EDP is evaluated to be 3.7×10^{-21} Js. Considering that most skyrmion-based logic designs have not performed circuit-level simulations or evaluated EDPs [5–9], our work provides a more comprehensive study on skyrmion logic gate performance.

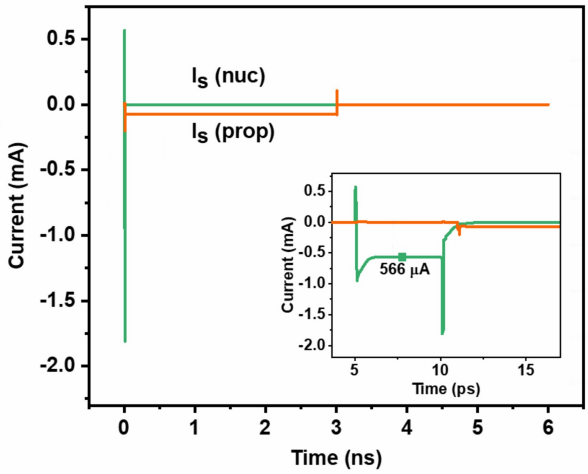

Fig. 10: Transient simulation results of SkyMDILogic AND gate Skyrmion nucleation and propagation currents.

SkyMDILogic has several unique advantages. The write current is much lower than most of the previous skyrmion and domain wall-based logic designs while achieving a high skyrmion movement velocity [5, 6, 9, 11–13]. A low writing current is helpful to improve the lifetime of the device. In addition, SkyMDILogic has a simple design, and does not require extra structures to avoid the transverse motion of skyrmions [9, 13]. Moreover, SkyMDILogic uses a single skyrmion for the logic operation and is not subject to requirements such as multi-skyrmion synchronization [12].

V. Conclusion

In this work, we design a logic gate based on skyrmion-magnetic domain interconversion (SkyMDILogic) and use it as a model structure to study the effects of elevated temperatures and structural defects on speed and skyrmion stability using various geometrical and magnetic parameters. We have found that elevated temperatures can significantly disrupt skyrmion stability. On the other hand, the elevated temperature can help with the depinning of magnetic domains in the presence of structural defects, thus improving the propagation process. The energy-delay product is estimated to be 3.6×10^{-21} Js at 50 K, and it differs by 2-3 % at different temperatures. Our findings have paved the way for developing skyrmion-based logic gates, which suggest that thermal effects and structural defects need careful consideration to ensure optimal operation speeds and device stability.

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