Ujjwal Guin, Ph.D., IEEE Senior Member

Last update on December 7, 2023

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RESEARCH INTERESTS

- Hardware Security for traditional and 2.5D/3D ICs
- Supply Chain Security and Blockchain
- Cryptography and Post-Quantum Cryptography
- Post-CMOS Technologies
- VLSI Design & Test

ACADEMIC APPOINTMENTS

- Associate Professor, Dept. of Electrical and Computer Engineering, Auburn University, AL, 2023-Present
- Assistant Professor, Dept. of Electrical and Computer Engineering, Auburn University, AL, 2016-2023

EDUCATION

- **Ph.D.**, Electrical Engineering (EE), University of Connecticut, CT, USA, 2011-2016
- **M.S.**, Electrical and Computer Engineering (ECE), Temple University, PA, USA, 2008-2010
- **B.E.**, Electronics & Telecomm. Engineering (ETC), Bengal Engr. and Science Univ., India, 2000-2004

PROJECT SPONSORS

- Air Force Office of Scientific Research (AFSOR)
- United States Secret Service (USSS)
- National Science Foundation (NSF)
- Air Force Research Laboratory (AFRL)
- United States Army
- Auburn University

GRANTS AND CONTRACTS (PI AND CO-PI)

- External Contracts/Grants Received or In-Force: $4,084,465 (My Share: $2,032,105)
- Available upon request.

AWARDS AND HONORS

- Best Paper, "*Beware of Discarding Used SRAMs: Information is Stored Permanently,*" IEEE Physical Assurance and Inspection of Electronics (PAINE), 2022.
- Best Paper Nomination, "*Defect Characterization and Testing of Skyrmion-Based Logic Circuits,*" VLSI Test Symposium (VTS), 2021.
- NSF CISE Research Initiation Initiative (CRII), 2018.
- Most Downloaded Article, U. Guin, D. DiMase, and M. Tehranipoor, "*Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead*", Journal of Electronic Testing: Theory and Applications (JETTA), 2014.

- Best Poster Nomination, "Low-cost On-Chip Structures for Combating Die and IC Recycling", PhD Forum at DAC, 2014.
- Best Student Paper Award, U. Guin and M. Tehranipoor, "*On Selection of Counterfeit IC Detection Methods*", IEEE North Atlantic Test Workshop (NATW), 2013.

Student Awards Under My Supervision

- Finalist, Bring Down Counterfeiting Policy Hackathon, October 2022.
- 1st Place, HeLLO: CTF '21, Attacks on Hardware Logic Locking & Obfuscation Capture The Flag 2021, Jan 24, 2022.
- 1st Place, Hack@CHES 2021, The Hardware Capture the Flag in Conjunction with International Conference on Cryptographic Hardware and Embedded Systems (CHES), 2021.
- 2nd Place, Hack@SEC 2021, The Hardware CTF in Conjunction with USENIX Security Conference, 2021.
- 1st Place, UF/FICS Hardware De-obfuscation Competition, 2019.

PUBLICATIONS

- **Books**
  1. M. Tehranipoor, **U. Guin**, and D. Forte, "*Counterfeit Integrated Circuits: Detection and Avoidance,*" Springer, 2015.
- **Book Chapters**
  1. P. Cui, **U. Guin**, and M. Tehranipoor, "*Trillion Sensors Security,*" in Emerging Topics in Hardware Security, Springer, 2021.
  2. **U. Guin**, and M. Tehranipoor, "*Obfuscation and Encryption for Securing Semiconductor Supply Chain,*" in Hardware Protection through Obfuscation, Springer, 2017.
- **Patents**
  1. M. Tehranipoor, D. Forte, and **U. Guin**,"*A comprehensive framework for protecting intellectual property in the semiconductor industry,*" U.S. Patent No. 11,611,429, March 2023.
- **Journal Papers (Accepted)**
  1. Y. Zhong, and **U. Guin**, "*Complexity Analysis of the SAT Attack on Logic Locking,*" in IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), pp. 1-14, 2023.
  2. Y. Zhong, and **U. Guin**, "*A Comprehensive Test Pattern Generation Approach Exploiting SAT Attack for Logic Locking,*" in IEEE Transactions on Computers, pp. 1-11, 2023.
  3. Y. Zhong, A. Jain, M.T. Rahman, N. Adadi, J. Xie, and **U. Guin**, "AFIA: ATPG-Guided Fault Injection Attack on Secure Logic Locking," Journal of Electronic Testing: Theory and Applications (JETTA), pp. 1-17, 2023.
  4. W. Wang, A. D. Singh, and **U. Guin**, "*A Systematic Bit Selection Method for Robust SRAM PUFs*," Journal of Electronic Testing: Theory and Applications (JETTA), pp. 301-311, 2022.
  5. B. J. Lucas, A. Alwan, M. Murzello, Y. Tu, P. He, A. J. Schwartz, D. Guevara, **U. Guin**, K. Juretus, and J. Xie, "*Lightweight Hardware Implementation of Binary Ring-LWE PQC Accelerator,*" in IEEE Computer Architecture Letters, pp. 17-20, 2022.
  6. Z. Collier, **U. Guin**, J. Sarkis, and J. Lambert, "*Decision Model with Quantification of Buyer-Supplier Trust in Advanced Technology Enterprises,*" in Benchmarking: an International Journal, pp. 1-24, 2021.
  7. C. Tang, L. Alahmed, J. Xu, M. Shen, N. A. Jones, M. Sadi, **U. Guin**, W. Zhao, and P. Li, "*Effects of temperature and structural geometries on a skyrmion logic gate,*" in IEEE Transactions on Electron Devices (TED), pp. 1706-1712, 2021.

8. D. DiMase, Z. A. Collier, J. Muldavin, J. A. Chandy, D. Davidson, D. Doran, **U. Guin**, J. Hallman, J. Heebink, E. Hall, and Honorable A. R. Shaffer, "*Zero Trust for Hardware Supply Chains: Challenges in Application of Zero Trust Principles to Hardware,*" in National Defense Industrial Association (NDIA), pp. 1-53, 2021, [White Paper].
9. P. He, **U. Guin**, and J. Xie, "*Novel Low-Complexity Polynomial Multiplication over Hybrid Fields for Efficient Implementation of Binary Ring-LWE Post-Quantum Cryptography,*" in IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), pp. 383-394, 2021.
10. M. Sadi, and **U. Guin**, "*Test and Yield Loss Reduction of AI and Deep Learning Accelerators,*" IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), pp. 104-115, 2021.
11. P. Chowdhury, **U. Guin**, A. D. Singh, and V. D. Agrawal, "*Estimating Operational Age of an Integrated Circuit,*" Journal of Electronic Testing: Theory and Applications (JETTA), pp. 1-16, 2021.
12. A. Jain, Z. Zhou and **U. Guin**, "*TAAL: Tampering Attack on Any Key-based Logic Locked Circuits,*" ACM Transactions on Design Automation of Electronic Systems (TODAES), pp. 1-22, 2021.
13. Y. Zhang, A. Jain, P. Cui, Z. Zhou, and **U. Guin**, "*A Novel Topology-Guided Attack and Its Countermeasure Towards Secure Logic Locking,*" Journal of Cryptographic Engineering, pp. 1-14, 2020.
14. W. Wang, **U. Guin**, and A. D. Singh, "*Aging-Resilient SRAM-based True Random Number Generator for Lightweight Devices,*" Journal of Electronic Testing: Theory and Applications (JETTA), pp. 301-311, 2020.
15. J. Mahmod, and **U. Guin**, "*Robust, Low-Cost and Secure Authentication Scheme for IoT Applications,*" Cryptography, pp. 1-20, 2020.
16. P. Cui, J. Dixon, **U. Guin**, and D. DiMase, "*A Blockchain-Based Framework for Supply Chain Provenance,*" IEEE Access, pp. 157113-157125, 2019.
17. P. Cui, **U. Guin**, A. Skjellum, D. Umphress,"*Blockchain in IoT: Current Trends, Challenges, and Future Roadmap,*" Journal of Hardware and Systems Security, pp. 338-364, 2019.
18. Y. Zhang and **U. Guin**, "*End-to-End Traceability of ICs in Component Supply Chain for Fighting Against Recycling,*" IEEE Transactions on Information Forensics and Security, pp. 767-775, 2019.
19. **U. Guin**, N. Asadizanjani, and M. Tehranipoor "*Standards for Hardware Security,*" GetMobile: Mobile Computing and Communications, pp. 5-9, 2019.
20. B. Cyr, J. Mahmod, and **U. Guin**, "*Low-Cost and Secure Firmware Obfuscation Method for Protecting Electronic Systems from Cloning,*" IEEE Internet of Things Journal, pp. 3700-3711, 2019.
21. S. Wang, A. Ali, **U. Guin**, and A. Skjellum, "*IoTCP: A Novel Trusted Computing Protocol for IoT,*" Journal of The Colloquium for Information System Security Education (CISSE, pp. 165-180), 2018.
22. **U. Guin**, Z. Zhou, and A. Singh, "*Robust Design-for-Security (DFS) Architecture for Enabling Trust in IC Manufacturing and Test,*" IEEE Transactions on VLSI Systems (TVLSI), pp. 818-830, 2018.
23. M. Alam, M. Tehranipoor, and **U. Guin**, "*TSensors Vision, Infrastructure and Security Challenges in Trillion Sensor Era: Current Trends and Future Directions,*" Journal of Hardware and Systems Security (HaSS), pp. 311-327, 2017.
24. M. Tehranipoor, **U. Guin**, and S. Bhunia, "*Invasion of the Hardware Snatchers: Cloned Electronics Pollute the Market,*" IEEE Spectrum, pp. 36-41, 2017.
25. **U. Guin**, S. Bhunia, D. Forte, and M. Tehranipoor, "*SMA: A System-Level Mutual Authentication for Protecting Electronic Hardware and Firmware,*" IEEE Transactions on Dependable and Secure Computing (TDSC), pp. 265-278, 2016.
26. **U. Guin**, Q. Shi, D. Forte, and M. Tehranipoor, "*FORTIS: A Comprehensive Solution for Establishing Forward Trust for Protecting IPs and ICs,*" ACM Transactions on Design Automation of Electronic Systems (TODAES)), pp. 1-20, 2016.
27. **U. Guin**, D. Forte, and M. Tehranipoor, "*Design of Accurate Low-Cost On-Chip Structures for protecting Integrated Circuits against Recycling,*" IEEE Transactions on VLSI Systems (TVLSI), pp. 1233-1246, 2015.

28. **U. Guin**, K. Huang, D. DiMase, J. M. Carulli Jr., M. Tehranipoor, and Y. Makris, "*Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain*," Proceedings of the IEEE, pp. 1207-1228, 2014. **(cited in "*White House 100-Day Reviews under Executive Order 14017*" on "*Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth*," 2021)**.
29. **U. Guin**, D. DiMase, and M. Tehranipoor, "*Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead,*" Journal of Electronic Testing: Theory and Applications (JETTA), pp. 9-23, 2014. **(Most Downloaded Article in 2014)**.
30. **U. Guin**, D. DiMase, and M. Tehranipoor, "*A Comprehensive Framework for Counterfeit Defect Coverage Analysis and Detection Assessment,*" Journal of Electronic Testing: Theory and Applications (JETTA), pp. 25-40, 2014. **(Top 10 Downloaded Article in 2014)**.

- **Conference Papers**

1. **U. Guin** and B. Krishnamachari, "*Blockchain-enabled Whitelisting for securing 3D ICs,*" in GOMACTech, pp. 1-4, 2024.
2. G. Odom, Z. T. Tisha, and **U. Guin**, "*Self-Referencing Electrical Tests using SRAM Power-up States for Detecting Recycled ICs,*" in GOMACTech, pp. 1-6, 2024.
3. Y. Zhong, A. Ebrahim, **U. Guin**, and V. Menon, "*A Modular Blockchain Framework for Enabling Supply Chain Provenance,*" in IEEE Physical Assurance and Inspection of Electronics (PAINE), pp. 1-7, 2023.
4. Y. Zhong, J. Hovanes, and **U. Guin**, "*On-Demand Device Authentication using Zero-Knowledge Proofs for Smart Systems,*" in Great Lakes Symposium on VLSI (GLSVLSI), pp. 1-6, 2023.
5. J. Hovanes, Y. Zhong, and **U. Guin**, "*A Novel IoT Device Authentication Scheme Using Zero-Knowledge Proofs,*" in GOMACTech, pp. 1-4, 2023.
6. J. Hovanes, Y. Zhong, and **U. Guin**, "*Beware of Discarding Used SRAMs: Information is Stored Permanently,*" in IEEE Physical Assurance and Inspection of Electronics (PAINE), pp. 1-7, 2022, **(Best Paper Award)**.
7. Y. Zhong, and **U. Guin**, "*Fault-Injection Based Chosen-Plaintext Attacks on Multicycle AES Implementations,*" in Great Lakes Symposium on VLSI (GLSVLSI), pp. 1-6, 2022.
8. Y. Zhong, and **U. Guin**,"*Chosen-Plaintext Attack on Energy-Efficient Hardware Implementation of GIFT-COFB,* in IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 1-4, 2022.
9. Y. Zhang, C. Tang, P. Li, and **U. Guin**, "*CamSkyGate: Camouflaged Skyrmion Gates for Protecting ICs,* in Design Automation Conference (DAC), pp. 1-6, 2022.
10. Z. Zhou, **U. Guin**, P. Li, and V. D. Agrawal, "*Fault Modeling and Test Generation for Technology-Specific Defects of Skyrmion Logic Circuits,* in VLSI Test Symposium (VTS), pp. 1-7, 2022.
11. M. Sadi, P. Li, **U. Guin**, S. Walters, and D. DiMase, "*Low Power, Rad-Hard, and Secure Polymorphic and Neuromorphic Designs using Skyrmions,* in GOMACTech, 2022.
12. Y. Tu, P. He, **U. Guin** and J. Xie, "*Low-Complexity Implementation of Lightweight Ring-LWE based Post-Quantum Cryptography,* in GOMACTech, 2022.
13. Pratiksha Mittal, Austin Walthall, Pinchen Cui, Anthony Skjellum and **U. Guin**, "*A Blockchain-Based Contactless Delivery System for Addressing COVID-19 and Other Pandemics,* in IEEE Workshop on Blockchain Security, Application, and Performance (BSAP), pp. 1-6, 2021.
14. Z. Zhou, **U. Guin**, P. Li and V. Agrawal, "*Defect Characterization and Testing of Skyrmion-Based Logic Circuits,* in VLSI Test Symposium (VTS), pp. 1-7, 2021, **(Best Paper Nomination)**.
15. S. Kundu, K. Basu, M. Sadi, T. Titirsha, S. Song, A. Das and **U. Guin**, "*Special Session: Reliability Analysis for AI/ML Hardware,* in VLSI Test Symposium (VTS), pp. 1-10, 2021.
16. A. Jain, Z. Zhou, and **U. Guin**, "*Survey of Recent Developments for Hardware Trojan Detection,*" in IEEE International Symposium on Circuits & Systems (ISCAS), pp. 1-5, 2021.

17. A. Jain, and **U. Guin**, "*A Novel Tampering Attack on AES Cores with Hardware Trojans*," in International Test Conference in Asia (ITC-Asia), pp. 77-82, 2020.
18. A. Jain, M. T. Rahman and **U. Guin**, "*ATPG-Guided Fault Injection Attacks on Logic Locking,*" in IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE), pp. 1-6, 2020.
19. A. Stern, D. Mehta, S. Tajik, **U. Guin**, F. Farahmandi and M. Tehranipoor, "*SPARTA: Laser Probing Approach for Sequential Trojan Detection in COTS Integrated Circuits,*" in IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE), pp. 1-6, 2020.
20. A. Jain, **U. Guin**, M. T. Rahman, N. Asadizanjani, D. Duvalsaint, and R. D. (Shawn) Blanton, "Special Session: Novel Attacks on Logic-Locking", in VLSI Test Symposium (VTS), pp. 1-10, 2020.
21. J. Xie, K. Basu, K. Gaj and **U. Guin**, "Special Session: The Recent Advance in Hardware Implementation of Post-Quantum Cryptography", in VLSI Test Symposium (VTS), pp. 1-10, 2020.
22. W. Wang, **U. Guin**, and A. Singh, "*A Zero-Cost Detection Approach for Recycled ICs using Scan Architecture,*" in VLSI Text Symposium (VTS), pp. 1-6, 2020.
23. Y. Zhang, P. Cui, Z. Zhou, and **U. Guin**, "*TGA: An Oracle-less and Topology Guided Attack on Logic Locking,*" Attacks and Solutions in Hardware Security (ASHES), pp. 75-83, 2019.
24. P. Cui and **U. Guin**, "*Countering Botnet of Things using Blockchain-Based Authenticity Framework,*" in IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 598-603, 2019.
25. **U. Guin**, W. Wang, C. Harper, and A. D. Singh, "*Detecting Recycled SoCs by Exploiting Aging Induced Biases in Memory Cells,*" in IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 72-80, 2019.
26. J. Mahmod, S. Millican, **U. Guin**, and V. D. Agrawal, "*Delay Fault Testing: Present and Future,*" in IEEE VLSI Test Symposium (VTS), pp. 1-10, 2019.
27. P. Chowdhury, **U. Guin**, A. D. Singh and V. D. Agrawal, "*Two-Pattern ΔI_{DDQ} Test for Recycled IC Detection,*" in International Conference on VLSI Design (VLSID), pp. 82-87, 2019.
28. **U. Guin**, P. Cui, and A. Skjellum, "*Ensuring Proof-of-Authenticity of IoT Edge Devices using Blockchain Technology,*" in IEEE International Conference on Blockchain, pp. 1042-1049, 2018.
29. W. Wang, A. Singh, **U. Guin**, and A. Chatterjee, "*Exploiting Power Supply Ramp Rate for Calibrating Cell Strength in SRAM PUFs,*" in IEEE Latin-American Test Symposium (LATS), pp. 1-6, 2018.
30. M. Alam, S. Chowdhury, M. Tehranipoor, and **U. Guin**, "*Robust, Low-Cost, and Accurate Detection of Counterfeit ICs using Digital Signatures,*" IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 209-214 , 2018.
31. Z. Zhou, **U. Guin**, and V. D. Agrawal, "*Modeling and Testing for Combinational Hardware Trojans,*" VLSI Test Symposium (VTS), pp. 1-6, 2018.
32. **U. Guin**, A. Singh, M. Alam, J. Cañedo, and A. Skjellum, "*A Secure Low-Cost Edge Device Authentication Scheme for the Internet of Things,*" International Conference on VLSI Design (VLSID), pp. 85-90, 2018.
33. **U. Guin**, "*Efficient Strategies for Detection and Avoidance of Counterfeit ICs,*" IEEE North Atlantic Test Workshop (NATW), pp. 1-5, 2017.
34. **U. Guin**, Z. Zhou, and A. Singh, "*A Novel Design-for-Security (DFS) Architecture to Prevent Unauthorized IC Overproduction,*" IEEE VLSI Test Symposium (VTS), pp. 1-6, 2017.
35. B. Shakya, **U. Guin**, M. Tehranipoor and D. Forte, "*Performance Optimization for On-Chip Sensors to Detect Recycled ICs,*" IEEE International Conference on Computer Design (ICCD), pp. 289-295, 2015.
36. **U. Guin**, X. Zhang, D. Forte, and M. Tehranipoor, "*Low-Cost On-Chip Structures for Combating Die and IC Recycling,*" Design Automation Conference (DAC), pp. 1-6, 2014.

37. **U. Guin**, D. Forte, D. DiMase, and M. Tehranipoor, "*Counterfeit IC Detection: Test Method Selection Considering Test Time, Cost, and Tier Level Risk,*" GOMACTech, pp. 1-4, 2014.
38. **U. Guin**, D. Forte, and M. Tehranipoor, "*Low-cost On-Chip Structures for Combating Die and IC Recycling,*" GOMACTech, pp. 1-3, 2014.
39. **U. Guin**, D. Forte, and M. Tehranipoor, "*Anti-Counterfeit Techniques: From Design to Resign,*" IEEE Microprocessor Test and Verification (MTV), pp. 89-94, 2013.
40. **U. Guin** and M. Tehranipoor, "*CDIR: Low-Cost Combating Die/IC Recycling Structures,*" DMSMS, 2013 (Extended Abstract).
41. **U. Guin**, T. Chakraborty, and M. Tehranipoor, "*Functional F_{max} Test-Time Reduction using Novel DFTs for Circuit Initialization,*" IEEE Int. Conference on Computer Design (ICCD), pp. 1-6, 2013.
42. **U. Guin**, T. Chakraborty, and M. Tehranipoor, "*Novel DFTs for Circuit Initialization to Reduce Functional Fmax Test Time,*" IEEE North Atlantic Test Workshop (NATW), pp. 1-5, 2013.
43. **U. Guin** and M. Tehranipoor, "*On Selection of Counterfeit IC Detection Methods,*" IEEE North Atlantic Test Workshop (NATW), pp. 1-5, 2013. **(Received Best Paper Award)**.
44. M. Tehranipoor and **U. Guin**, "*Counterfeit Detection Technology Assessment,*" GOMACTech, pp. 1-4, 2013.
45. N. Murphy, **U. Guin**, and M. Tehranipoor, "*Counterfeit Detection Technology Assessment,*" DMSMS & Standardization, 2012.
46. **U. Guin** and C. -H. Chiang, "*Design for Bit Error Rate Estimation of High Speed Serial Links,*" IEEE VLSI Test Symposium (VTS), pp. 278-283, 2011.

- **Technical Reports**
  1. **U. Guin**, M. Tehranipoor, D. DiMase, and M. Megrdician, "*Counterfeit IC Detection and Challenges Ahead,*" ACM SIGDA, pp. 1-5, March 2013.

- **Thesis**
  1. **U. Guin**, "*Establishment of Trust and Integrity in Modern Supply Chain from Design to Resign,*" PhD Thesis, University of Connecticut, CT, 2016.
  2. **U. Guin**, "*Design for Bit Error Rate Estimation of High Speed Serial Links,*" Masters Thesis, Temple University, PA, 2010.

SERVICE

- **Editorial Activities**
  1. Associate Editor, Journal of Electronic Testing: Theory and Applications (JETTA), 2022-Present
  2. Associate Editor, Journal of Hardware and Systems Security (HaSS), 2022-Present
  3. Guest Editor, IEEE Blockchain Technical Briefs, 2022
  4. Guest Editor, IEEE Design & Test - Special Issue: International Test Conference (SI:ITC'2018)

- **Conference Organizing Committee**
  1. Vice-program Co-Chair, IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2024
  2. Tutorial Chair, International Conference on VLSI Design (VLSID) 2024
  3. Track Co-Chair, Hardware and System Security (HSS), ISQED 2024
  4. Co-program Chair, IEEE Physical Assurance and Inspection of Electronics (PAINE) 2023
  5. Tutorial Chair, GLSVLSI 2023
  6. Student Activities Chair, VLSI Test Symposium (VTS) 2021-Present
  7. Finance Chair, IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2023

8. Vice-Program Chair, IEEE Physical Assurance and Inspection of Electronics (PAINE) 2022
9. Vice Program Chair, CAD4 Security Workshop, DAC 2022
10. Chair, HOST 2022 Microelectronics Security Challenge 2022
11. Registration Chair/Vice Finance and Microelectronics Security Challenge Chair, IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2022
12. Technical Program Co-Chair (TPC), International Test Conference - India 2022
13. Registration Chair/Vice Finance, IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2021-2022
14. Publication Chair, IEEE International Conference on Omni-Layer Intelligent Systems (COINS) 2021
15. Registration Chair, IEEE Physical Assurance and Inspection of Electronics (PAINE) 2020
16. Audio/Video Chair, VLSI Test Symposium (VTS) 2019–2020

- **Session Organizer**
  1. Detection and Avoidance of Counterfeit ICs, IEEE International Test Conference - India 2022
  2. Security-Aware Computer Aided Electronic Design, Design Automation Conference (DAC) 2021
  3. Reliability Analysis for AI/ML Hardware, IEEE VLSI Test Symposium (VTS) 2021
  4. Novel Attacks on Logic Locking, IEEE VLSI Test Symposium (VTS) 2020
  5. The Recent Advance in Hardware Implementation of Post-Quantum Cryptography, IEEE VLSI Test Symposium (VTS) 2020
  6. Special Session on Hardware Security, Asian Test Symposium (ATS) 2019
  7. Reverse Engineering Track Co-Chair, International Symposium for Testing and Failure Analysis (ISTFA) 2018
- **Technical Program Committee**
  1. IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2020-Present
  2. International Test Conference (ITC) 2022 -Present
  3. IEEE Physical Assurance and Inspection of Electronics (PAINE) 2020-Present
  4. IEEE VLSI Test Symposium (VTS) 2019-Present
  5. International Conference on VLSI Design (VLSID) 2019-Present
  6. IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2019-Present
  7. IEEE International Conference on Blockchain 2019-Present
  8. ACM Great Lakes Symposium on VLSI (GLSVLSI) 2019-Present
  9. Design Automation Conference (DAC) 2020-2022
  10. IEEE North Atlantic Test Workshop (NATW) 2018- 2022
  11. International Symposium on Consumer Technologies (ISCT) 2019
  12. IEEE International Conference on Computer Design (ICCD) 2018
  13. IEEE Cyber Science and Technology Congress (CyberSciTech) 2018
  14. International Symposium on Devices, Circuits and Systems (ISDCS) 2018
- **Groups**
  1. Liaison of SAE G-19A Test Laboratory Standards Development Committee 2015-Present
  2. G-32 Cyber-Physical Systems Security Committee 2019-Present
  3. Subgroup lead of AS6171/1: Suspect/Counterfeit Test Evaluation Method 2016-2022
- **Tutorials**

1. Logic Locking: Current Trends, Attacks and Future Directions, International Conference on VLSI Design (VLSID), 2019.

- **Invited Talks**
  1. Trust and Assurance Workshop, Electronics Division Meeting, National Defense Industrial Association (NDIA), Arlington, VA, 2022, Title: *Counterfeit Defect Coverage That Was Completed By The SAE G-19A Group*.
  2. CAD for Security Workshop, Co-located with Design Automation Conference (DAC), San Francisco, CA, 2022, Title: *SAT Attack Complexity Analysis*.
  3. Micro-Electronics Security Training (MEST) Center, Gainesville, FL, 2021, Title: *Towards Resilient Approaches for Detecting Recycled ICs*.
  4. SRA Symposium on Hardware and Cyber-Physical Systems, Arlington, VA, Dec. 2019, Title: Counterfeit Defect Coverage Analysis: Current Status and Future Directions.
  5. IEEE Electronic Design Process Symposium (EDPS), Milpitas, CA, Sept. 2018, Title: Cybersecurity Solutions in Hardware.
  6. IEEE Microprocessor Test and Verification (MTV) Conference, Austin, TX, Dec. 2017, Title:Mutual Authentication: A Robust Solution for Preventing System-Level Cloning.
  7. International Test Conference (ITC), Fort Worth, TX, Nov. 2017, Title: Efficient Strategies for Combating Die and IC Recycling.
  8. IEEE North Atlantic Test Workshop (NATW), Warwick, RI, Title: Efficient Strategies for Detection and Avoidance of Counterfeit ICs.

- **Session Chair**
  1. Design Automation Conference (DAC) 2017-2022
  2. IEEE VLSI Test Symposium (VTS) 2017-Present
  3. International Test Conference (ITC) 2017-Present
  4. IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2019
  5. International Symposium for Testing and Failure Analysis (ISTFA) 2018
  6. International Conference On Computer Aided Design (ICCAD) 2017-2018
  7. IEEE International Conference on Blockchain 2018
  8. IEEE International Conference on Computer Design (ICCD) 2018

- **Reviewer (Grants) for**
  1. National Science Foundation 2019-Present
  2. Department of Energy 2021
  3. Cyber Florida 2019
  4. The University of Tennessee at Chattanooga Internal Grant Competition 2018
  5. Intramural Grants Program, Auburn University 2018

- **Reviewer (Journal) for**
  1. IEEE Transactions on Information Forensics & Security (TIFS) 2018-Present
  2. IEEE Transactions on VLSI Systems (TVLSI) 2015-Present
  3. Journal of Electronic Testing: Theory and Applications (JETTA) 2012-Present
  4. IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2016-Present
  5. ACM Transactions on Design Automation of Electronic Systems (TODAES) 2014-Present
  6. Journal of Hardware and Systems Security (HASS) 2016-Present
  7. IEEE Transactions on Circuits and Systems II 2019- Present
  8. IEEE Internet of Things Journal 2019-Present

9. Journal on Emerging Technologies in Computing Systems (JETC) 2017-Present
10. IEEE Design & Test 2014-Present
11. Nature Electronics 2019
12. MDPI Cryptography 2018
13. Integration, the VLSI Journal 2018
14. Transactions on Multi-Scale Computing Systems 2018
15. Future Generation Computer Systems 2018
16. IEEE Transactions on Industrial Informatics (TII) 2018
17. Embedded Systems Letters 2017
18. Transactions on Computers (TC) 2017
19. IEEE Transactions on Circuits and Systems (TCAS) 2017
20. IEEE Transactions on Dependable and Secure Computing (TDSC) 2016, 2017
21. IEEE Computer (COMSI) 2016
22. IEEE Transactions on Multi-Scale Computing Systems (TMSCS) 2015
23. IET Computers & Digital Techniques 2014

- **Judge for Poster Sessions and Hardware Demos**
  1. IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2017-Present
  2. Graduate Engineering Research Showcase, Auburn University 2016-Present
  3. Hack@DAC at Design Automation Conference (DAC) 2017

- **Conference Presentations**
  1. Design Automation Conference (DAC) 2022
  2. Great Lakes Symposium on VLSI (GLSVLSI) 2022-2023
  3. IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2018,2019
  4. IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2019
  5. IEEE VLSI Test Symposium (VTS) 2017, 2018
  6. International Conference on VLSI Design (VLSID) 2018, 2019
  7. IEEE International Conference on Blockchain 2018

TEACHING EXPERIENCES

- Associate Professor, ECE Department, Auburn University 2023- Present
  - Instructor
    - ELEC 5210/6210: Hardware Security I Fall 2023 - Present
    - ELEC 4200: Digital System Design Fall 2023- Present

- Assistant Professor, ECE Department, Auburn University 2016- 2023
  - Developed two novel Hardware Security courses
    - Hardware Security - I for Fall Semesters
    - Hardware Security - II for Spring Semesters
  - Instructor
    - ELEC 5210/6210: Hardware Security I Fall 2019 - Fall 2022
    - ELEC 5970/ELEC 6970: Hardware Security II Spring 2019 - Spring 2021
    - ELEC 4200: Digital System Design Spring 2019 - Spring 2022
    - ELEC 5970/ELEC 6970: Hardware Security I Fall 2018
    - ELEC 7970: Hardware Security II Spring 2018
    - ELEC 5970/ELEC 6970: Introduction to Hardware Security Fall 2017

        - ELEC 5200/6200: Computer Architecture and Design — Spring 2017
        - ELEC 5200/6200: Computer Architecture and Design — Fall 2016

- Graduate Student, ECE Department, University of Connecticut — August 2011- May 2012
    - Guest Lecturer
        - ECE 4095: Trustable Computing Systems — Spring 2014 - 2015
        - ECE 4451/5451: Introduction to Hardware Security and Trust — Spring 2014
        - ECE 4095: Hardware Hacking — Spring 2012
    - Teaching Assistant
        - ECE 3401: Digital Systems Design — Spring 2012
        - ECE3421: VLSI Design and Simulation — Spring 2012
        - ECE4401: Digital Design Laboratory — Fall 2011

- Graduate Student, ECE Department, Temple University — August 2008- May 2010
    - Teaching Assistant
        - 3622: Embedded System Design
        - 3623: Embedded System Design Lab
        - 3612: Microprocessor Systems Microprocessor Systems
        - 3613: Microprocessor Systems Microprocessor Systems Lab
        - 2612: Digital Circuit Design
        - 2613: Digital Circuit Design Lab

CURRENT STUDENTS

- Ph.D. Students
    1. Yadi Zhong, B.S., Auburn University
    2. Christopher McGill, B.S., The Pennsylvania State University
    3. Aritri Priya Saha, National Institute of Technology, Rourkela
    4. Tejaswini Koppula, Jawaharlal Nehru Technological Univ Hyderabad
    5. Zakia Tamanna Tisha, B.S., Bangladesh University of Professionals and M.S., University Of Minnesota-Duluth
    6. Swati Dey, B.Tech and M.Tech, Maulana Abul Kalam Azad University of Tech

- Master's Students
    1. Colton Bailey, B.S., Auburn University
    2. Gaines Odom, B.S., Auburn University

FORMER GRADUATE STUDENTS

- Ph.D. Students
    1. Yuqiao Zhang [MaxLinear], 2022, Thesis: Robust Solutions for Enabling Trust in Digital Circuits
    2. Ziqi Zhou [Cadence], 2021, Thesis: Novel Approaches for Microelectronics Security and Test

- Master's Students
    1. Josh Hovanes [TBD], 2023, Thesis: Aging-Induced Long-Term Data Remanence in SRAM Cells.
    2. Caleb Mccarley [Parsons], 2023.
    3. Pratiksha Mittal [DPSCD], 2021, Thesis: A Blockchain-based Contactless Delivery System for COVID-19 and Other Pandemics.
    4. Ayush Jain [Intel], 2020, Thesis: Novel Fault Injection Attacks on Logic Locking using ATPG.
    5. Jubayer Mahmod [Virginia Tech], 2019, Thesis: Towards Unclonable System Design for Resource-Constrained Applications.
    6. Prattay Chowdhury [Qualcomm], 2019.

- Undergraduate Students Mentored
    1. Cyril Adjei, 2021
    2. Mukarram Faridi, 2021
    3. Paschal Onyeka, 2021
    4. Umar Farouk, 2021
    5. Craig Manes, 2021
    6. Alex Bonner, 2020
    7. Stephen Fortner, 2020
    8. Yadi Zhong, 2020
    9. William Champion, 2020
    10. Holden Covington, 2020
    11. Julie Dixon, BS, 2019.
    12. Benjamin Cyr, BS, 2018.

PROFESSIONAL MEMBERSHIP

- Senior Member of the Institute of Electrical and Electronics Engineers (IEEE)
- Member of Association for Computing Machinery (ACM)

REFERENCES

Reference information will be provided upon request.

CITIZENSHIP STATUS

Indian with Green Card