Basic course information

Friday, August 10, 2012
11:08 AM

The class was set up to cover "advanced" topics
the topics in 8710 change from time to time, I look at students background and their interests and try to tune my course content to fit their needs.

For past offerings (3 out of my 12 years teaching here),

- one is on TCAD, at that time, we were using Medici
- One is on RF
- One is on on-chip measurement (2008)

All my courses are very hands-on, meaning I'll work with you with state-of-the-art devices (made at IBM and other places) and CAD tools (Cadence and Synopsys).

Some basic familiarity with unix / linux / matlab / python will be helpful but not required, I'll bring you up to speed with those skills over the semester.

plan

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My plan is very ambitious this time :

- Have a review or introduction depending on your background of semiconductors, pn junctions, transistors, mosfets and then
- get to more "advanced" topics including
- on-chip measurements, from DC to microwave freqs,
- compact models, including extraction, and modern CAD tools, cadence or ads, verilog-a for compact model development. You will learn how to build compact models and equally importantly put them into use in circuit simulators.
- TCAD, I know some of you like Chelvi have an interest in knowing more about TCAD.
- Noise, hopefully you will do some low-frequency noise measurements by yourself too.
- Radiation effects
- Temperature effects - all of our electronics need to work over certain temperature range, not just at 300K!

Obviously we still have the same hours, the plan is that you will spend most of your time on topics that interest you most, and work on class projects that closely relate to your research interests. For instance, one person is primarily interested in tcad, and can focus on the tcad

part of the course.

Professional and General Computing Tools

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Some basic familiarity with unix / linux / matlab / python will be helpful but not required, I'll bring you up to speed with those skills over the semester.

In modern companies there are often needs to quickly learn to use and deploy large scale software - the manuals can easily have thousands of pages. These are not general purpose software - and require specific engineering knowledge. In this course you will get to learn some or all of the following, depending on your interest and interest:

1. Basic linux
2. Basic matlab
3. Python
4. Iccap - for device and circuit measurement and compact modeling
5. Sentaurus suite of tools from synopsys - for device simulation
6. Cadence tools - we will not deal with layout, but will use it for compact modeling and verilog-a
7. ADS - for RF and microwave circuit simulation (yes, cadence can do it too, but ads has its own strength)

Teaching / learning philosophy

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1. Building on previous knowledge
2. For graduate level course, taking a course is taking on a research project - do not limit yourself to in-class material, mixing class with research is highly encouraged
3. Questions are encouraged
4. It is very important at this level to have a practical understanding of the correct order of magnitude, e.g.
   - Practical doping range is from 1e14 to 1e21, why?
   - Practical doping levels in modern bipolar, emitter around 1e20-1e21, base is around 1e18, collector, 1e16 to 1e18, why polysilicon emitter is used, thickness of poly emitter / poly gate in CMOS is around 100nm, base is around 100nm and less, collector is a few tenth of micrometers
   - VCE / VDS handling capability of modern transistors
5. Know the assumptions - an ideal wire in your circuit schematic is never an ideal wire, circuit design will be a lot simpler if so. Your transistor gm in equivalent circuit is independent of frequency - this is not true at very high frequencies, how high is very high? In what freq range can I trust my Cadence simulation?

Semiconductor device philosophy

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Most devices operate on the principle of modulating current through carrier (n and p) modulation using a voltage.

Both bipolar and field effect transistors work this way.

So it is critical to understand how applied voltages modulate carriers.

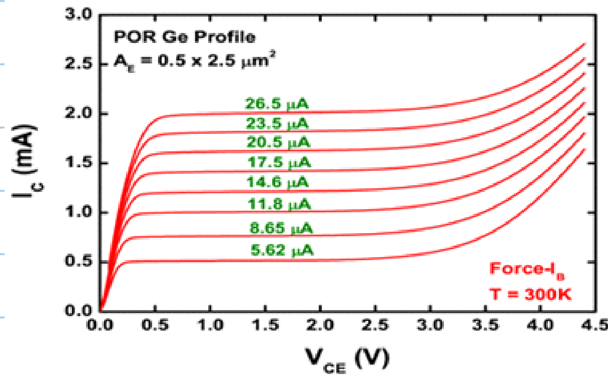
Carrier modulation means charge modulation by voltage, so that is capacitance.

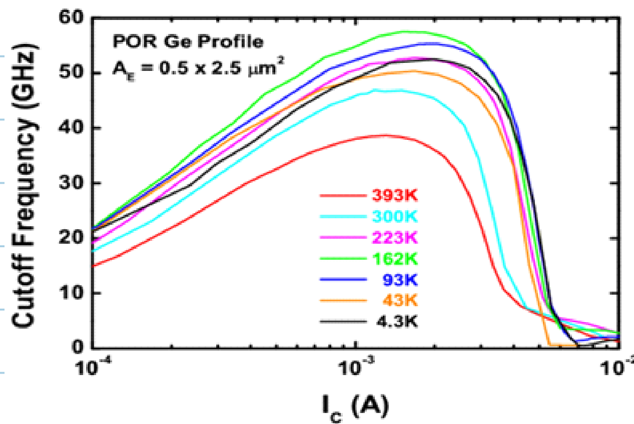
Capacitive current increases with frequency, so at high enough frequencies, current gain will be too low, transistors lose current amplification capability, so there exists a cut-off frequency above which there is no current amplification (ft.)

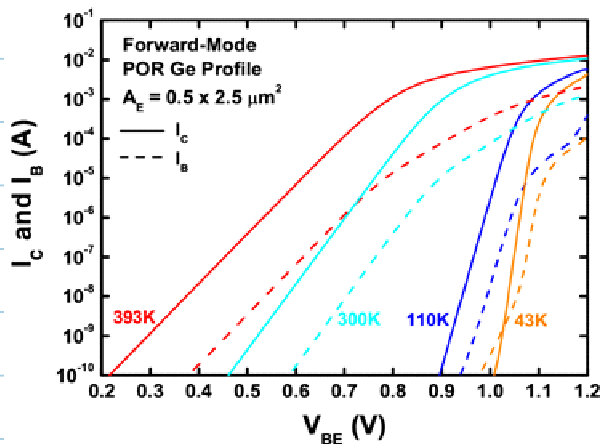
So no matter how complicated the device is, we need to understand / design / experimentally measure / build models / simulate:

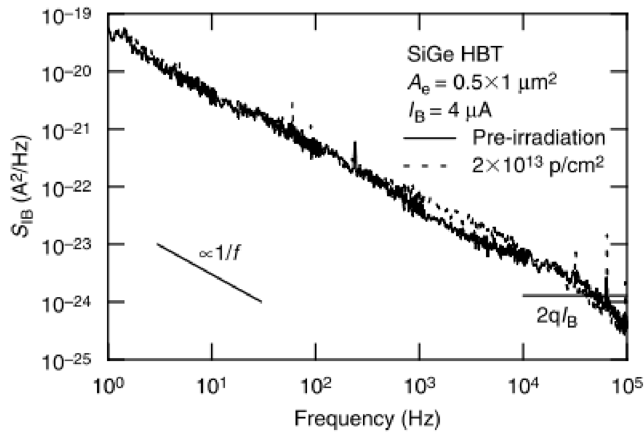
- How currents change with voltages under dc, ac, and transient excitations (I-V curves, s-parameters, noise etc)
- This inevitably involve charges (capacitances) responsible for producing currents

- All parasitic resistances, capacitances, inductances should be accounted for too, the level of which depends on freq requirement

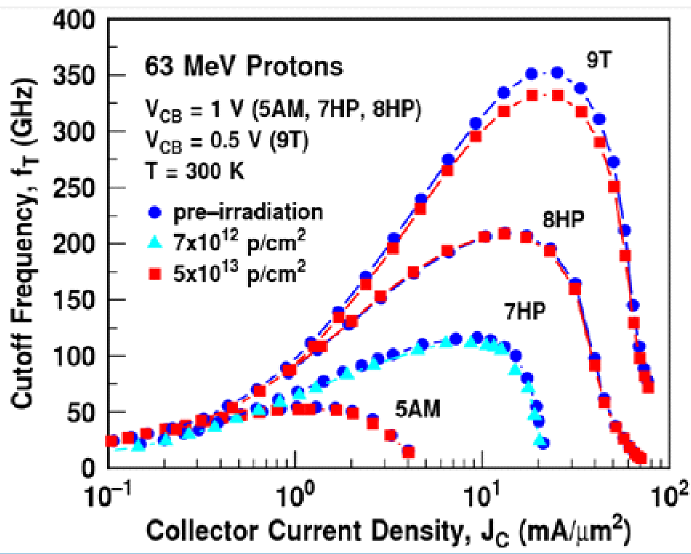








SiGe HBT
$A_e = 0.5 \times 1\ \mu m^2$
$I_B = 4\ \mu A$
Pre-irradiation
2×10^{13} p/cm²
∝1/f
$2qI_B$
S_{IB} (A²/Hz)
Frequency (Hz)



63 MeV Protons
V_{CB} = 1 V (5AM, 7HP, 8HP)
V_{CB} = 0.5 V (9T)
T = 300 K
pre–irradiation
7x10¹² p/cm²
5x10¹³ p/cm²
9T
8HP
7HP
5AM
Cutoff Frequency, f_T (GHz)
Collector Current Density, J_C (mA/µm²)

Circuit level

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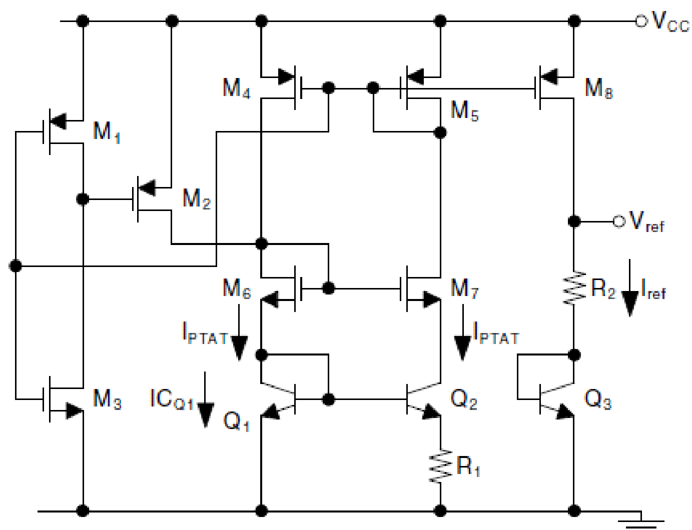
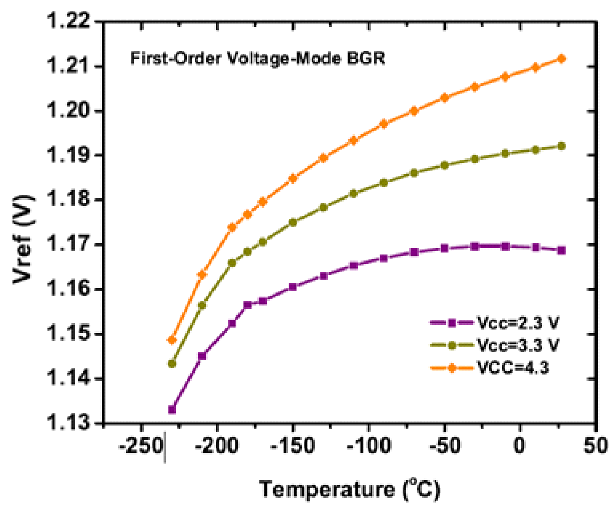


Fig. 1. Schematic of a first-order SiGe bandgap reference [2].



Device level

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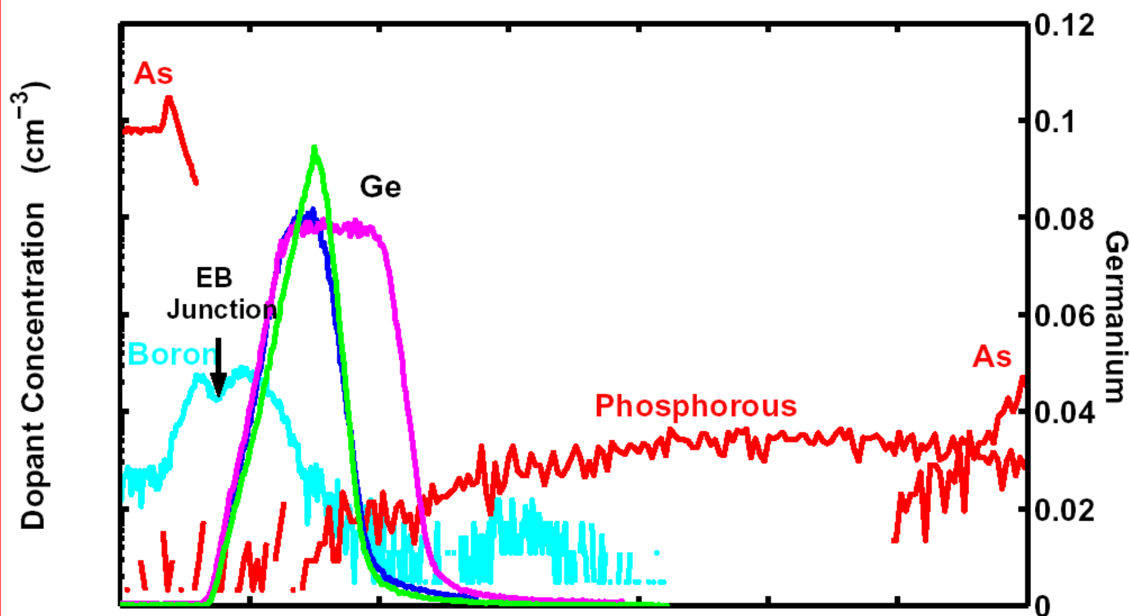
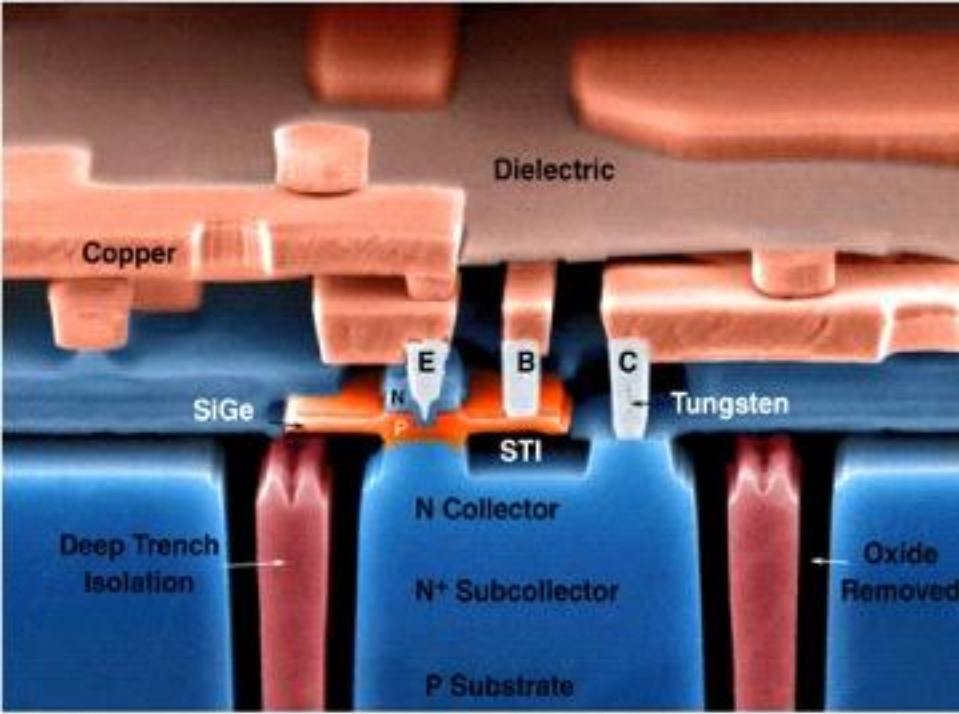
Design doping / Ge distributions

Drift-diffusion equation, Poisson's equation, Current continuity equations - solve them. Simulate - optimize design.




Dielectric
Copper
E
B
C
N
P
SiGe
Tungsten
STI
N Collector
Deep Trench
Isolation
N+ Subcollector
Oxide
Removed
P Substrate

Carrier level

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Drift
Diffusion
Non-equilibrium transport (track movement of individual electrons and holes)

Compact modeling

Monday, August 13, 2012
11:15 AM

Examples:

MOS:
Bsim3v3 still widely in use
Bsim4
PSP - for sub-90nm
Bsim SOI

Bipolar:
EM
SGP
Vbic
Modern standard: mextram and Hicum

Why we need compact models:

For a 0.13um SiGe BiCMOS process, mask cost can be as high as $1million!

Accurate models will save design cost.

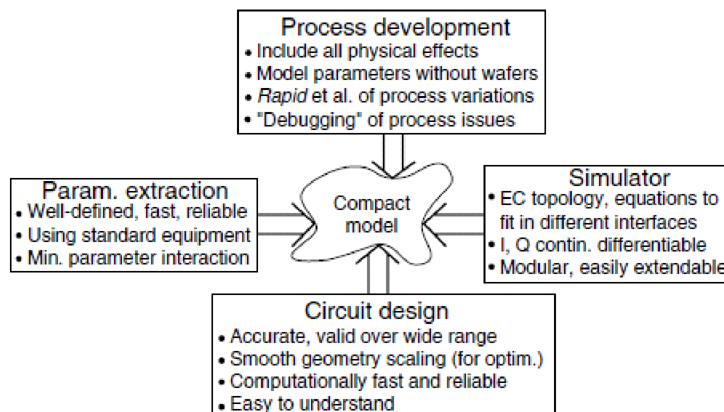
Modern compact models are sophisticated. It takes many years (or 20 years) historically to develop production circuit design ready models used in modern design kits found in IBM, Intel ...

It is constantly being developed as technologies evolve.

Compact models are always behind actual technology development

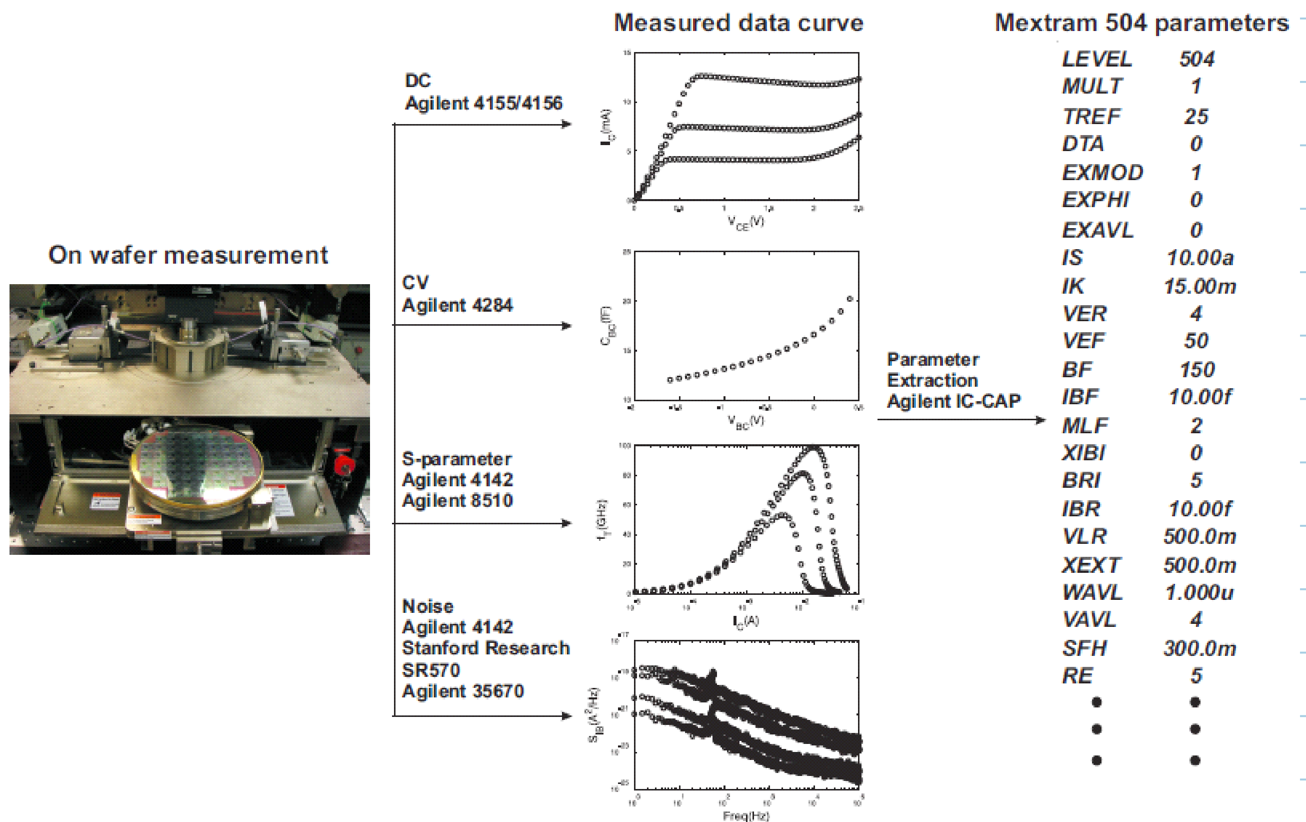
I'll focus on bipolar compact models as I have more experience with their internal workings and we have data you can experiment with.

There are many aspects of compact model development beyond just transistor theories - which are hard to begin with:



Picture From Schroeter's book chapter on Hicum,

Typical compact modeling procedures - using a HBT example



Source: recent Mextram PhD Dissertation from TU Delft, by H. Wu.

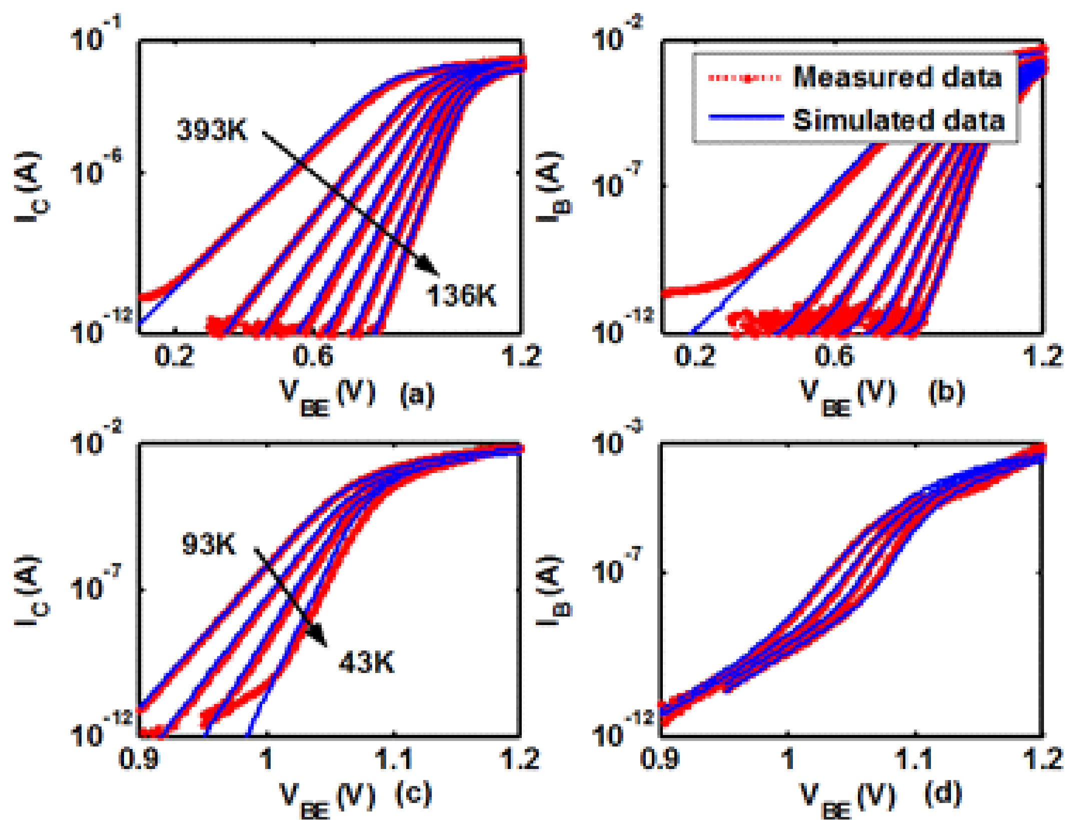
Challenges of teaching:

- Access to state of the art devices
- In depth understanding of knowledge / development in several decades in short time
- Expensive equipment, each probe is easily over 1000$ direct cost (before 45% overhead)
- Steep learning curves involved for about every step from measurement to theory to parameter extraction

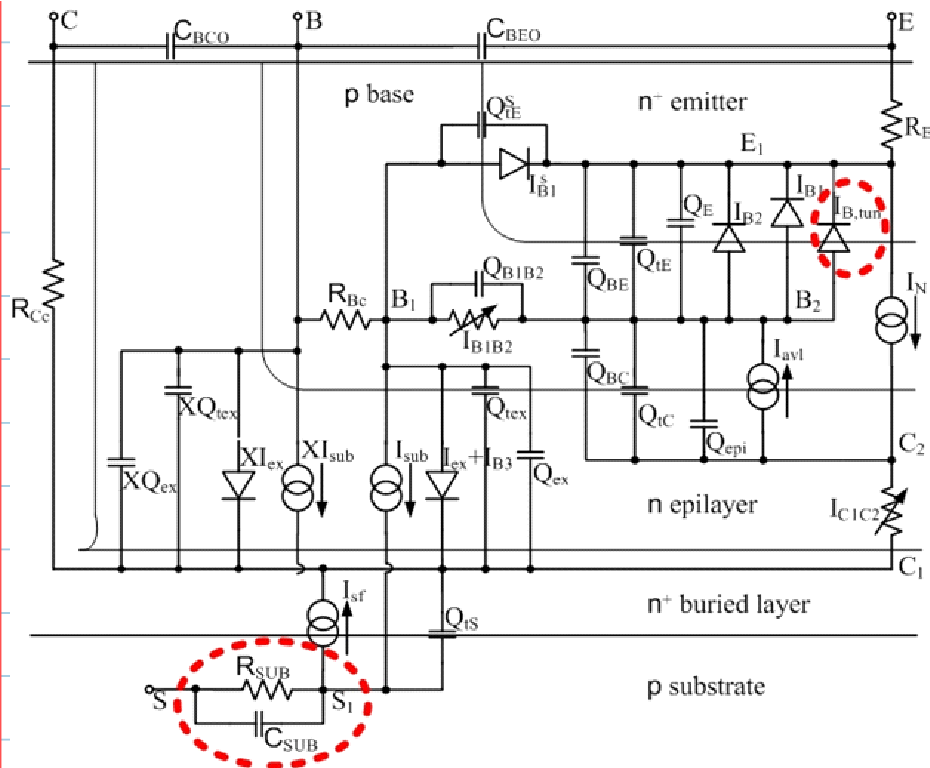
a wide T range SiGe HBT example

Thursday, April 26, 2012
9:55 PM

Model SiGe HBT from 393 down to 43 K with a single T-scalable description



Model Topology



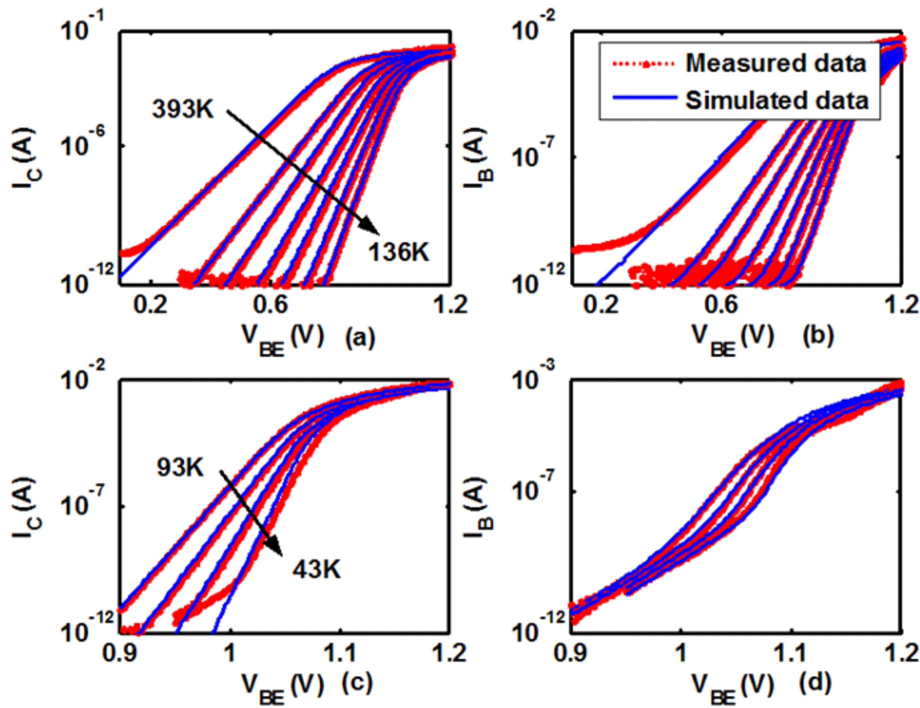
- **Based on industry standard bipolar model Mextram.**
- **Extensive new developments to enable wide temperature range modeling**
- **Accounts all important** cryo-T **physics such as freeze-out, tunneling**

DC Gummel Curves

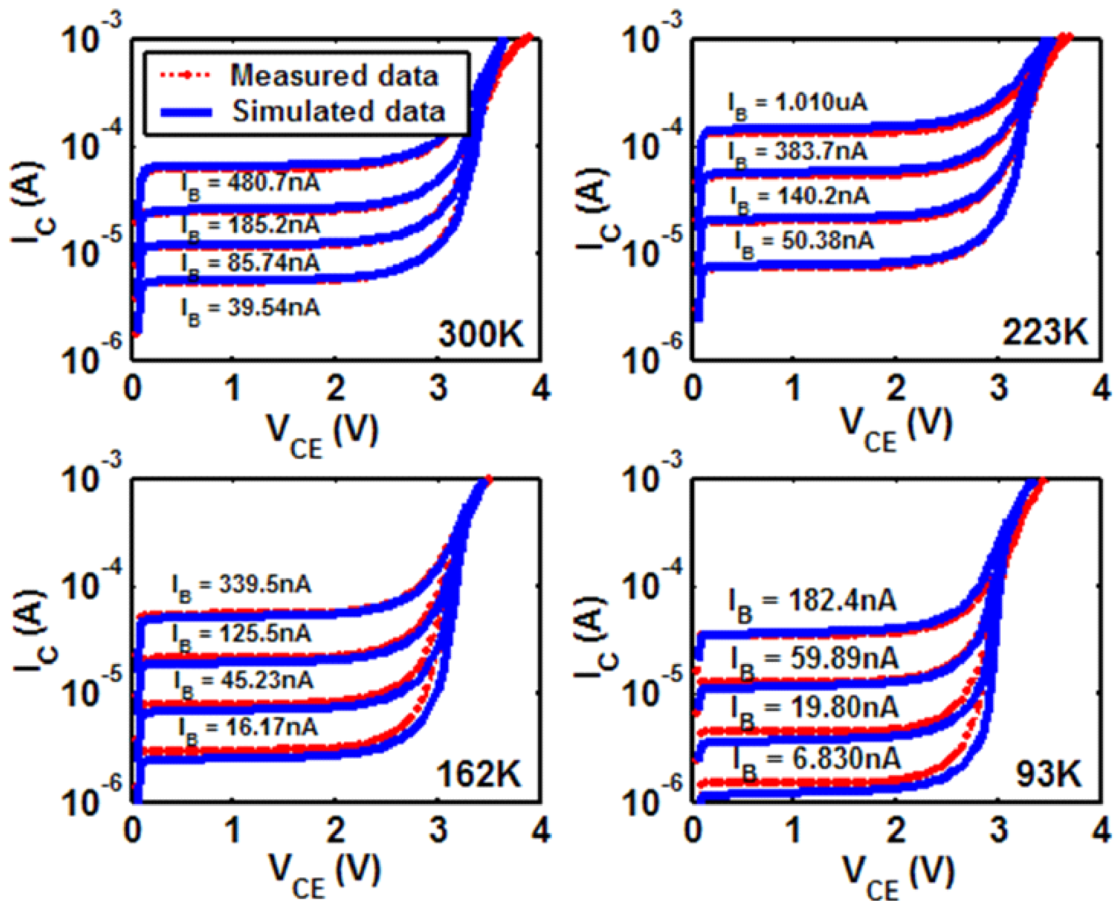
- All injection levels (Kirk effect, epi layer, resistance, crowding, self

heating)

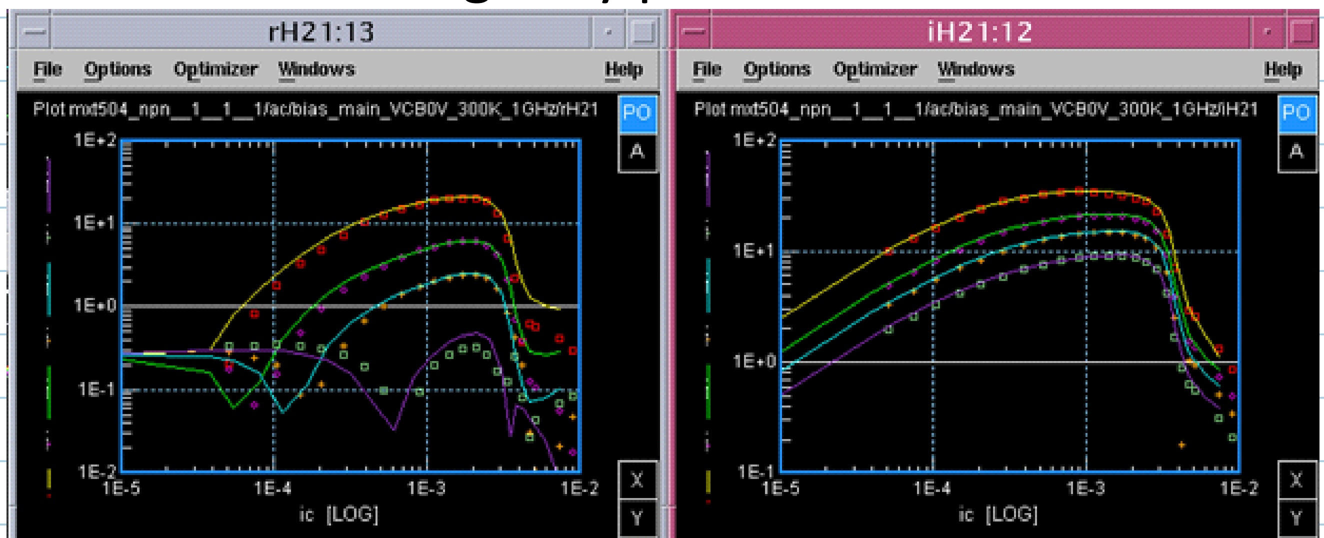
- Forward trap-assisted tunneling



DC Output Curves



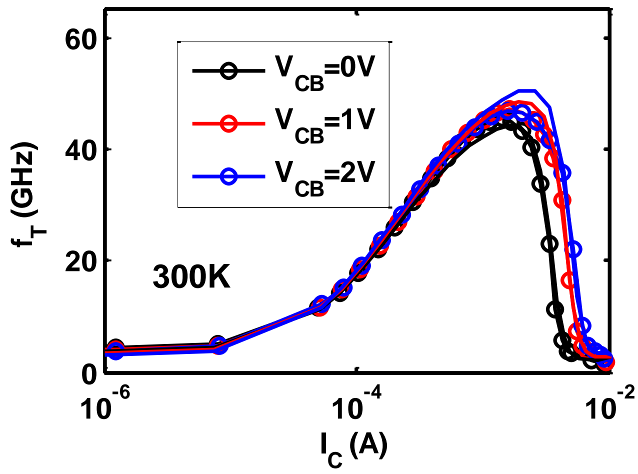
H21 Real and Imaginary parts



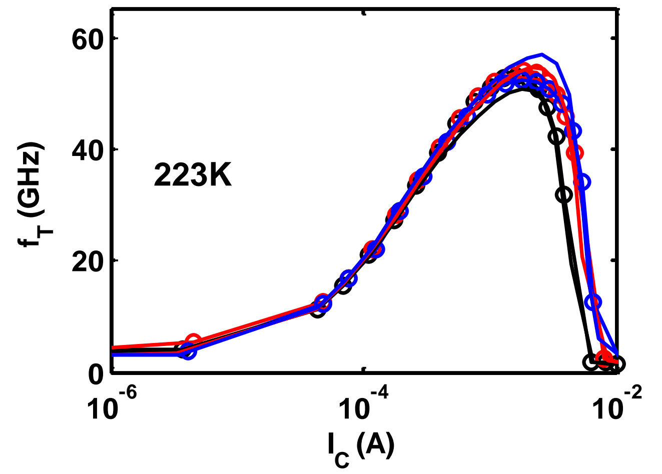
Real part@1,2,3,5GHz

Imaginary part@1,2,3,5GHz

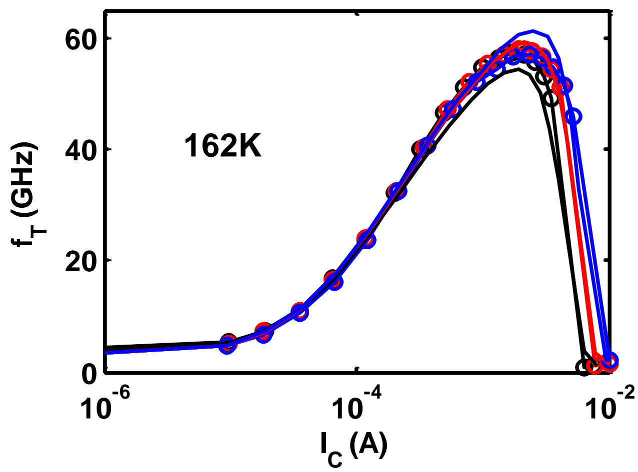
Cut-off Frequency



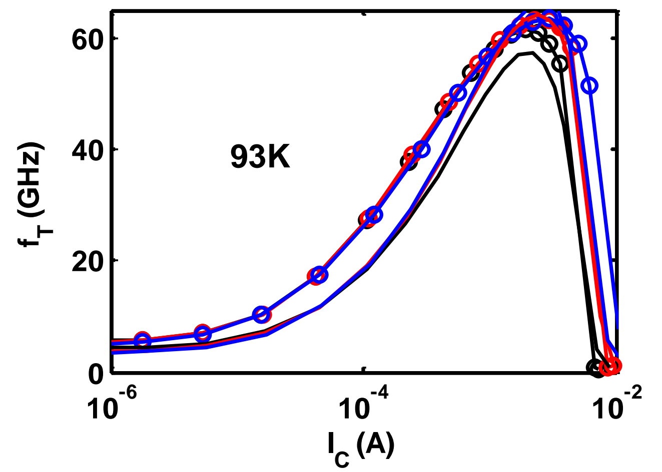
V_CB=0V
V_CB=1V
V_CB=2V
300K
f_T (GHz)
I_C (A)



223K
f_T (GHz)
I_C (A)



162K
f_T (GHz)
I_C (A)



93K
f_T (GHz)
I_C (A)

Freeze-out

Friday, April 27, 2012
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- Classic model
- Altematt model
- Improved Altematt model

E_C

E_A

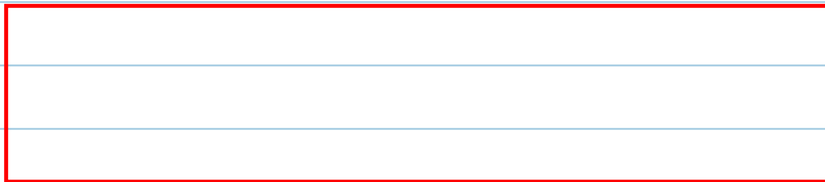
E_{dop}

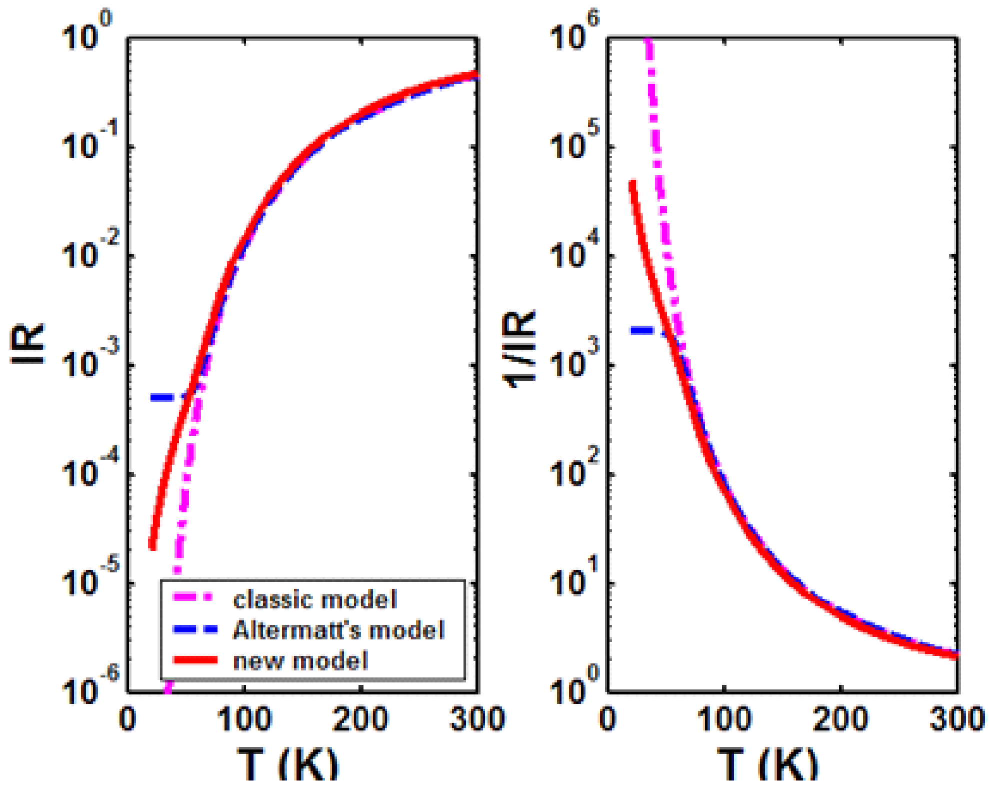
E_F

$$N^-_{dop} = N_{dop} \times f(E_A) = \frac{N_{dop}}{1 + g_A \exp(\frac{E_A - E_F}{kT})}$$

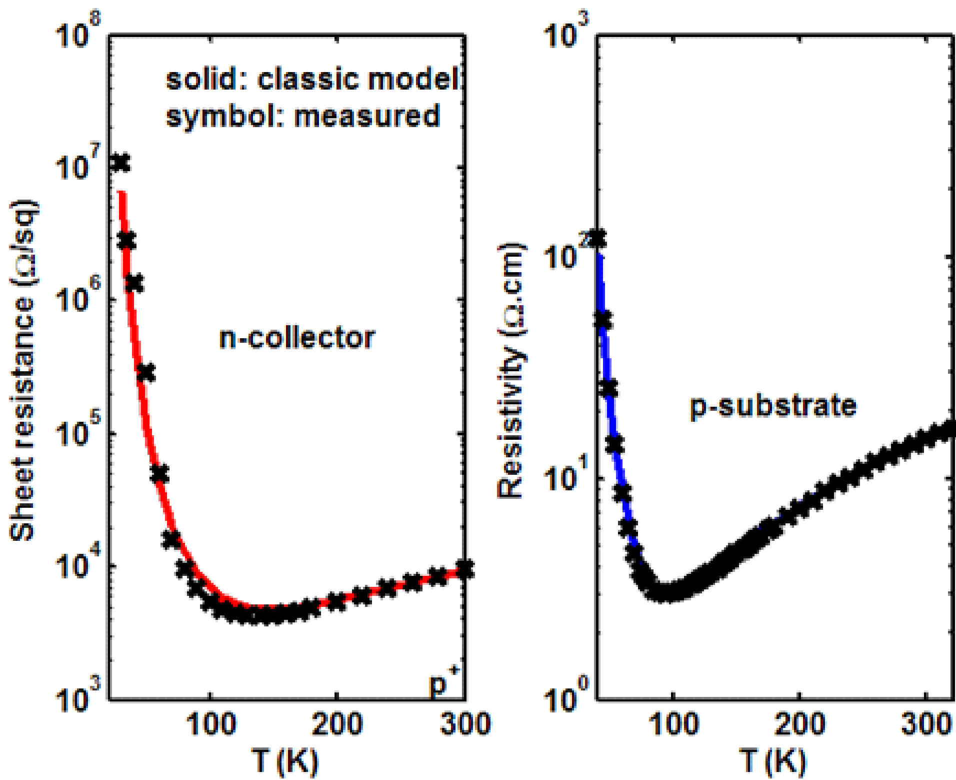
$$N^-_{dop} = (1-b)N_{dop} + bN_{dop} \times f(E_A)$$

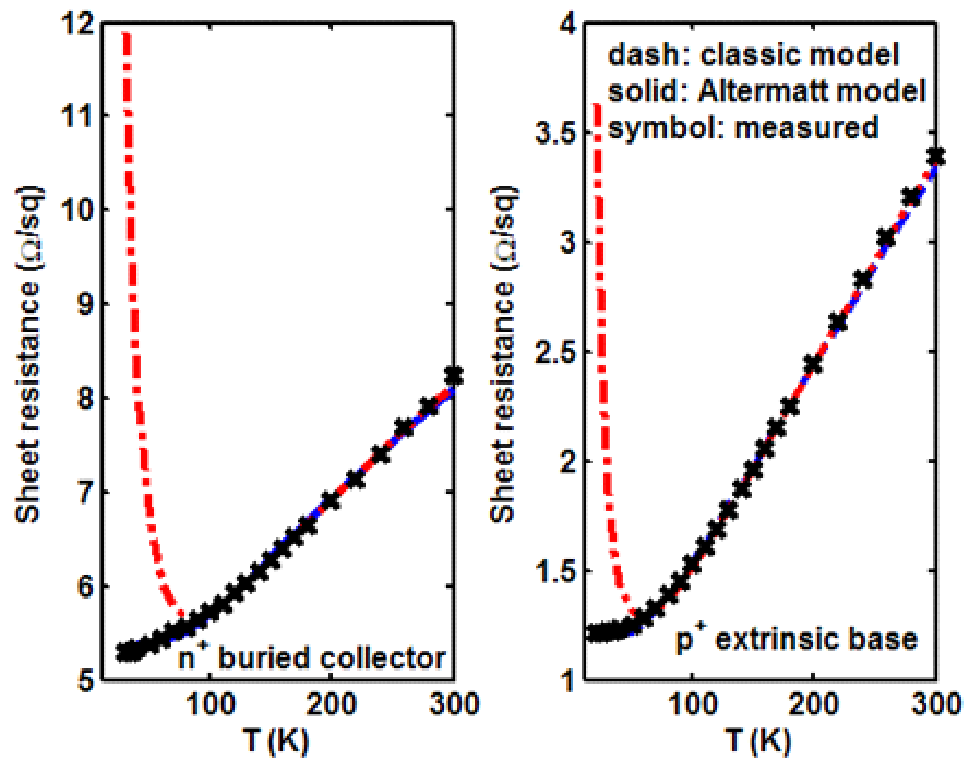
Altematt's model





Light and Heavy Doping R-T

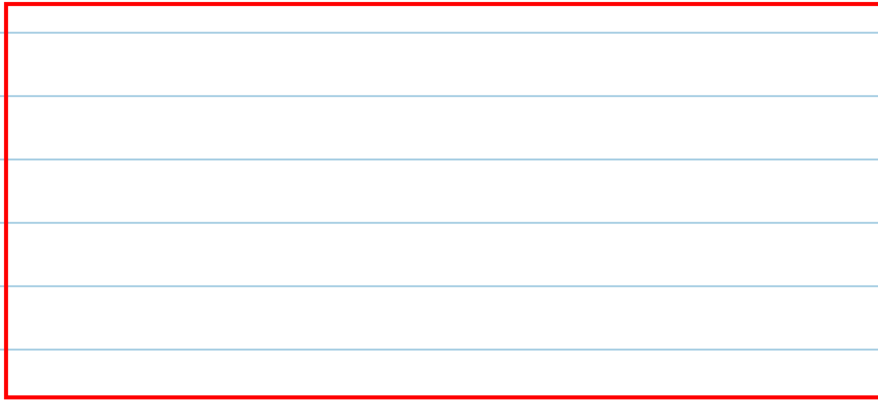




The popular approach of simply reducing ionization energy at high doping does not work at low T!

Why?

Once T is sufficiently low so kT is comparable to the Ea, you start having incomplete ionization again!



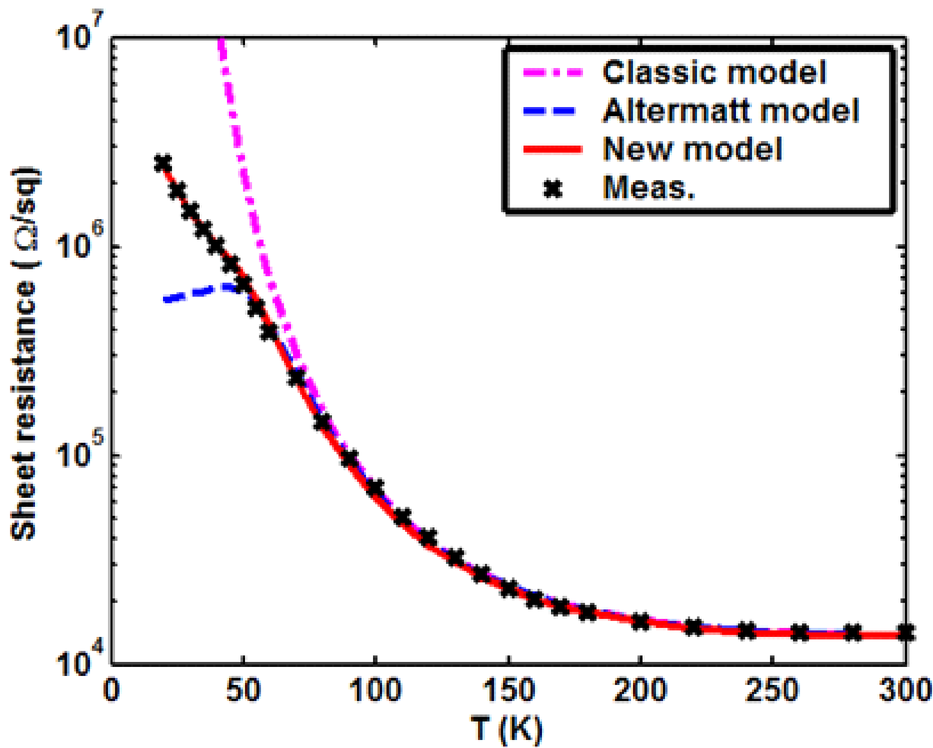
Our new IR Model

Intrinsic Base R-T

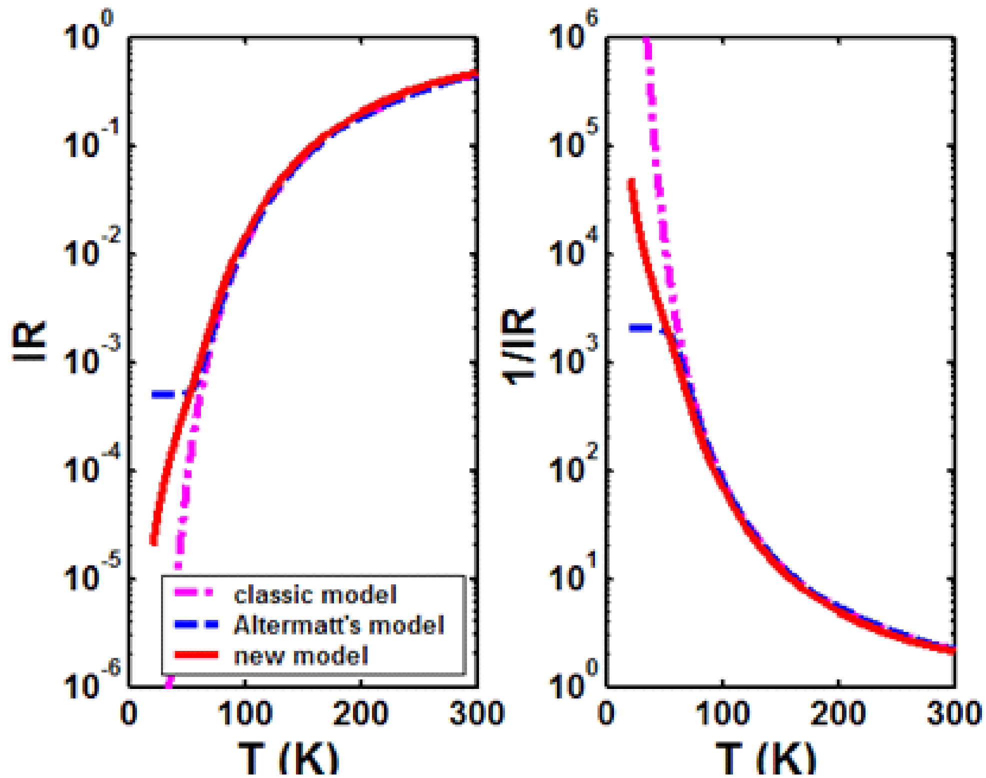
$$IR(T) = \frac{-G + (1-b) + \sqrt{[G-(1-b)]^2 + 4G}}{2}$$

$$G = g_A^{-1} \frac{N_V}{N_{dop}} \exp(-\frac{E_{dop}}{kT})$$

- Bound state fraction "b" is not constant over T and needs to be made T-dependent!



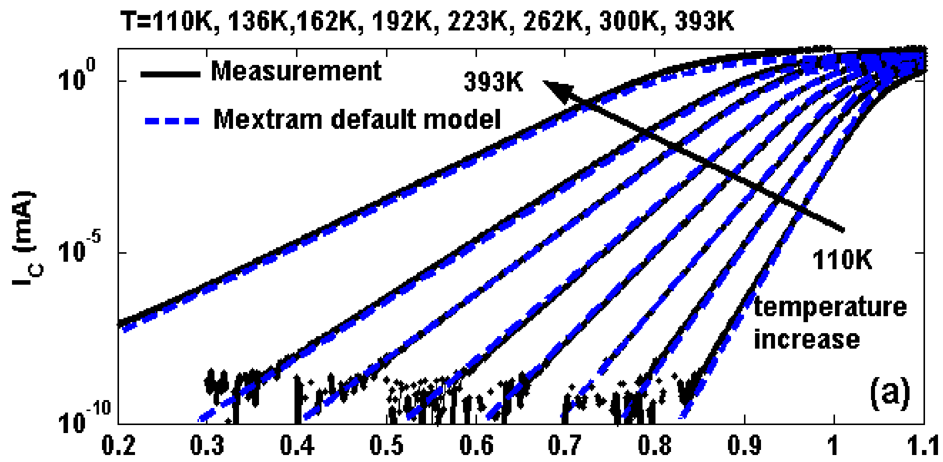
Doping level is close to Mott-transition

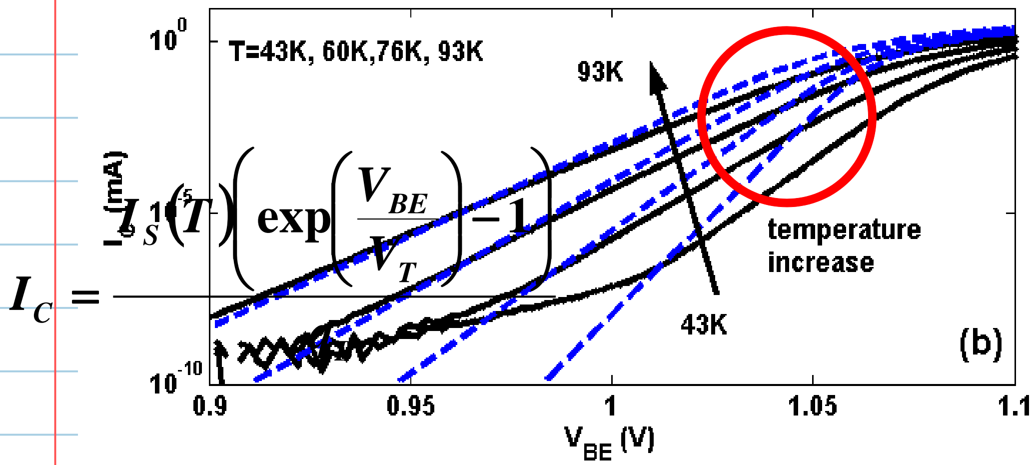


For bipolar transistors, as I will show you in a moment, **incomplete ionization rate is** NOT just a function of temperature and doping level, but **also a function of bias, or minority carrier injection** - which I call "Minority carrier injection induced dopant de-ionization"

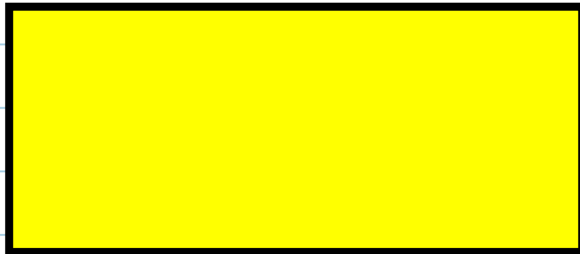
Low injection gummel

Saturday, May 05, 2012
7:34 AM





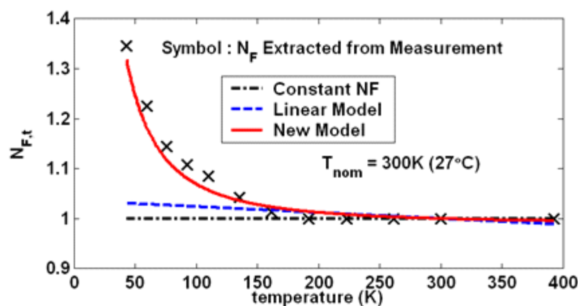
$$I_C = I_S(T)\left(\exp\left(\frac{V_{BE}}{V_T}\right)-1\right)$$

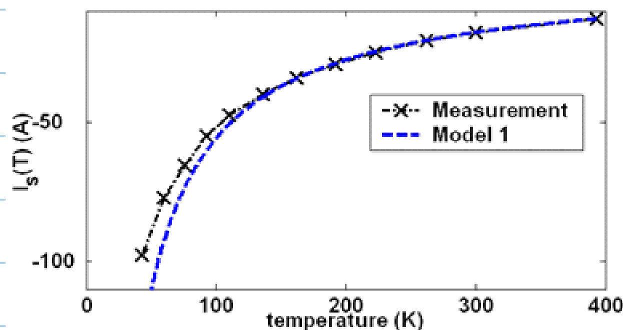


$$I_S(T) = I_{S,nom}\left(\frac{T}{T_{nom}}\right)^{X_{IS}} \exp\left(\frac{E_{a,nom}\left(1 - \frac{T}{T_{nom}}\right)}{V_T}\right)$$

T-dependence of Gummel Curves: Slope and Intercept

- Slope at low T is much less than Shockley theory prediction (NF=1)
- Intercept (IS) shows much less decrease with cooling



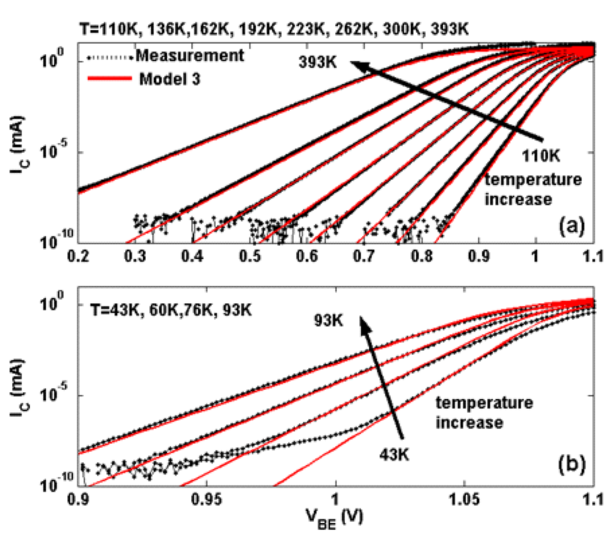


- Model and include NF(T) in I-V to make slope of IC-VBE less than Shockley theory
- **Modify IS(T) such that IS does NOT decrease as much with cooling to match measured IS(T) dependence**

$$I_S(T) = I_{S,nom}\left(\frac{T}{T_{nom}}\right)^{\frac{X_{IS}}{N_F(T)}} \exp\left(\frac{-E_{a,t}\left(1-\frac{T}{T_{nom}}\right)}{N_F(T)V_T}\right)$$

$$N_F(T) \ldots \left(\ldots \left(\ldots\right)^{X_{NF}}\right)$$

$$I_C = \ldots I_S(T)\left(\exp\left(\frac{V_{BE}}{N_F(T)V_T}\right)-1\right)$$



BGR example

Friday, April 27, 2012
12:03 PM

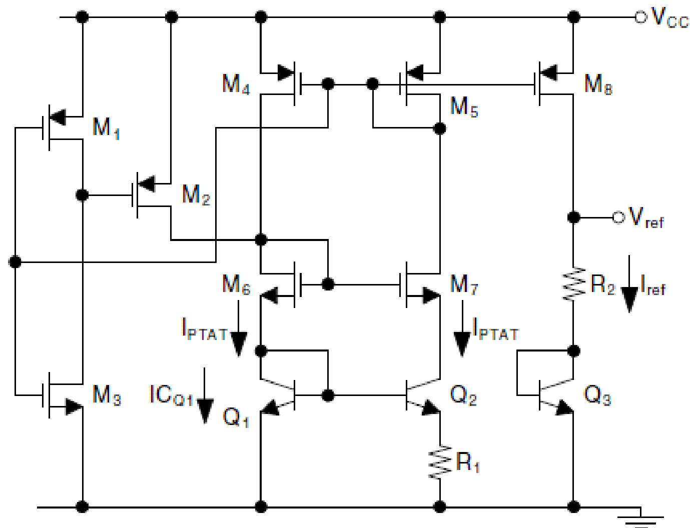
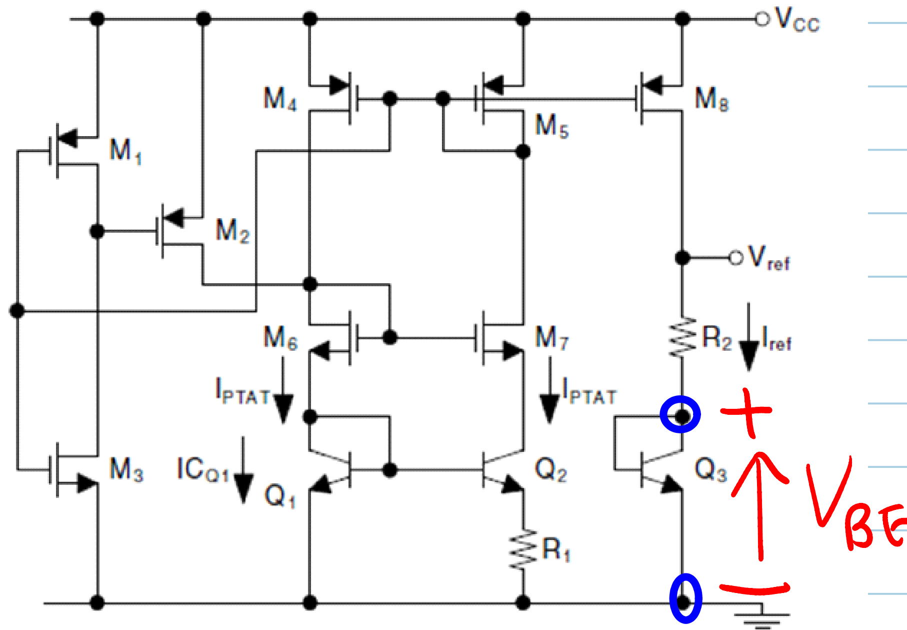


Fig. 1. Schematic of a first-order SiGe bandgap reference [2].

VBE-T



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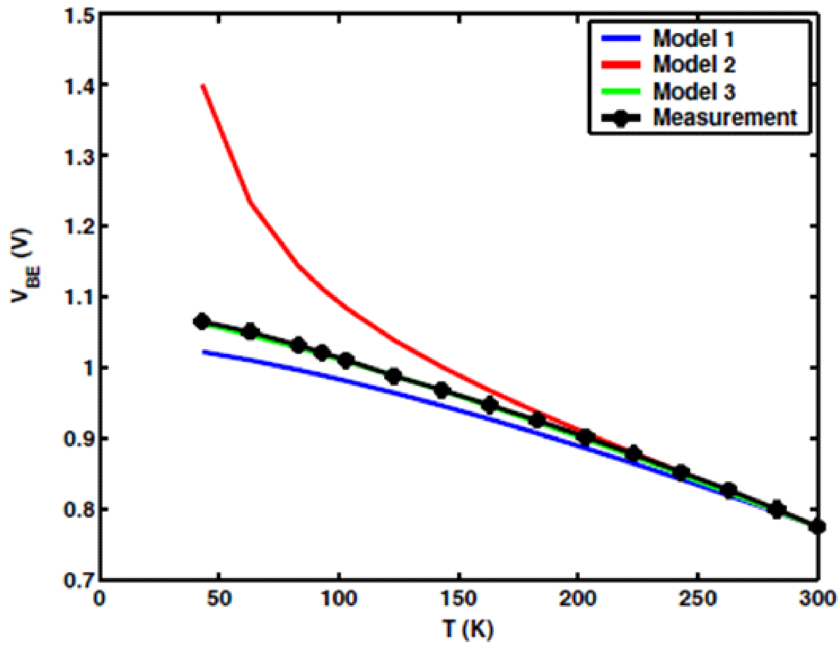
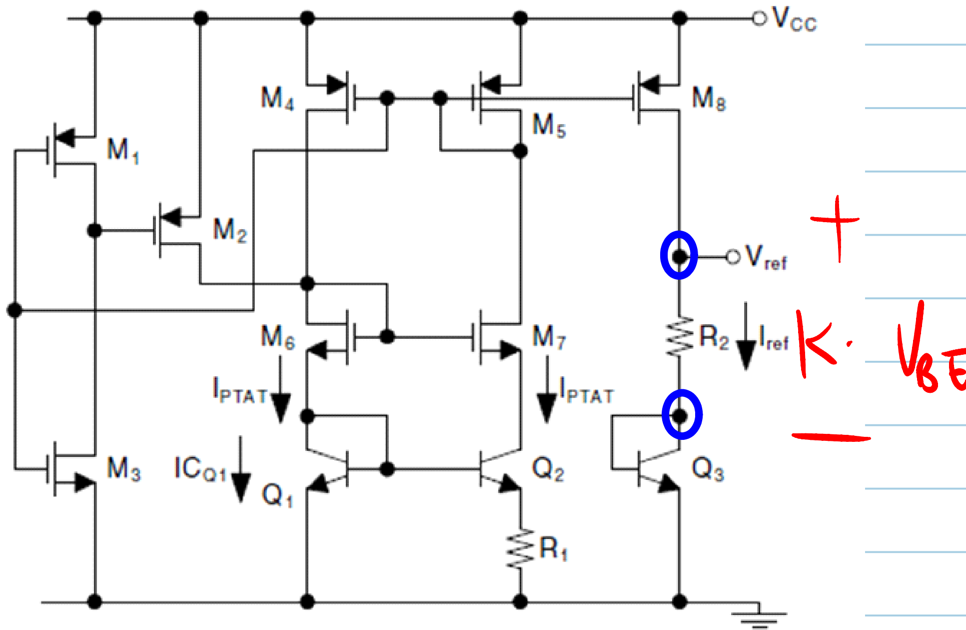


Fig. 5. Measured and modeled V_{BE} from 43-300 K.

PTAT Voltage - T



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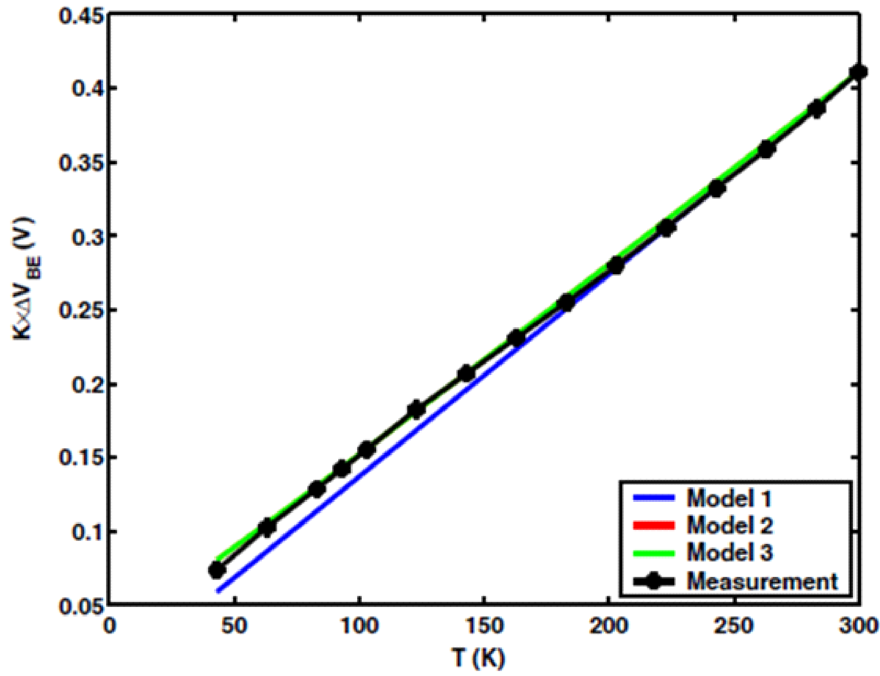
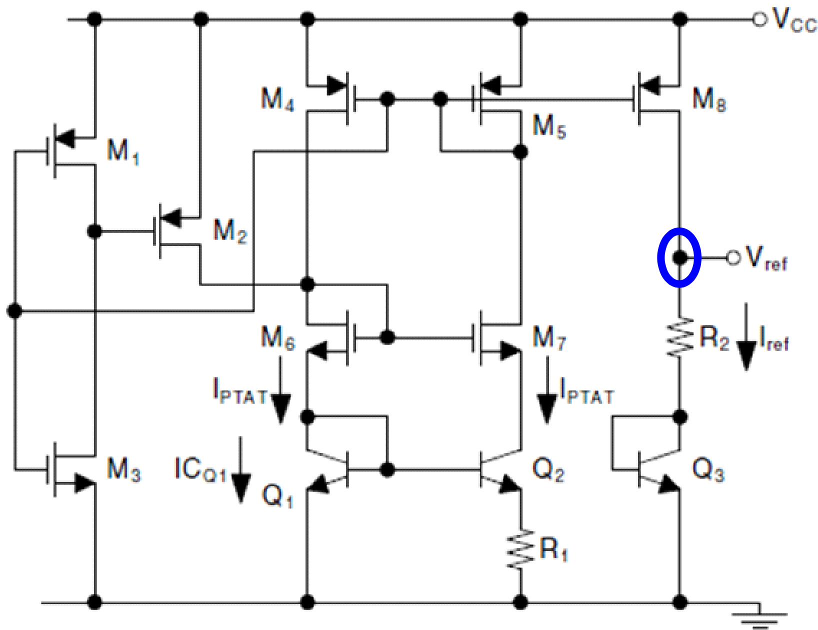


BGR Output - T



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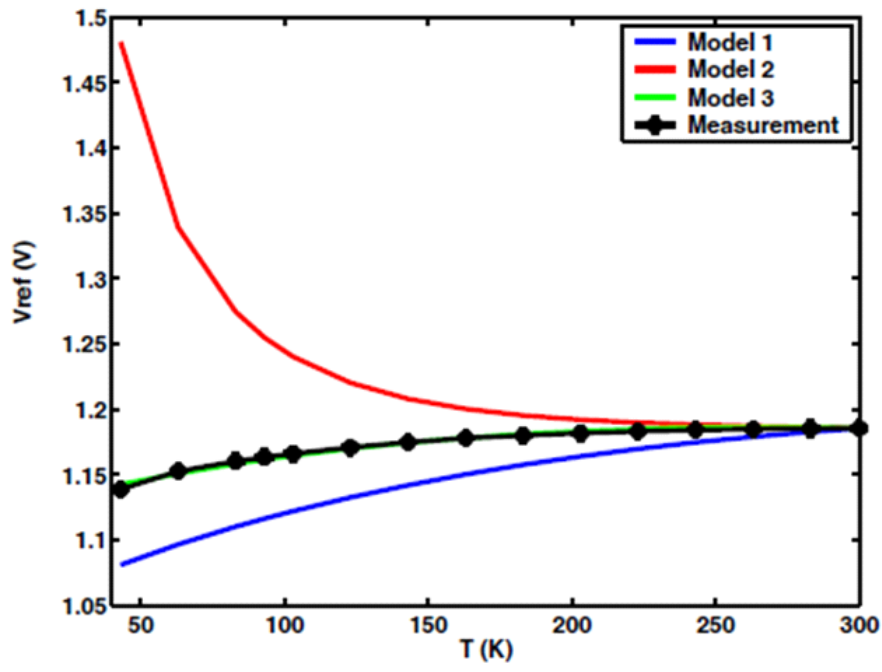
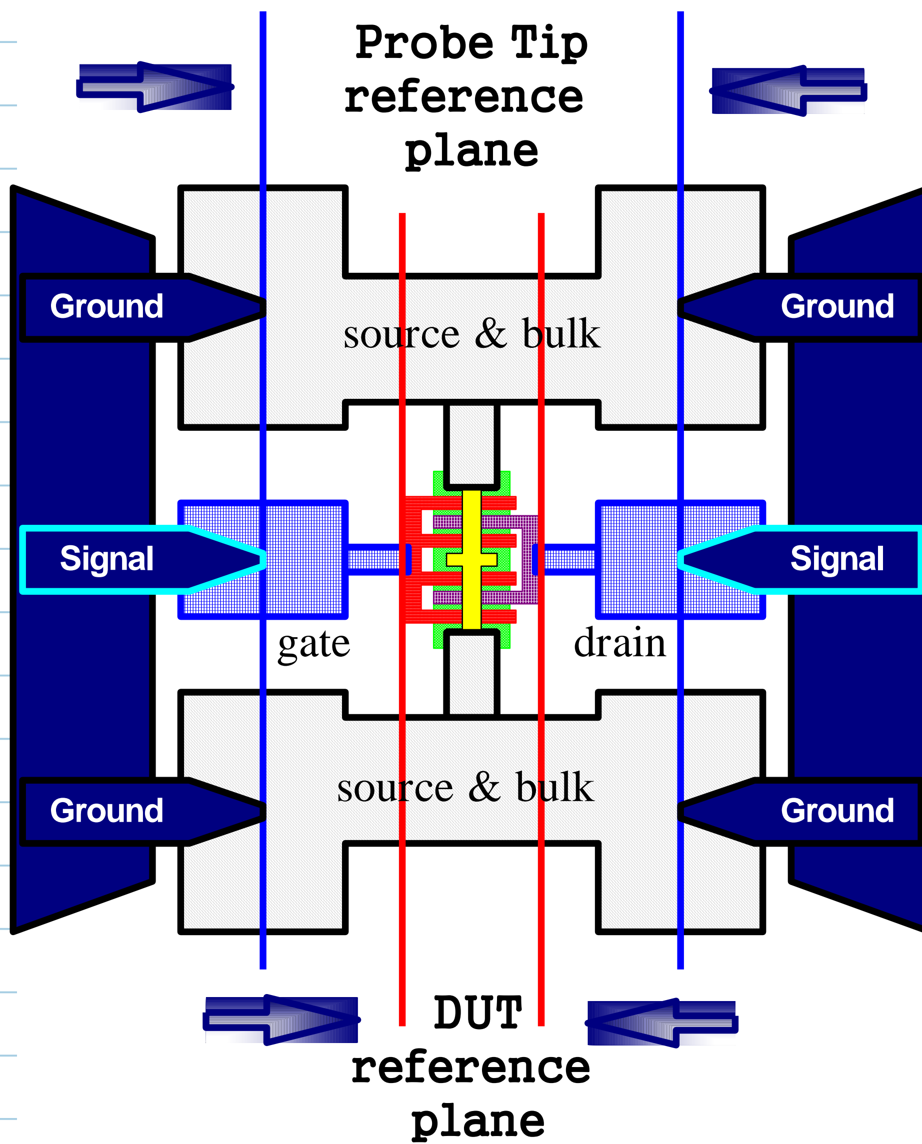
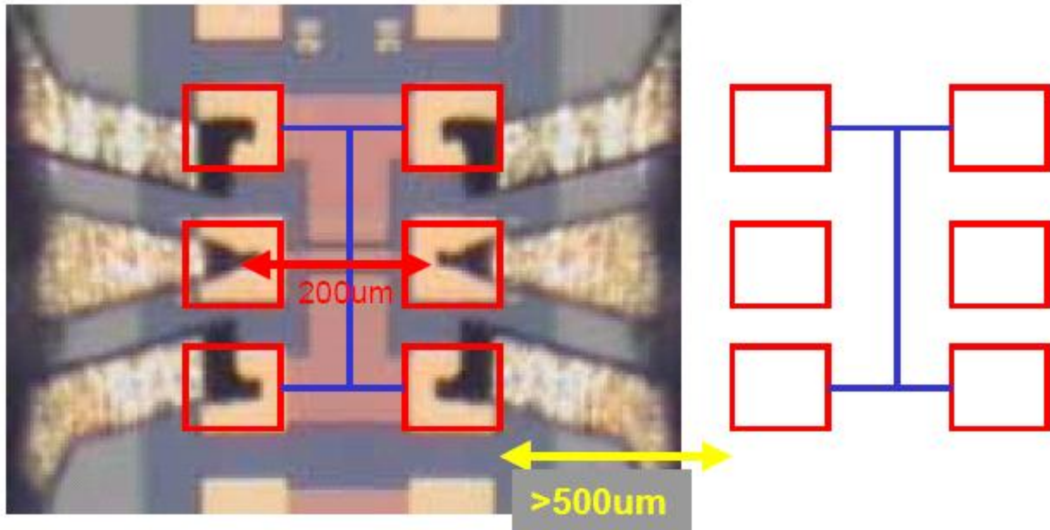


Model 1
Model 2
Model 3
Measurement
Vref (V)
T (K)
1.5
1.45
1.4
1.35
1.3
1.25
1.2
1.15
1.1
1.05
50
100
150
200
250
300

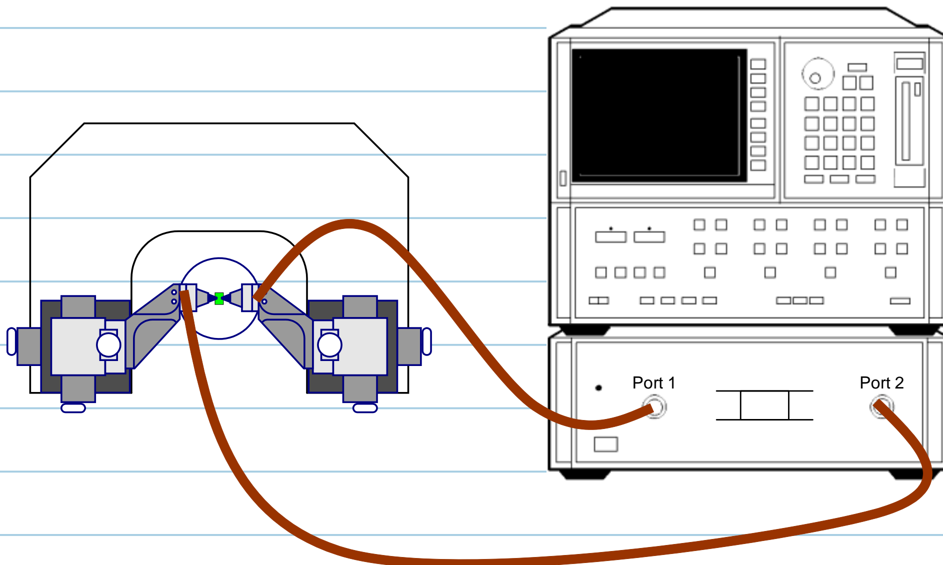
High freq (50MHz - 110GHz) on-chip measurements

Friday, August 10, 2012
12:00 PM





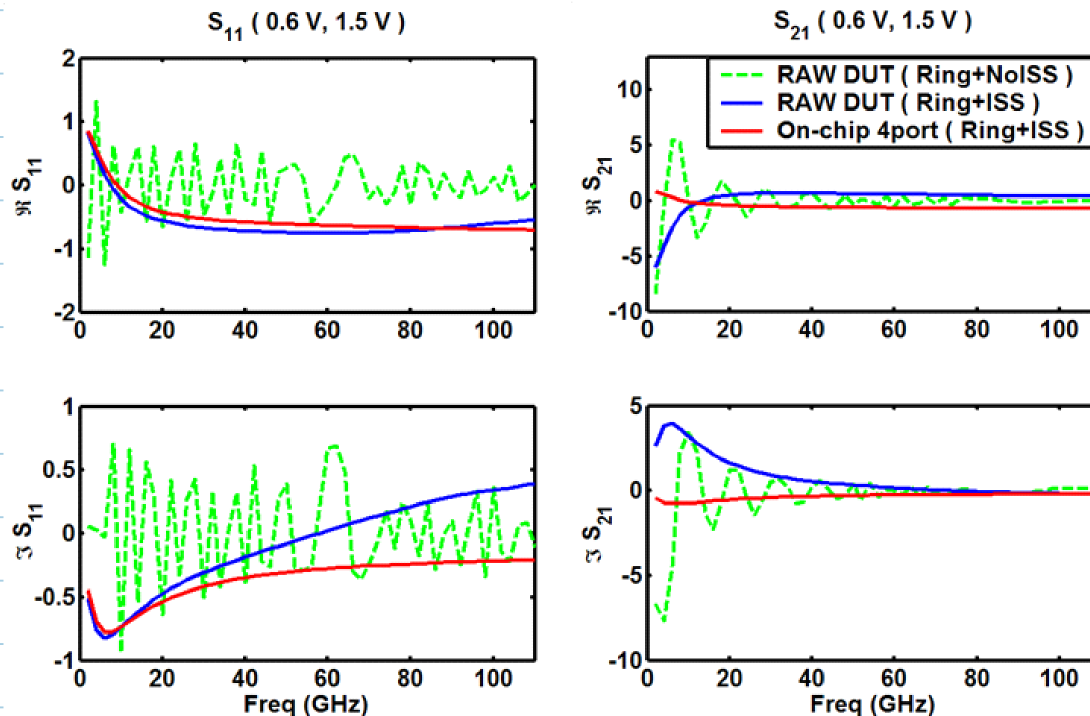
s should have more than 200um separation to avoid



A typical setup consists of a VNA with test sets, bias Tees, power supplies, cables, connectors, and probes. “Error correction” not only moves the ref plane from internal VNA ports to probe tips, but also corrects the imperfections of the VNA system, along with cables, connections and probes.
De-embedding removes effect of pads and interconnects.

All of these "jargons" may not make sense to you yet. Let us look at a 110GHz measurement on 130nm RF

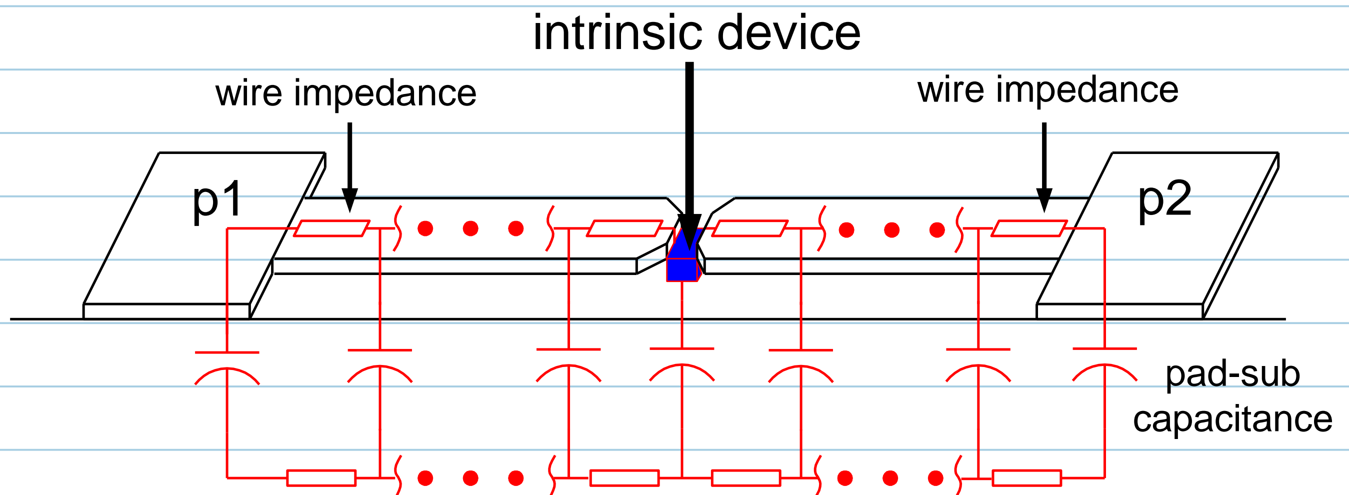
CMOS as an example:



The green is without calibration of instruments. It is nothing but junk with no usable information to us!

That calibration only works up to the point of probe tips.

We cannot directly use the probe tips to probe our transistor terminals (say on the order of 0.1um or so) - instead we can only land our probe tips on a large chunk of metal called pads (on the order of 100um), we have to use metal interconnects on chip to connect transistor terminals (small) to the metal pads.



We must then remove the effects of the pads and interconnects leading from pads to transistor terminals to obtain "true" transistor characteristics (s-parameters).

To do this, various techniques have been developed, and my group has in the past developed several techniques, some were developed or improved by students taking this course. Xiaoyun Wei's half PhD dissertation is on a new measurement technique. Qingqing Liang did pioneering work on 4-port de-embedding. Kejun Xia had some interesting simplifications of Xiaoyun's techniques.

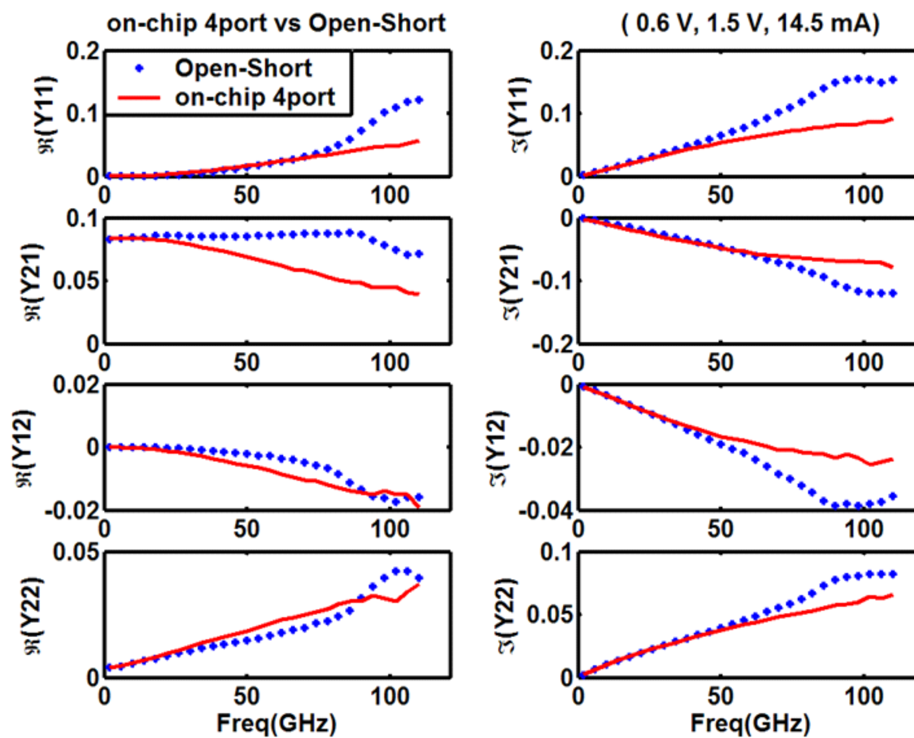
They have been used by both industry like IBM and some are commercially available in Cascade's Wincal software.

I'd like to introduce you to at least the basics of high frequency s-parameter measurement, underlying

principles of calibration and on-chip de-embedding.

We will try to find some data that can be used by you to get a feel of on-chip measurements.

On-chip 4-port vs O/S, Vgs=0.6V



On-chip s-parameter measurement - more details

Friday, August 10, 2012
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- **Standard** approach - **two step** measurement
  - Move **reference plane to probe tips using ISS calibration**
    - SOLT
    - LRRM
    - 4-port (16 term error model)
  - **Move reference plane to DUT** (Base,gate/collector,drain) – also known as "**de-embedding**"
    - Open/short (lumped)
    - "3 step" (lumped)
    - 4-port (distributed)
- **One step approach**
  - Move reference plane directly from inside VNA to DUT in a single step
  - This is routinely done with LRM by III-V folks on wafer,
  - One step is widely viewed as not applicable to Si due to lossy substrate and a few other reasons

Principle and standard practices

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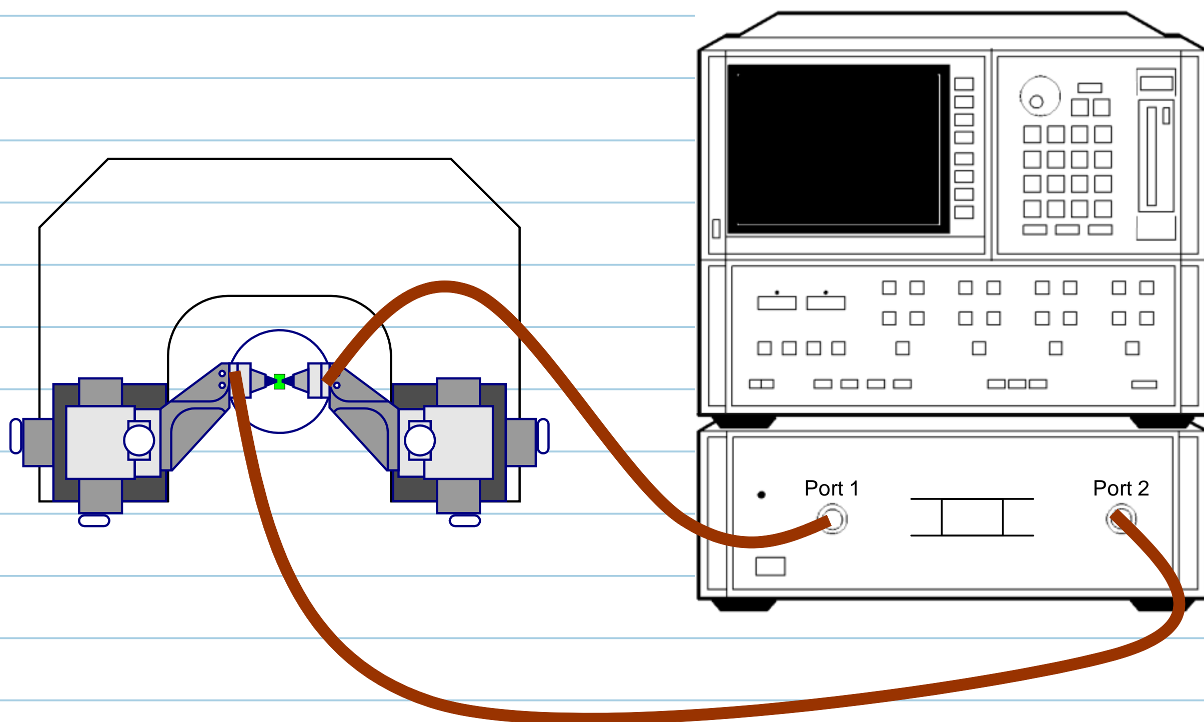


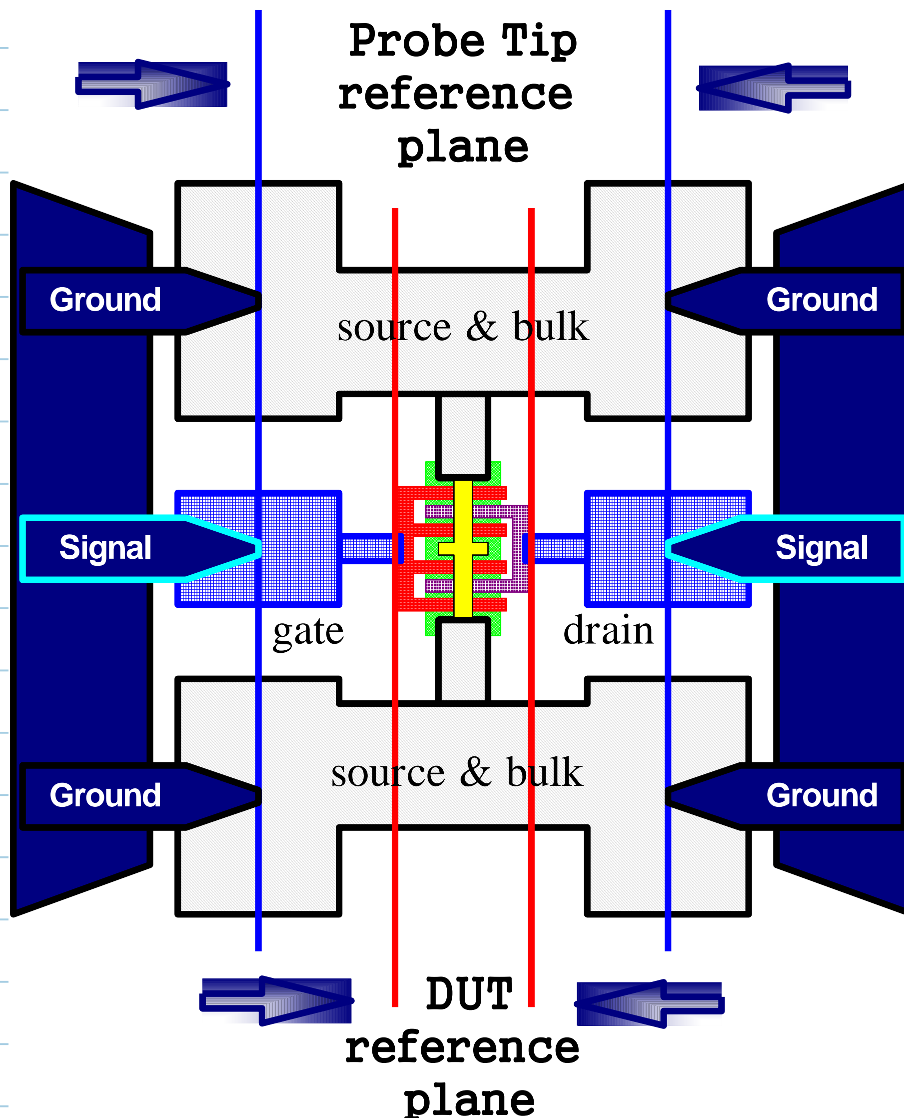
Typically we start with a process often referred to as calibration, using golden standards of various impedances (often called ISS).

After VNA system error calibration, the measurement reference plane is moved from internal VNA ports to the probe tips.

What is measured is the s-parameters of the transistor test structure that includes the transistor, the pads, and the interconnects leading to the transistor terminals (well, how that is defined will also be dependent on what you consider as part of

the transistor).

Next we need to somehow remove the pads and the interconnects from our measured s-parameters, this process is typically called de-embedding.



Let us look at a G-S probe layout and think about the cross sections to get a good feel of what is involved, with the widely used open-short model:

signal

ground

b

e/s

Y_1

Z_1

Y_3

Z_3

Z_2

c

Y_2

cut

B

Y_1

Z_1

b

e

Z_3

E

Y_3

Z_2

c

C

Y_2

signal

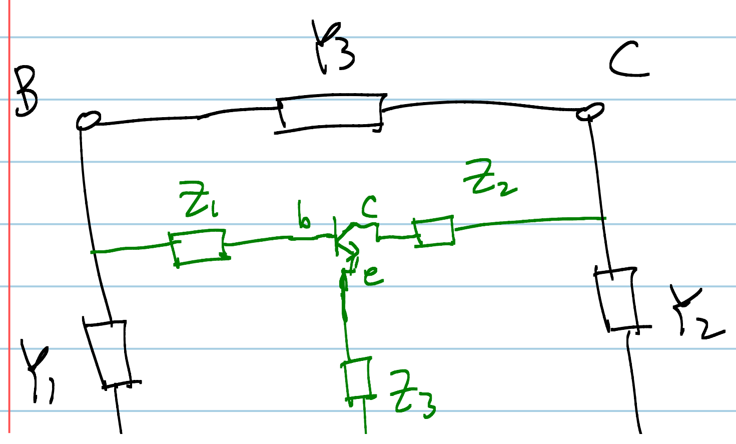
c

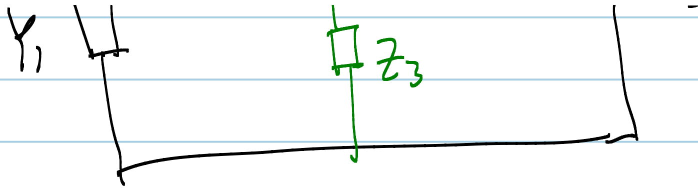
e/s

isolation/ oxide/nitride

p-substrate

A model for the pads + interconnects is thus obtained:




Y_1
Z_3

Effect of ISS calibration and de-embedding

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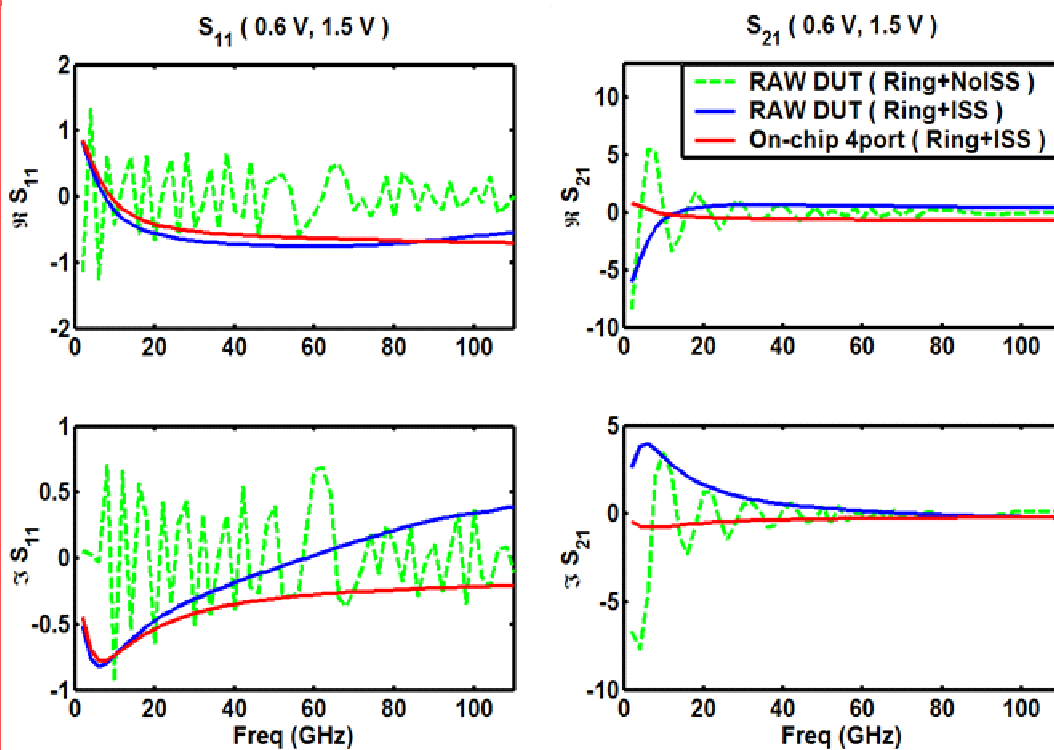
Let us look at a S11 and S21 example

a. directly measured without performing ISS calibration
b. With ISS calibration only
c. With single step calibration (VNA error + pads/interconnects)



Standard Open/Short De-embedding

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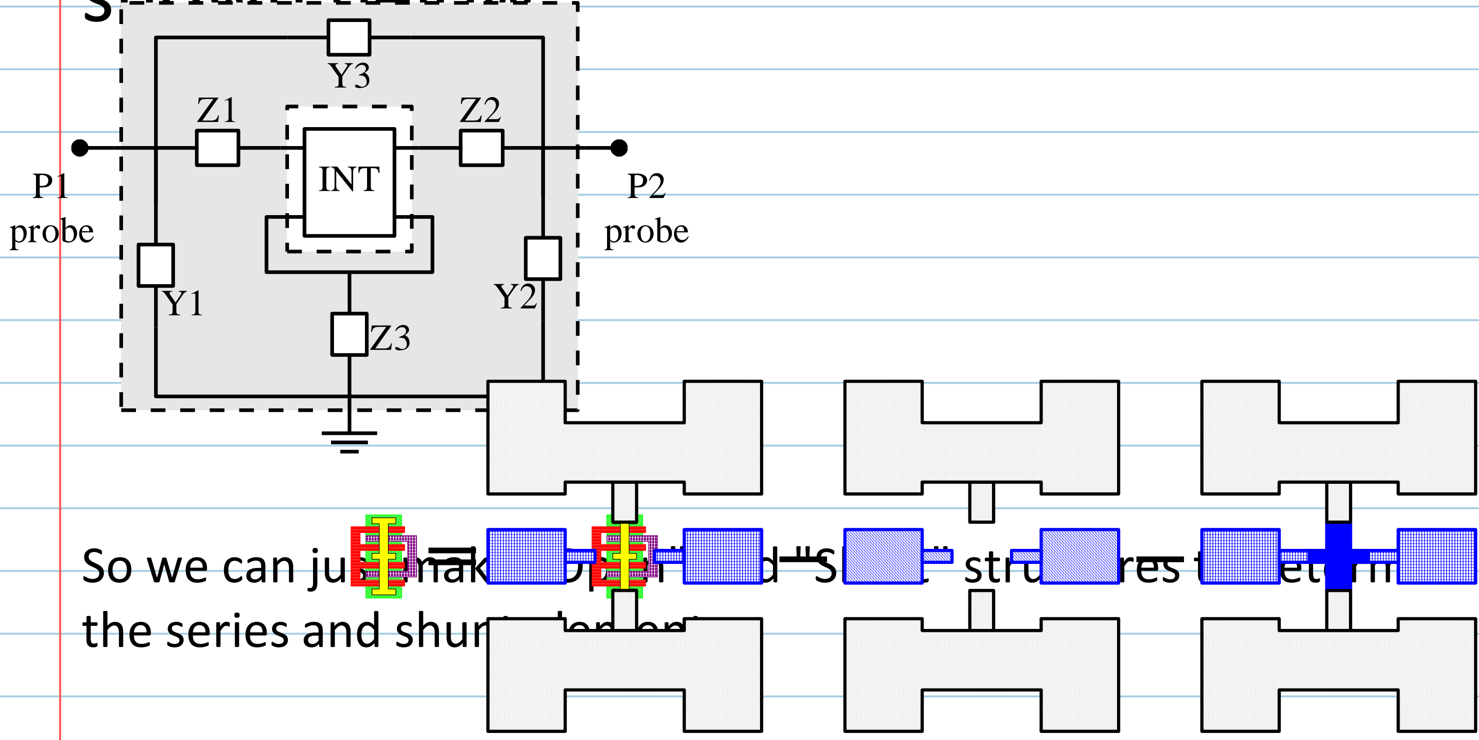
Pads and interconnects can be "lumped" into ideal series and shunt elements as shown below:



So we can ju[...] mak[...] d "S[...] stru[...]res t[...]
the series and shun[...]

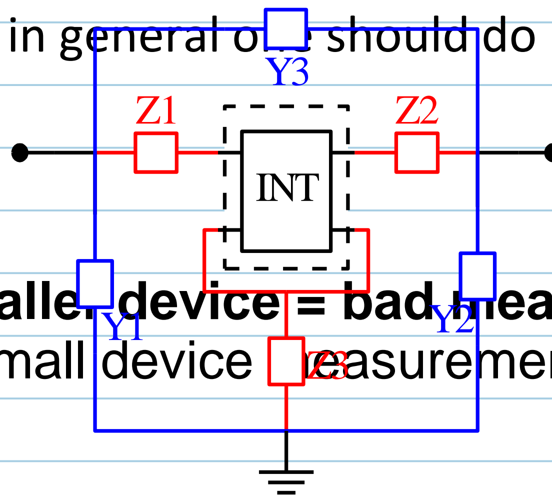
$$Y_{total\,with\,short} = Y_{total} - Y_{open}$$

$$Z_{device} = Z_{total\ with\ short} - Z_{short\ without\ open}$$

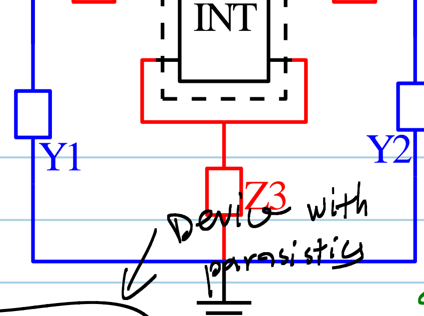
This is better than using L, C, R based equivalent circuits as it allows frequency dependence that cannot be described by L, C, R elements - which can be physically meaningful.

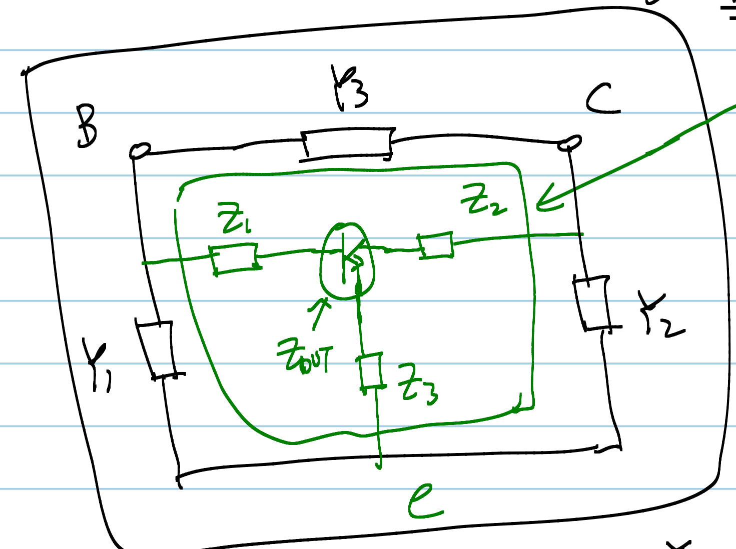
You will always do open first, and can always compare that with using open-short.

Depending on device and frequency, you may find that only open is important for you, in general one should do both open and short



Larger pads + smaller device = bad measurement, be suspicious about small device measurement data





$$Z_{TX} = Z|_{Green} - Z_{series}$$

or

$$Z|_{Green\ block} = Z_{TX} + \underbrace{\begin{bmatrix} Z_1+Z_3 & Z_3 \\ Z_3 & Z_2+Z_3 \end{bmatrix}}_{Z_{series}}$$

$$Z_{series} = (Y_{short} - Y_{open})^{-1}$$

$$Y_{green\ block} + \underbrace{\begin{bmatrix} Y_1+Y_3 & -Y_3 \\ -Y_3 & Y_2+Y_3 \end{bmatrix}}_{Y_{open}} = Y_{Device\ with\ parasitics}$$

$$\Rightarrow Y_{Green} = Y_{Device\ with\ para} - Y_{open}$$

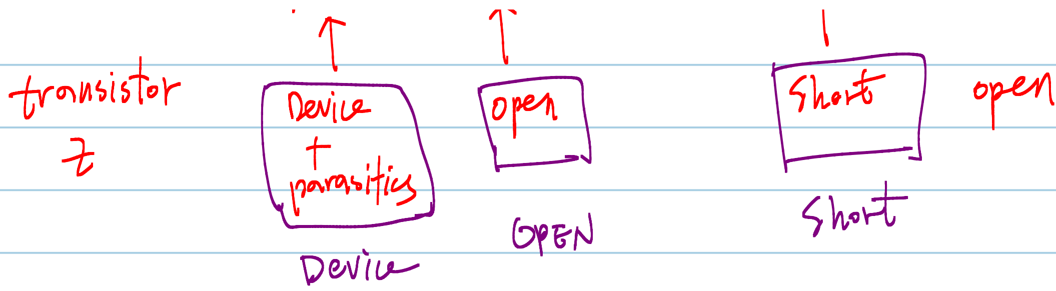
Now recall that

$$Z_{TX} = Z|_{Green} - Z_{series} \qquad Y_{Green} = Y_{Device\ with\ para} - Y_{open} \qquad Z_{Green} = Y_{Green}^{-1}$$

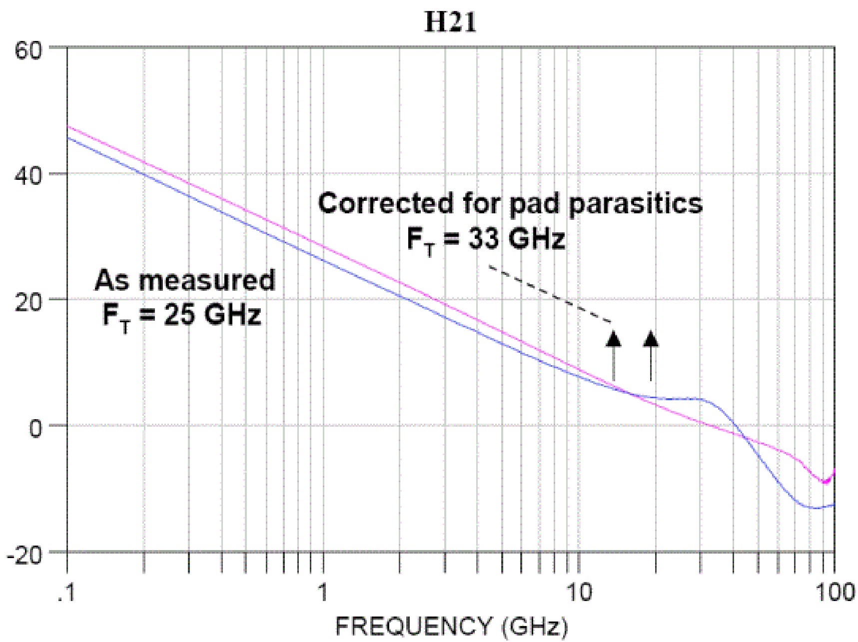
$$Y_{series} = Y_{short} - Y_{open} \Rightarrow Y_{series}^{-1} = Z_{series}$$

$$Z_{TX} = (Y_{device\ with\ para} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}$$

transistor ↑ Z_{TX}; Device ↑ $Y_{device\ with\ para}$; open ↑ Y_{open}; Short ↑ Y_{short}; open ↑ Y_{open}



* open/short can both be important, depending on device too, and the impedance at the biasing conditions.



layout

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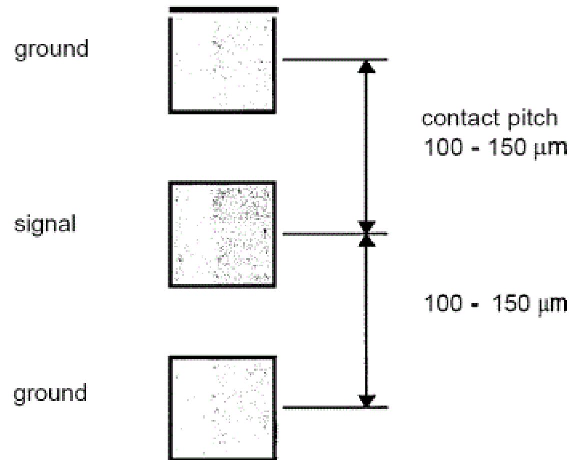
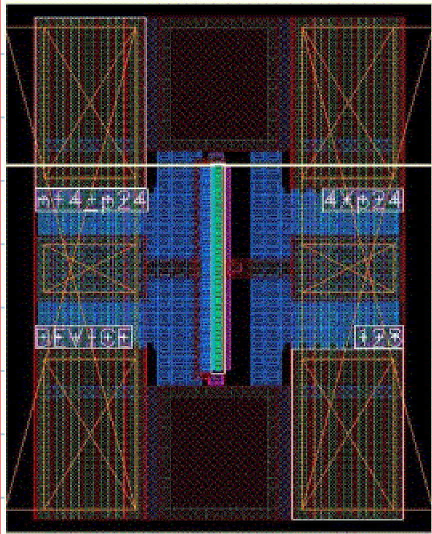
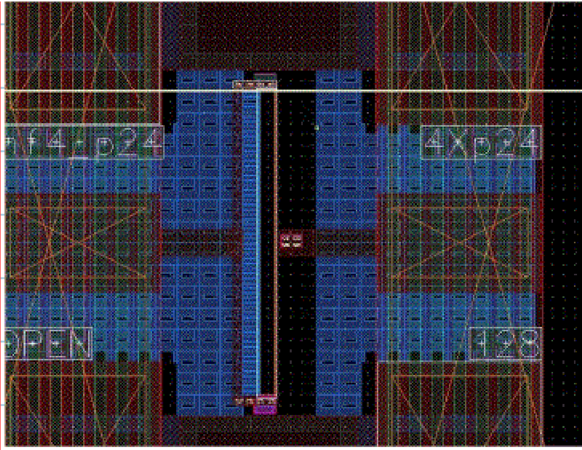
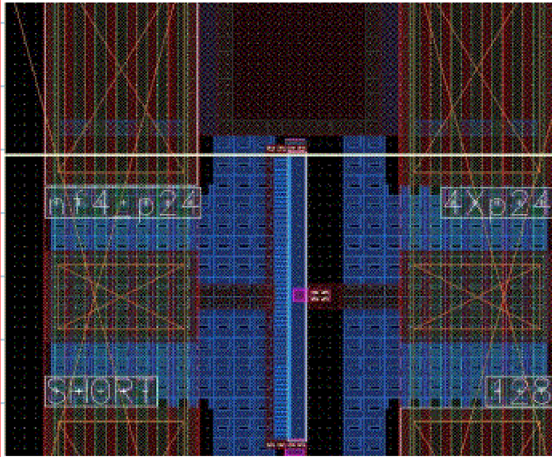


An example of large device layout




nf4_p24
4Xp24
OPEN
128


nf4_p24
4Xp24
SHORT
128

4-port

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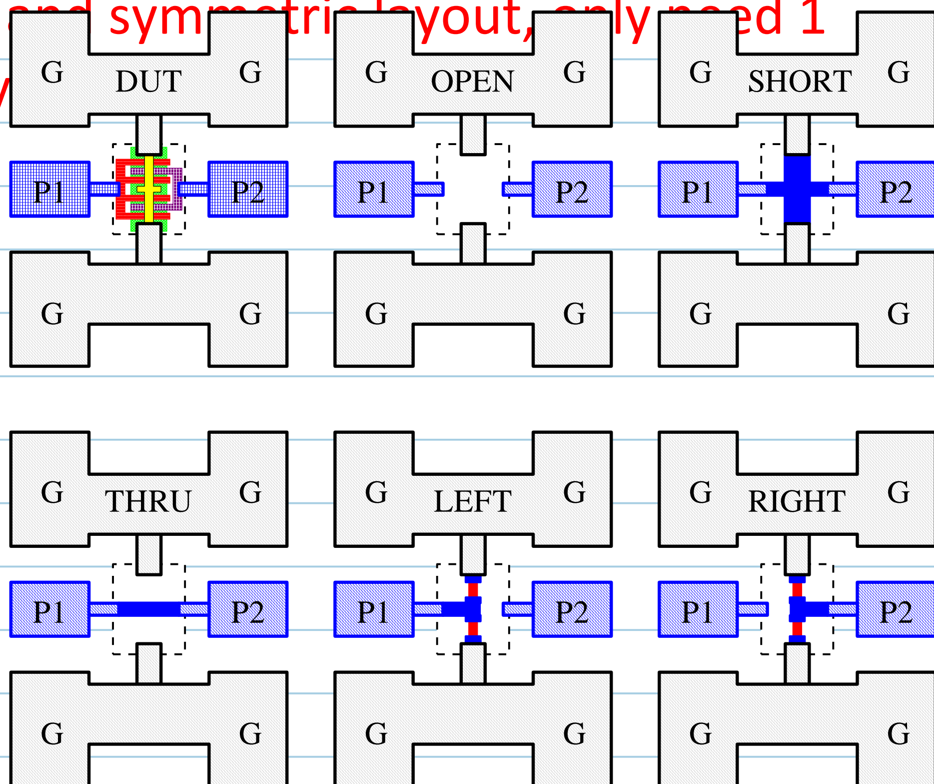
Instead of lumped circuit, we can use lumped black box for complete description

We need additional test structures:

- Three more dummies used for 4port de-embedding
- With passive and symmetric layout, only need 1 more dummy



Y_{EE} Y_{EI}

$$\begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{bmatrix}$$

Y_{IE} Y_{II}

An efficient 4-port single step algorithm - yes, we need math power

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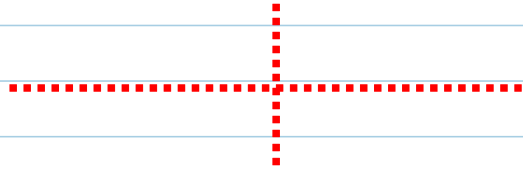
Y^{DUT} Y^{OPEN} Y^{SHORT} Y^{LEFT} Y^{RIGHT} Y^{THRU}

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$

Y^{INT}

$$\begin{bmatrix} I_e \\ I_i \end{bmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{bmatrix} V_e \\ V_i \end{bmatrix}$$



$$Y^{DUT} V_e = Y_{ee} V_e + Y_{ei} V_i$$
$$-Y^{INT} V_i = Y_{ie} V_e + Y_{ii} V_i$$

$$Y^{DUT} = Y_{ee} - Y_{ei} \left(Y^{INT} + Y_{ii} \right)^{-1} Y_{ie}$$
$$Y^{INT} = -Y_{ii} - Y_{ie} \left(Y^{DUT} - Y_{ee} \right)^{-1} Y_{ei}$$

$$\left(Y^{LEFT}-Y^{SHORT}\right)-x\left(Y^{OPEN}-Y^{SHORT}\right)=Y_{ei}\begin{bmatrix}0 & 0\\ 0 & a\end{bmatrix}Y_{ie}$$

$$\left(Y^{RIGHT}-Y^{SHORT}\right)-y\left(Y^{OPEN}-Y^{SHORT}\right)=Y_{ei}\begin{bmatrix}b & 0\\ 0 & 0\end{bmatrix}Y_{ie}$$

$$\left(Y^{THRU}-Y^{SHORT}\right)-z\left(Y^{OPEN}-Y^{SHORT}\right)=Y_{ei}\begin{bmatrix}c & c\\ c & c\end{bmatrix}Y_{ie}$$

$$Y_{ee}=Y^{SHORT}$$

$$Y^{OPEN}-Y^{SHORT}=Y_{ei}\left(Y^{open,\mathrm{int}}+Y_{ii}\right)^{-1}Y_{ie}$$

$$\left|\left(Y^{LEFT}-Y^{SHORT}\right)-x\left(Y^{OPEN}-Y^{SHORT}\right)\right|=0$$

$$Y^{LEFT}-Y^{SHORT}=Y_{ei}\left(Y^{left,\mathrm{int}}+Y_{ii}\right)^{-1}Y_{ie}$$

$$\left|\left(Y^{RIGHT}-Y^{SHORT}\right)-y\left(Y^{OPEN}-Y^{SHORT}\right)\right|=0$$

$$\left(Y^{LEFT}-Y^{SHORT}\right)-x\left(Y^{OPEN}-Y^{SHORT}\right)=Y_{ei}\left[\left(Y^{left,\mathrm{int}}+Y_{ii}\right)^{-1}-x\left(Y^{open,\mathrm{int}}+Y_{ii}\right)^{-1}\right]Y_{ie}$$

$$\left|\left(Y^{THRU}-Y^{SHORT}\right)-z\left(Y^{OPEN}-Y^{SHORT}\right)\right|=0$$

$$Y^{LO}=\left(Y^{LEFT}-Y^{SHORT}\right)-x\left(Y^{OPEN}-Y^{SHORT}\right)$$

$$Y^{RO}=\left(Y^{RIGHT}-Y^{SHORT}\right)-y\left(Y^{OPEN}-Y^{SHORT}\right)$$

$$Y^{TS}=\left(Y^{THRU}-Y^{SHORT}\right)-z\left(Y^{OPEN}-Y^{SHORT}\right)$$

$$Y_{is} = k_l Y_{ei}' \qquad m_1 = \frac{y_{12}^{TS} / y_{11}^{TS} - y_{12}^{RO} / y_{11}^{RO}}{y_{12}^{LO} / y_{11}^{LO} - y_{12}^{TS} / y_{11}^{TS}}$$

$$Y_{ei} = k_r Y_{ie}'$$

$$Y_{ii} = k_r k_l Y_{ii}' \qquad m_2 = \frac{y_{21}^{TS} / y_{11}^{TS} - y_{21}^{RO} / y_{11}^{RO}}{y_{21}^{LO} / y_{11}^{LO} - y_{21}^{TS} / y_{11}^{TS}}$$

$$Y_{ee} = Y^{SHORT}$$

$$Y_{ie}' = \begin{bmatrix} 1 & y_{12}^{RO} / y_{11}^{RO} \\ m_1 & m_1 y_{12}^{LO} / y_{11}^{LO} \end{bmatrix}$$

$$Y_{ei}' = \begin{bmatrix} 1 & m_2 \\ y_{21}^{RO} / y_{11}^{RO} & m_2 y_{21}^{LO} / y_{11}^{LO} \end{bmatrix}$$

$$Y_{ii}' = \left[Y_{ie}' \left(Y^{SHORT} - Y^{OPEN} \right)^{-1} Y_{ei}' \right]$$

$$Y^{INT} = k_r k_l \left[-Y_{ii}' - Y_{ie}' \left(Y^{DUT} - Y_{ee} \right)^{-1} Y_{ei}' \right]$$

$$Y^{LINT} = -Y_{ii}' - Y_{ie}' \left(Y^{LEFT} - Y_{ee} \right)^{-1} Y_{ei}'$$

$$Y^{left,int} = k_r k_l Y^{LINT} = \begin{bmatrix} g_l & 0 \\ 0 & 0 \end{bmatrix}$$

$$g_l = 1 / R_L \qquad k_r k_l = g_l / Y_{11}^{LINT}$$

An 1-110GHz example

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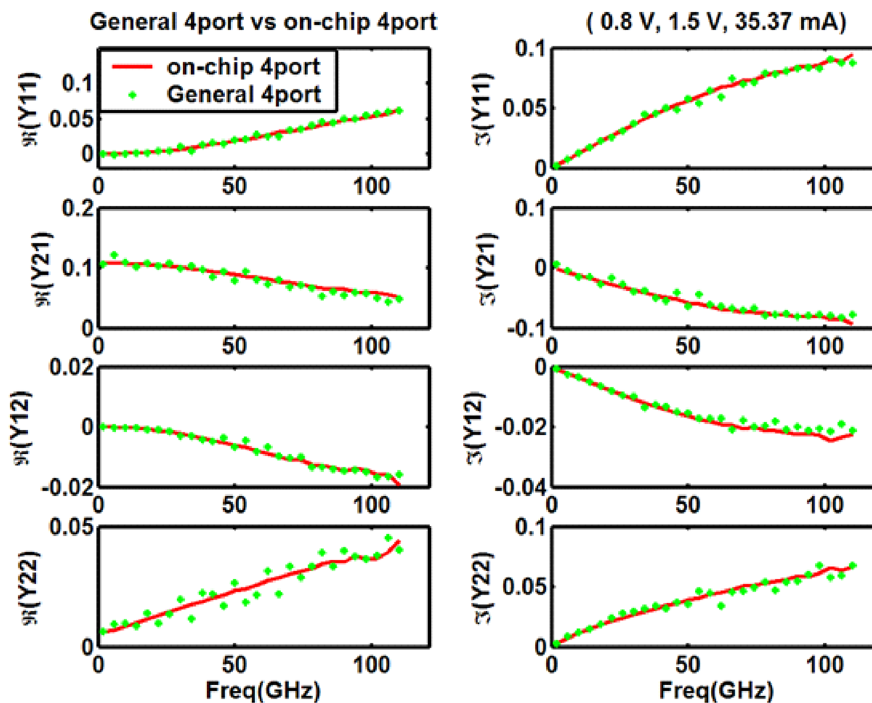
An 1-110GHz example



- General 4-port works, but with some “noise” over frequency – due to switch error which can be corrected - we have indeed done so on our own 8510C (2-40GHz)

- **Advantages:**

No need to redo calibration every few hours - need to lift probes, change substrates, and go through all the probe manipulation with swapping substrate
Faster measurement

Disadvantages:
Need to use the new algorithm - Cascade implemented one of our Single-value-decomposition (SVD) based 4 port algorithm in their Wincal calibration software

TCAD for device optimization

Friday, August 10, 2012
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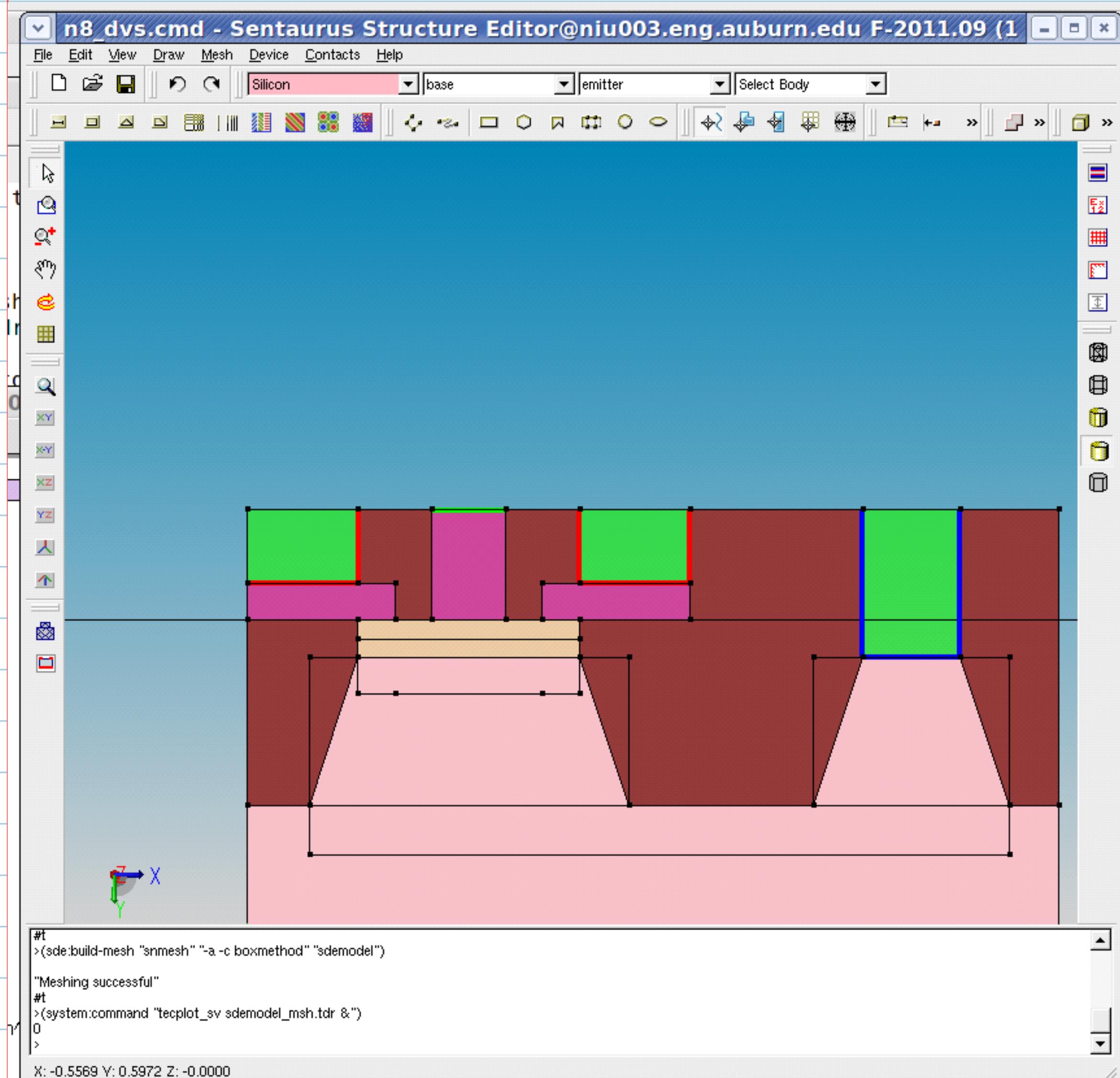
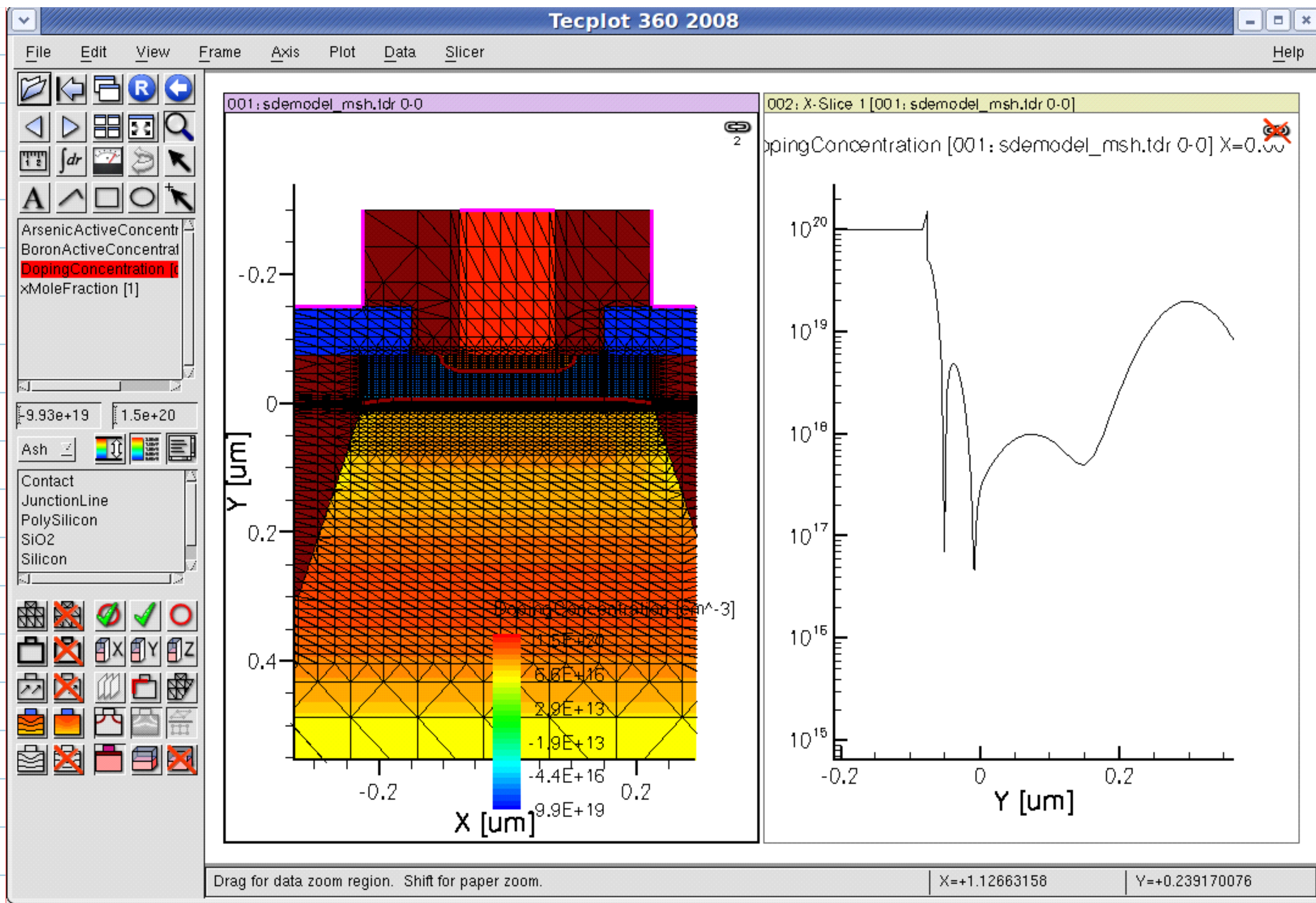
Structure building

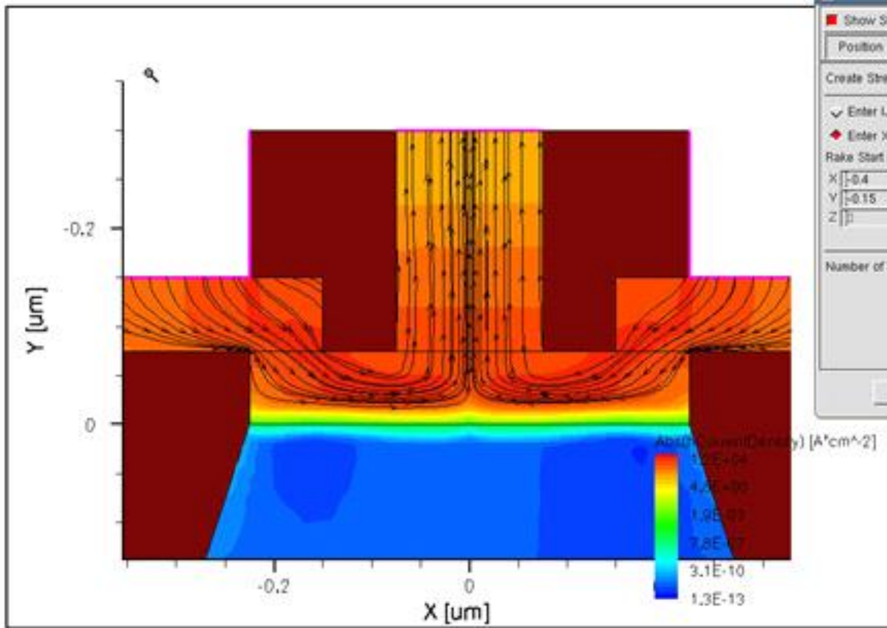


Specify doping etc, meshing,



Advanced features will also help us understand internal physics a whole lot better - with better visuals of complicated physics effects, such as 2-D distributed base current flow, emitter current crowding effect in bipolar transistors:

The picture shows how hole current flows from the base contact towards the emitter in a SiGe HBT:


Show Streamtraces
Position
Lines
Rod/Ribbon
Timing
Term Line
Integration
Create Streamtraces with Format
Surface Line
Direction
Both
Enter IJK Positions
Zone
Enter XYZ Positions
Create Rake
Rake Start Position
Rake End Position
Create Stream(s)
Streamtraces per Rake
Number of Streamtraces: 50
Delete Last
Delete All
Close
Help
Y [um]
-0.2
0
X [um]
-0.2
0
3.1E-10
1.3E-13
Drag for data zoom region. Shift for paper zoom.
X=-0.305552524
Y=-0.341069191

Cryo optimization of SiGe HBTs - a practical example

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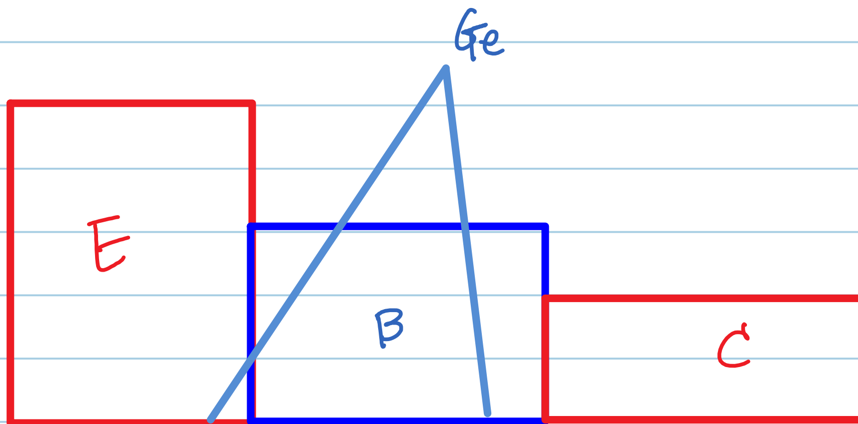
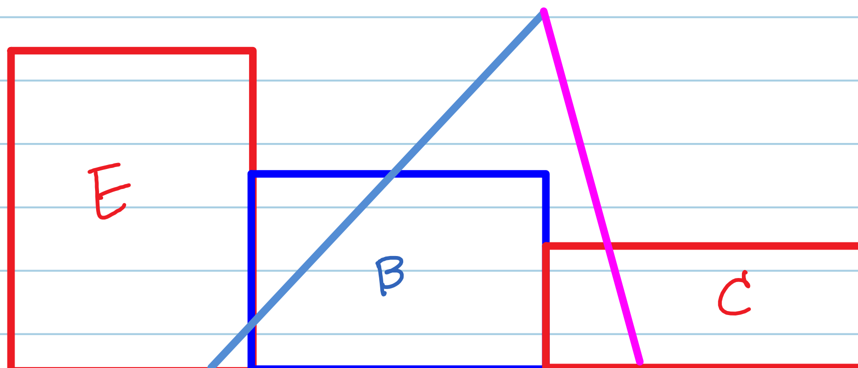
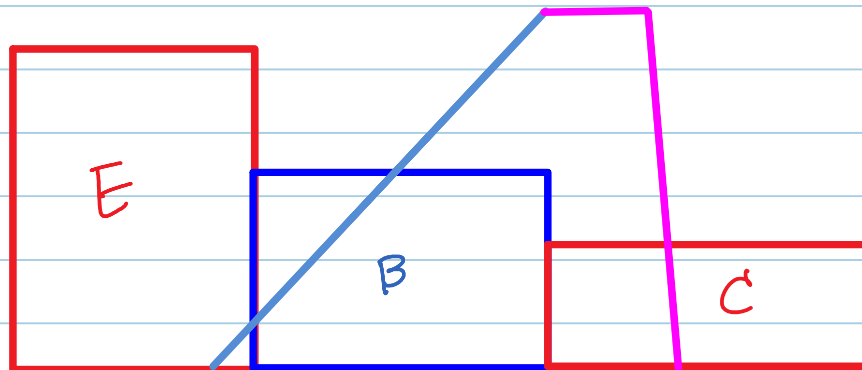
12:10 PM







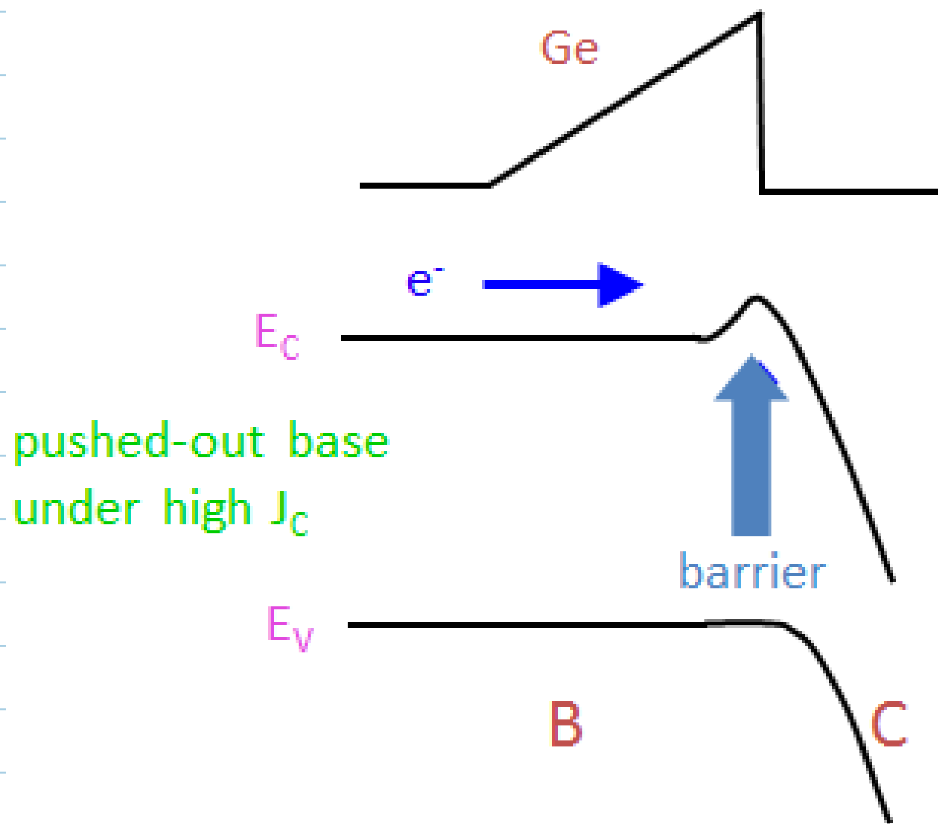
What makes ft roll off?

- Conventional wisdom: SiGe/Si heterojunction barrier

  - Ge retrograding causes a conduction band barrier at high injection

  - electrons transiting the base “see” this barrier

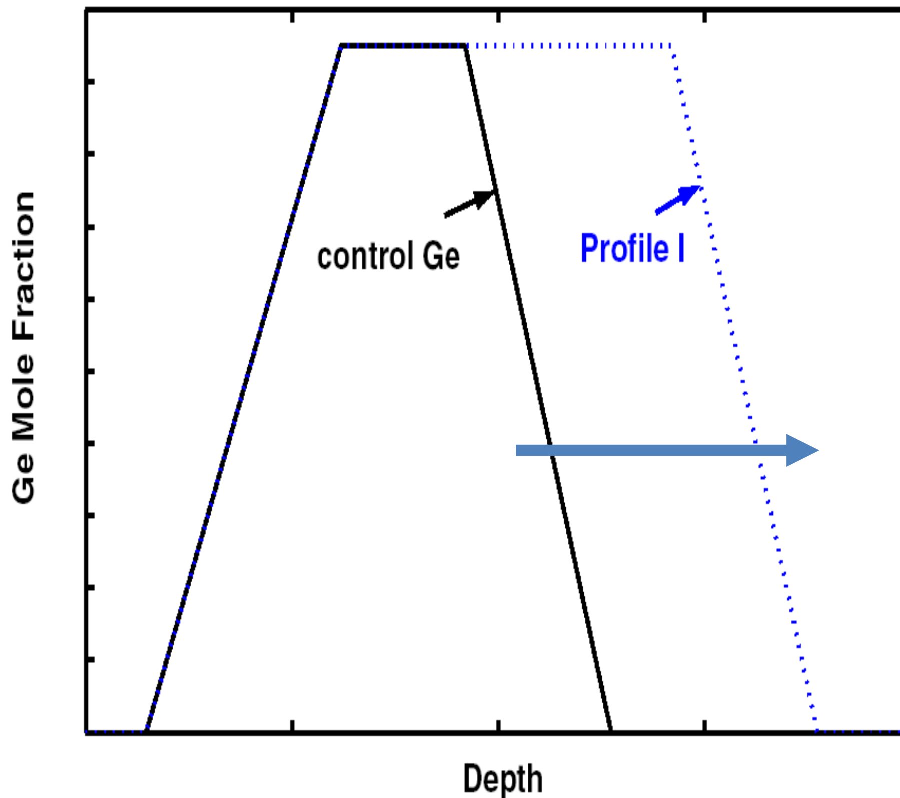
  - effect is thermally-activated and gets worse at low T!



Bandgap Engineering Implications:

Deep Ge extension into collector (with cost) is good …

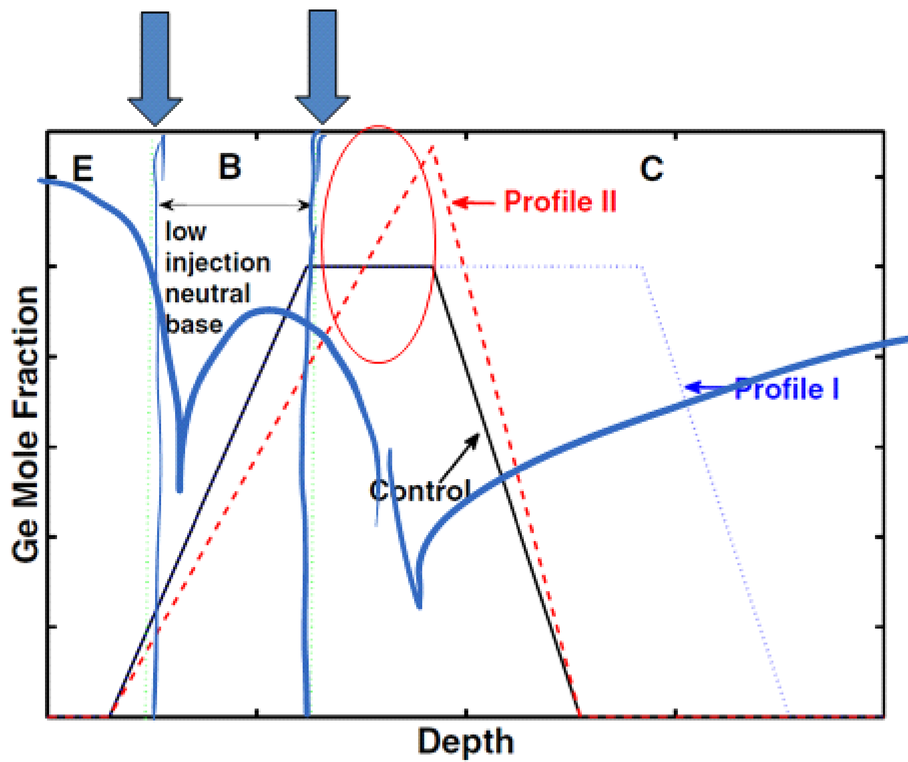
Large Ge retrograding gradient is bad!

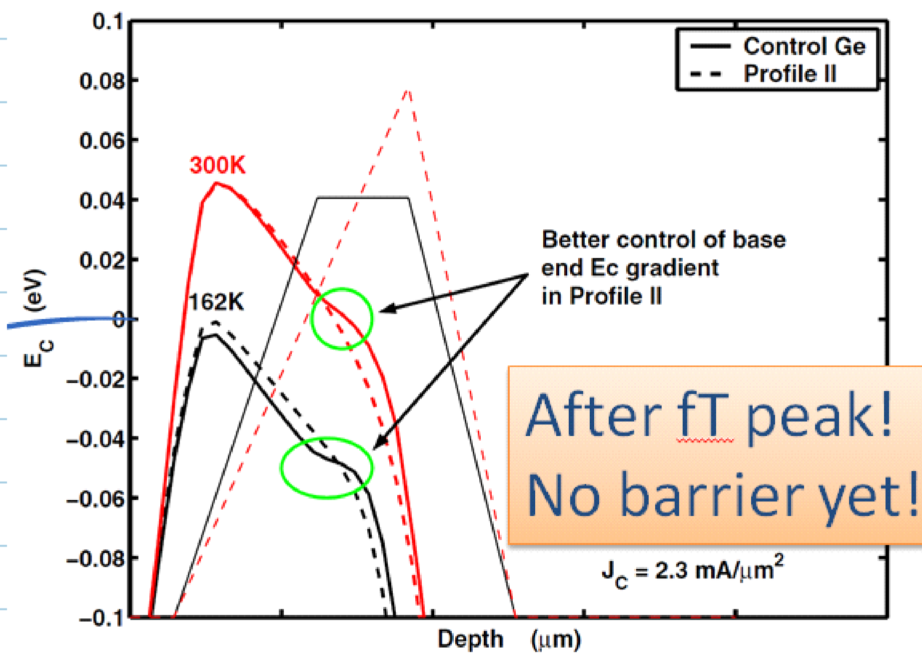


What is worse is that this does NOT work in simulation and in experiments for a HBT technology at hand. Why?

New profile design:

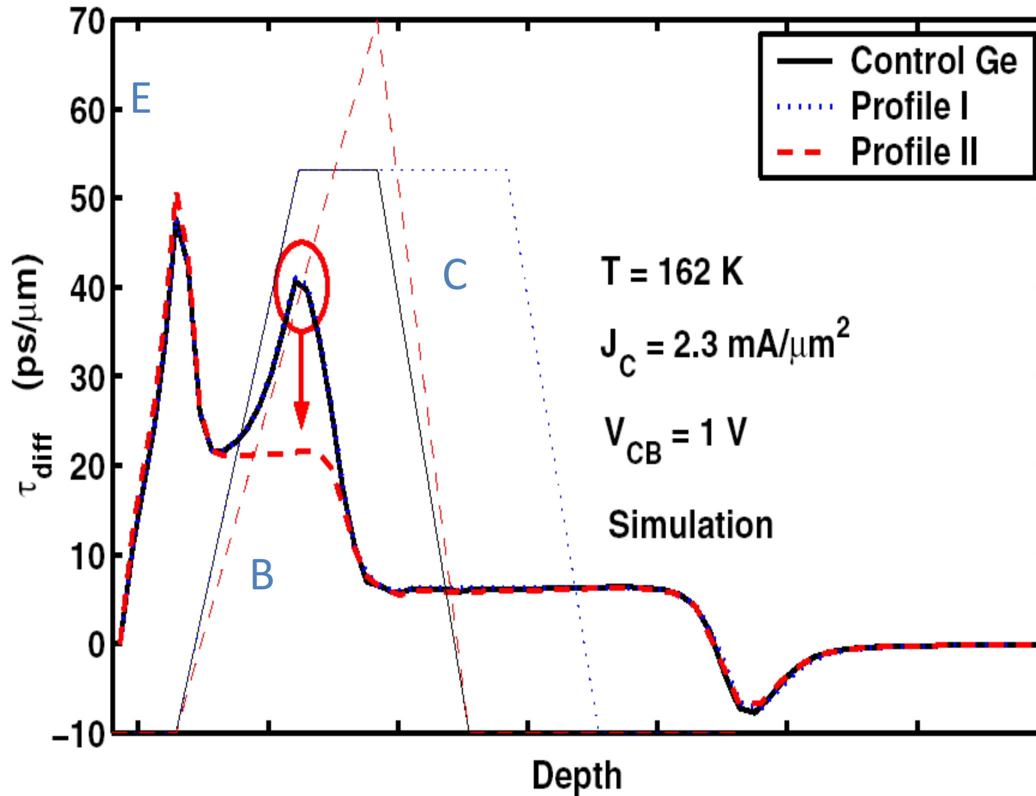
- fT rolls off well before barrier effect occurs!
- "Useless" Ge gradient in low injection CB SCR is VERY useful !





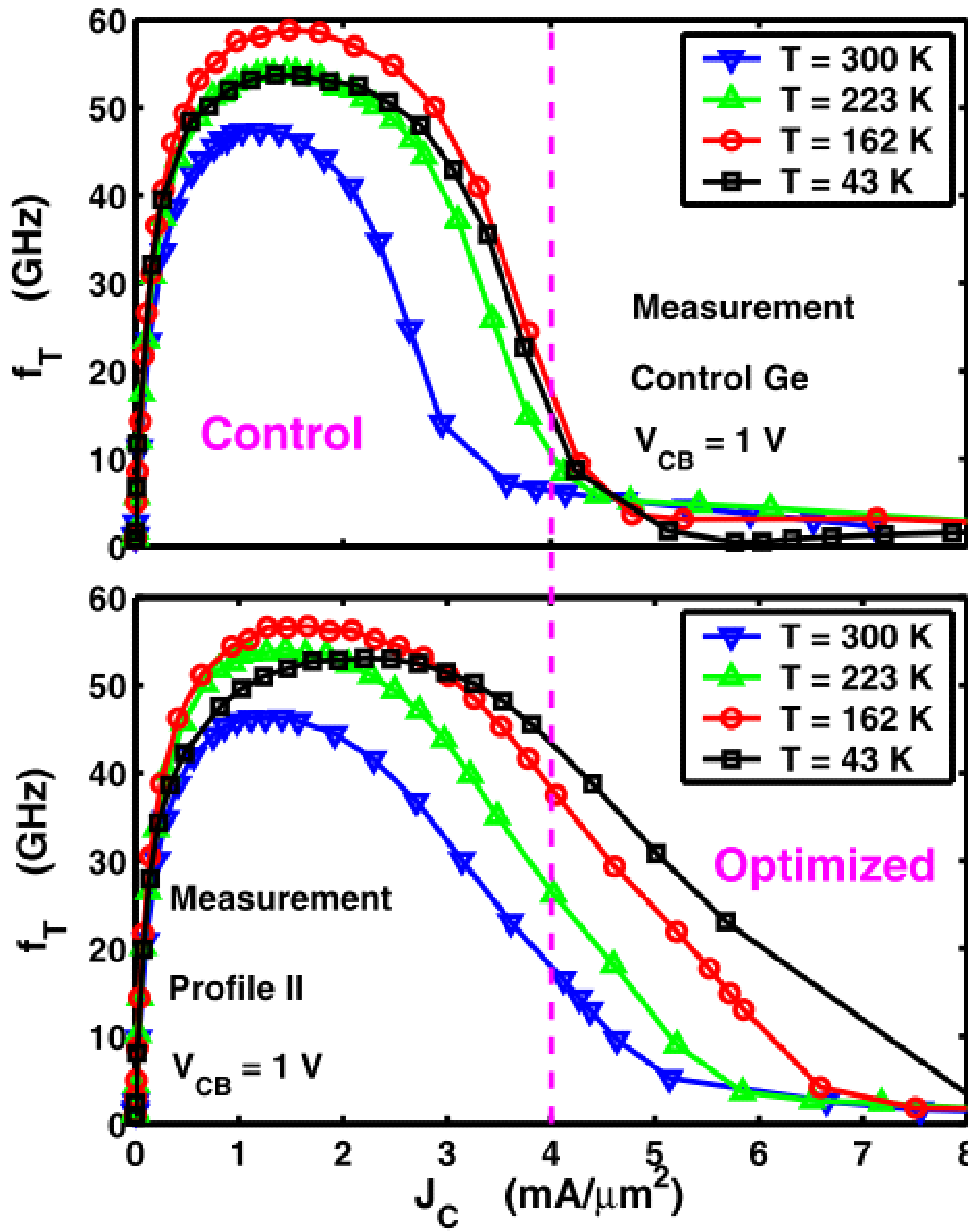
Transit Time Perspective

- Delay “Hump” Forms Near Ge Transition in Control
- Optimized Profile II Effectively Eliminates Hump



Large Ge retrograding can be good to have!

Experimental f_T Results



T = 300 K
T = 223 K
T = 162 K
T = 43 K
Measurement
Control Ge
V_{CB} = 1 V
Control
f_T (GHz)
Measurement
Profile II
V_{CB} = 1 V
Optimized
J_C (mA/μm^2)

Noise

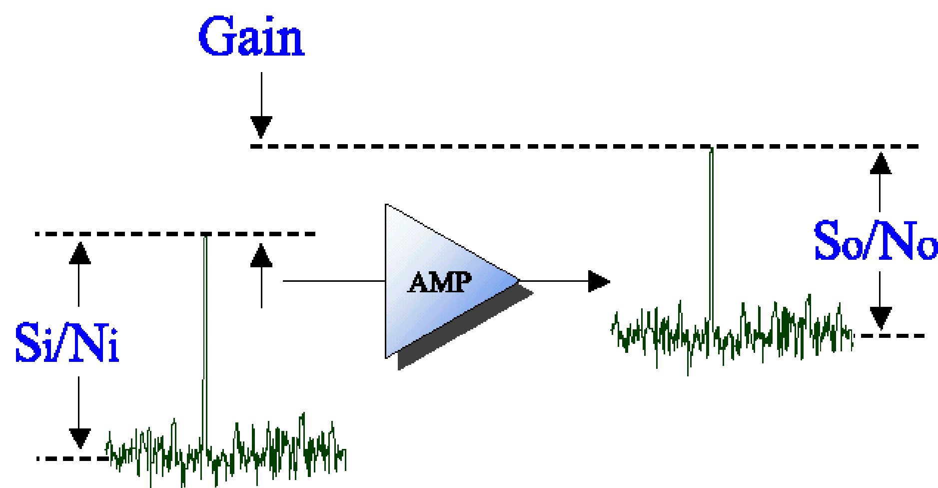
Sunday, April 29, 2012
12:05 AM

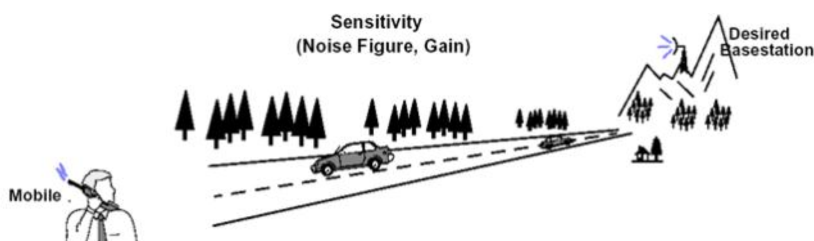
Why we care

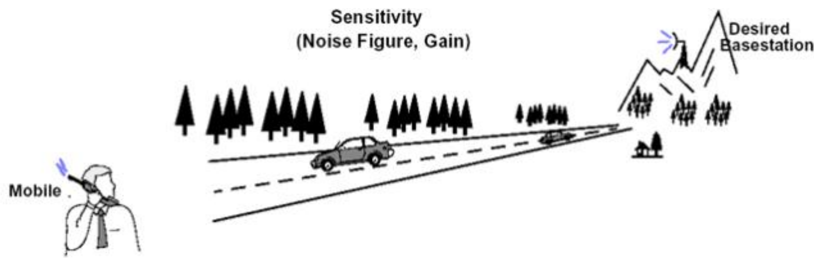
Sunday, April 29, 2012
12:25 PM

Noise Figure and Receiver Sensitivity

- Low Bit Error Rate requires high signal to noise ratio (SNR)
- Noise Figure characterizes SNR = (Si/Ni)/(So/No)
- Noise figure determines the minimum detectable signal
- LNA NF determines sensitivity to a large extent
- 1dB degradation in Noise Figure is a big deal – for cell phones, it means 26% more additional base stations

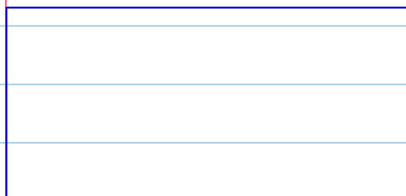






- LNA and mixer noise
  - Noise figure
  - Transistor noise parameters (NFmin, Rn, Yopt)
  - Transistor noise source modeling
- LO phase noise
  - Typically frequency synthesizer output noise
  - Oscillator phase noise is key concern
  - 1/f noise and base/gate resistance upconversions
- IF/baseband amplifier noise
  - All low-frequency noise sources important
  - 1/f particularly important for zero IF or low IF

$$F = \frac{S_{in} / N_{in}}{S_{out} / N_{out}}$$



Noise Factor

Noise Factor

Noise Figure (dB)

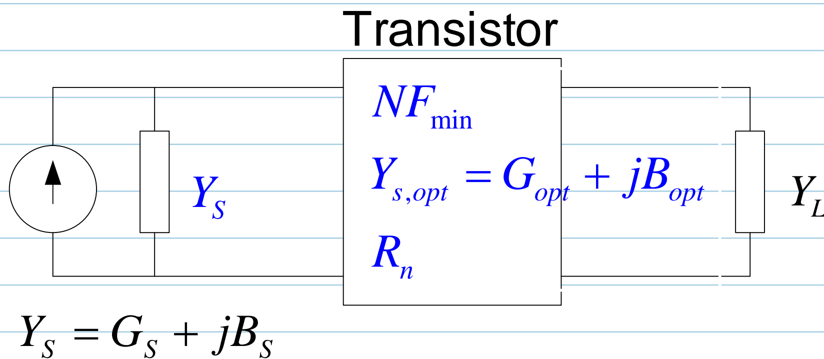
$$NF = 10\log 10(F)$$

$$N_{added} = (F-1)N_{in}$$

High frequency noise

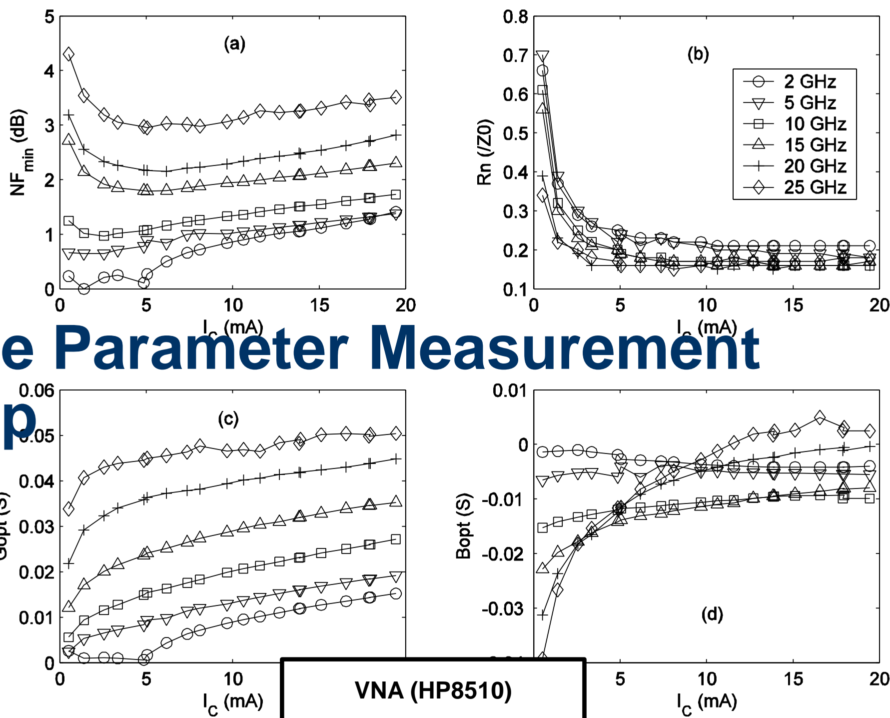
Sunday, April 29, 2012
12:07 AM

Noise parameters

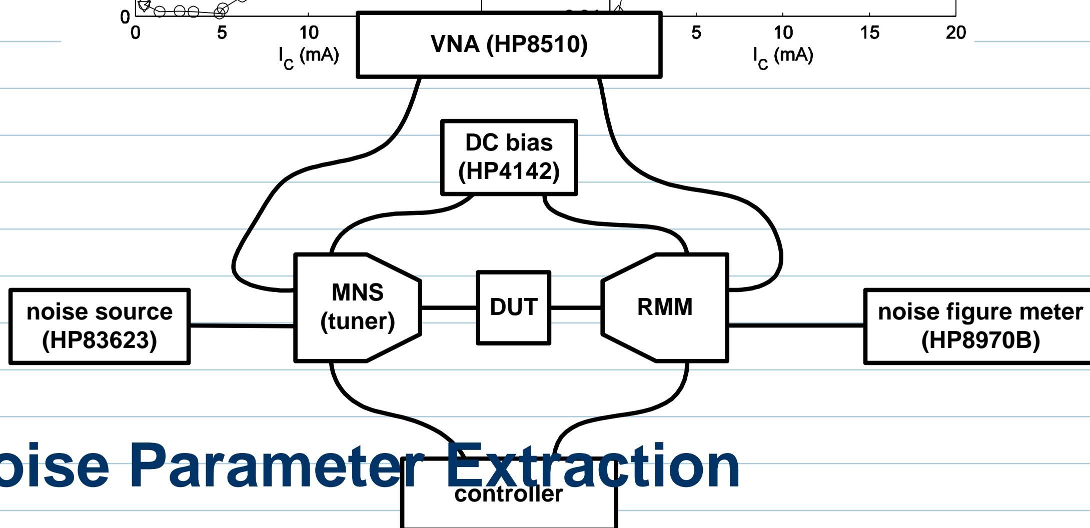


$$NF = NF_{\min} + \frac{R_n}{G_s} \left| Y_s - Y_{s,opt} \right|^2$$

Typical noise parameter current and frequency dependences



Noise Parameter Measurement Setup



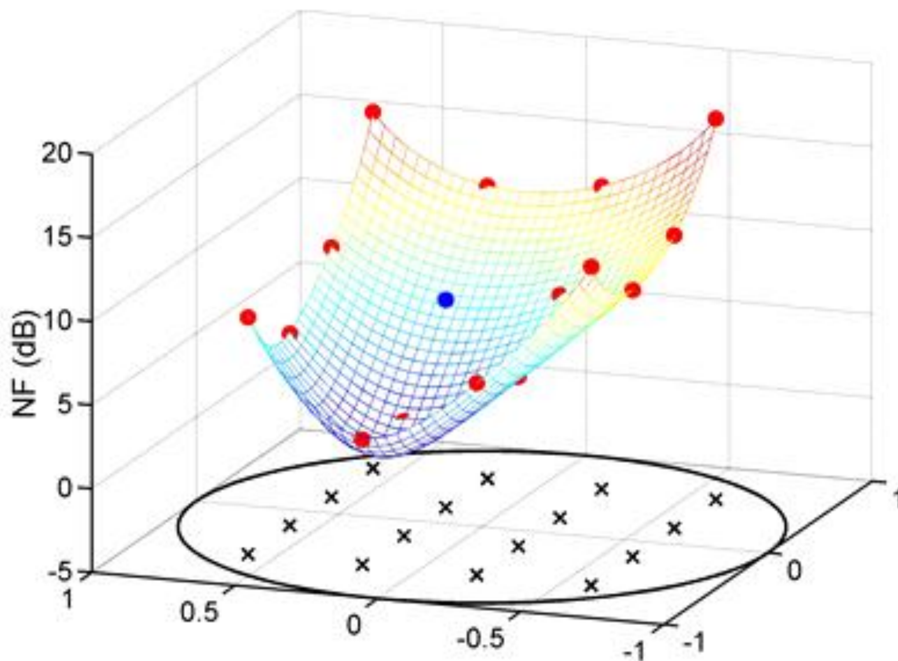
Noise Parameter Extraction

Measure F at multiple states (Ys), then fit F as a function of Ys to determine Fmin, Rn, Gopt and Bopt.

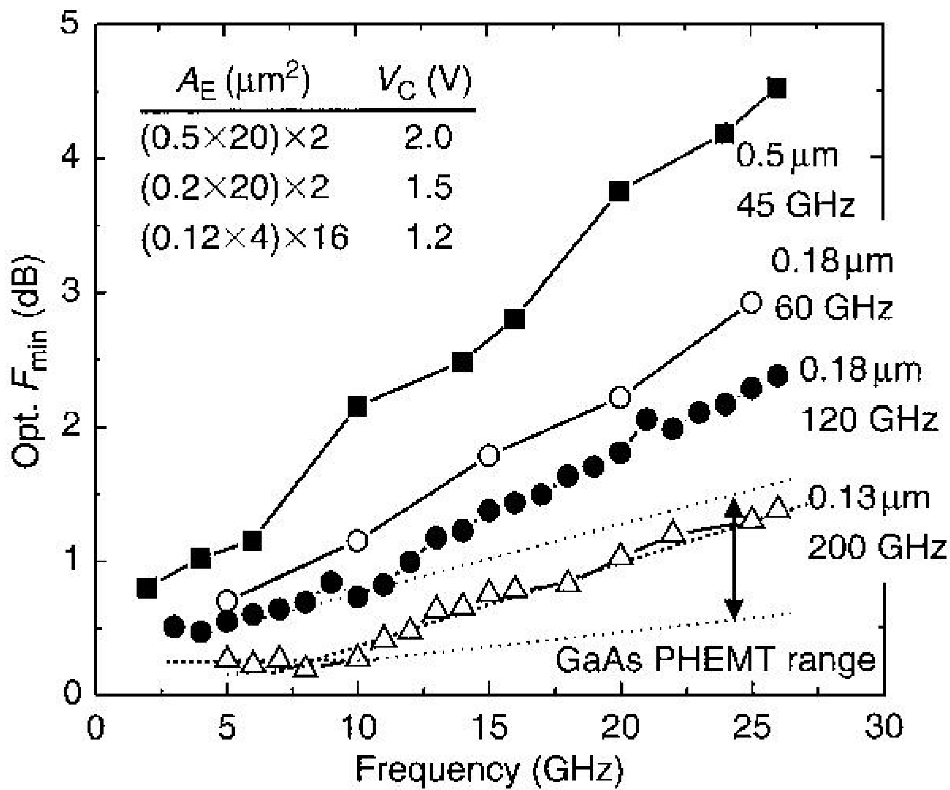
$$F = F_{min} + \frac{R_n}{G_S} \left| Y_S - Y_{opt} \right|^2$$

$$E(A, B, C, D) = \sum_{i=1}^{N} \left\{ B \times \left[(G_{S,i} - C)^2 + (B_{S,i} - D)^2 \right] - (F_i - A) \times G_{S,i} \right\}^2$$

where $A = F_{min}, B = R_n, C = G_{opt} = Real(Y_{opt}), D = B_{opt} = Imag(Y_{opt})$

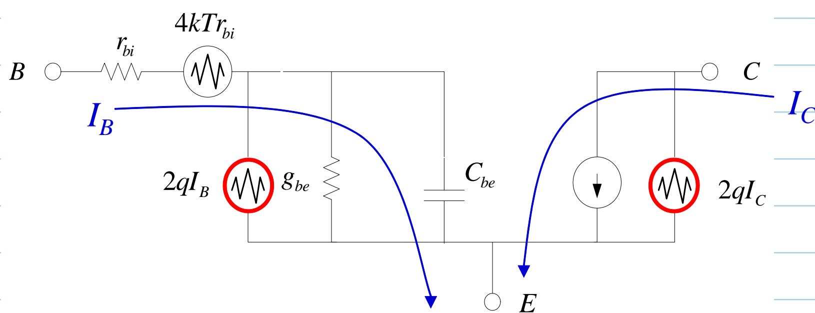


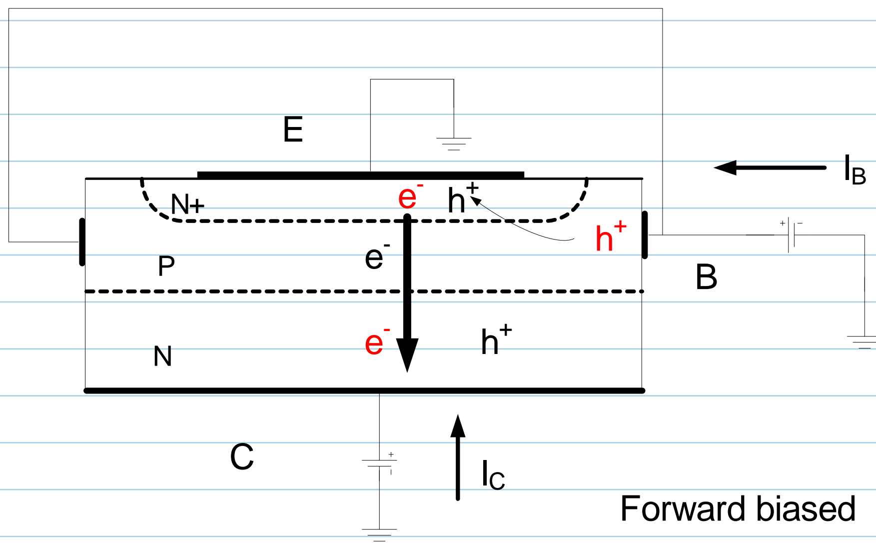
NFmin - technology scaling

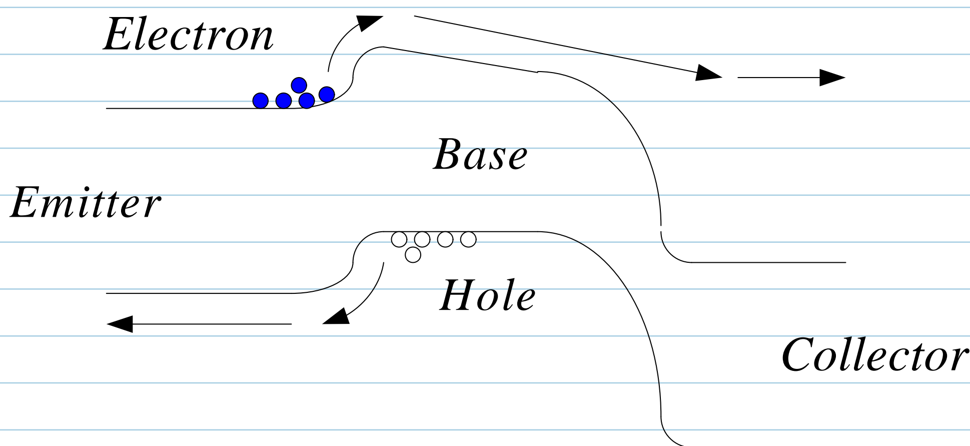


(from Greenberg IBM)

SPICE model of noise source (typical in design kits)







Many new models have been developed in recent years, in my group as well. Below is a summary of a recent compact model

- K. Xia, G. Niu, and Z. Xu, "A New Approach to Implementing High-Frequency Correlated Noise for Bipolar Transistor Compact Modeling", *IEEE-TED, Vol. 59, No. 2, pp. 302-308, 2012.*

Velocity fluctuation origin of "shot" noises

The major noise sources in a bipolar transistor are the base resistance *thermal* noise, or Johnson noise, the base current *shot* noise, and the collector current *shot* noise. The base resistance thermal noise is typically described by a noise voltage with a spectral density of $4kTR$, and the shot noise is described by a spectral density of $2qI$, with I as the DC base current or collector current. These descriptions are based on *macroscopic* views. The standard derivation of the magic $2qI$ shot noise assumes a Poisson stream of an elementary charge q. These charges need to overcome a potential barrier, and thus flow in a completely uncorrelated manner. In a bipolar transistor, the base current shot noise $2qI_B$ results from the flow of base *majority* holes across the EB junction potential barrier. The reason that I_B appears in the base shot noise is that the amount of hole current overcoming the EB barrier is determined by the *minority* hole current in the emitter, I_B. Similarly, the collector current shot noise results from the flow of emitter *majority* electrons over the EB junction potential barrier, and has a spectral density of $2qI_C$.

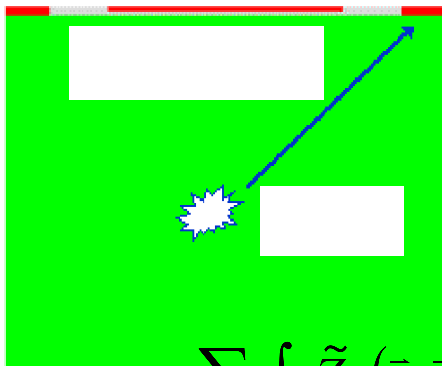
Surprisingly, however, both the $4kTR$ resistor noise and the $2qI$ shot noise can be attributed to the same physical origin at the *microscopic* level — the Brownian motion of electrons and holes, also referred to as *diffusion* noise as the same mechanism is responsible for diffusion. The thermal motion of carriers gives rise to fluctuations of carrier velocities, and hence fluctuations of current densities. The density of such current density fluctuation is $4q^2nD_n$ according to microscopic treatment of carrier motion [1, 2]. The current density fluctuation at each location propagates toward device terminals, giving rise to device terminal voltage or current noise. The problem of noise analysis is now equivalent to solving the transfer functions of noise propagation at each location and summing over the whole device space. These transfer functions can be solved analytically for ideal transistor operation with simplified boundary conditions, or numerically for arbitrary device structures, and the later process is referred to as *microscopic noise simulation.*

$$\delta V\left(r_{Contact}\right)$$

Various mathematical methods have been developed, all based on the impedance field method developed by Schockley and his colleagues [1] and its various generalizations. A very satisfying early application is the successful derivation of the $4kTR$ Johnson noise, a macroscopic model result, from the microscopic $4q^2nD_n$ *noise source density.* The impedance field approach is equivalent to the Green's function based approaches [3], which can be rigorously derived from the general master equation. Efficient numerical algorithms have been developed, which enabled the recent implementation of noise analysis in commercial device simulators, e.g., DESSIS from ISE and Taurus from TMA.

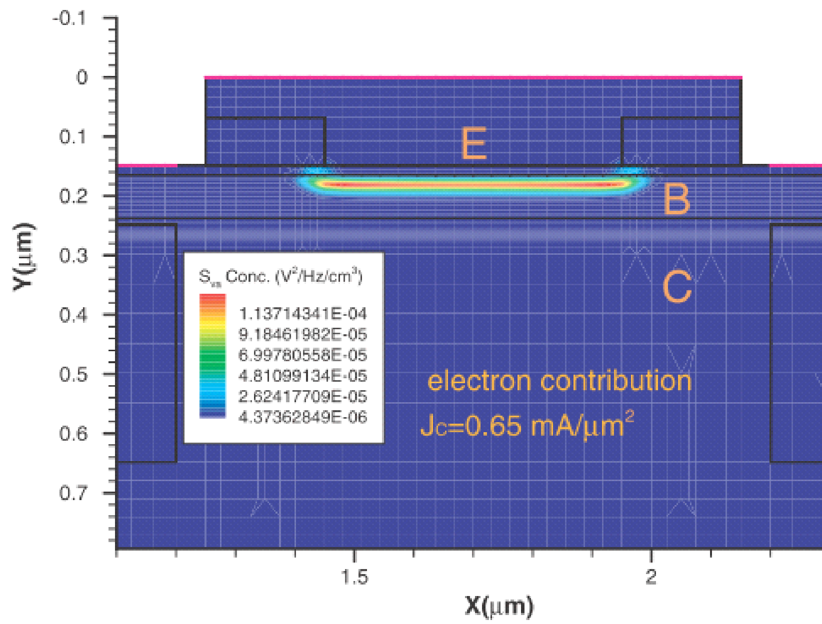
$$Z_{n/p}\left(r, r_{Contact}\right)$$

$$\delta I_{n/p}\left(r\right)$$



$$S_{\delta V(\vec{r}_{Contact})} = \sum_{\alpha=n,p} \int_{\Omega} \tilde{Z}_{\alpha}\left(\vec{r}, \vec{r}_{Contact}\right) \cdot K_{\delta I_{\alpha}} \cdot \tilde{Z}_{\alpha}^{*}\left(\vec{r}, \vec{r}_{Contact}\right) d\Omega$$

$$\tilde{Z}_{n/p}\left(\vec{r}, \vec{r}_{Contact}\right) = \frac{1}{q} \nabla_{\vec{r}} Z_{n/p}\left(\vec{r}, \vec{r}_{Contact}\right),$$



$= n, p$

Figure 4.5: 2D distribution of $C^{e}_{S_{v_a,v_a^*}}$ at 2 GHz, J_C=0.65 mA/μm^2.

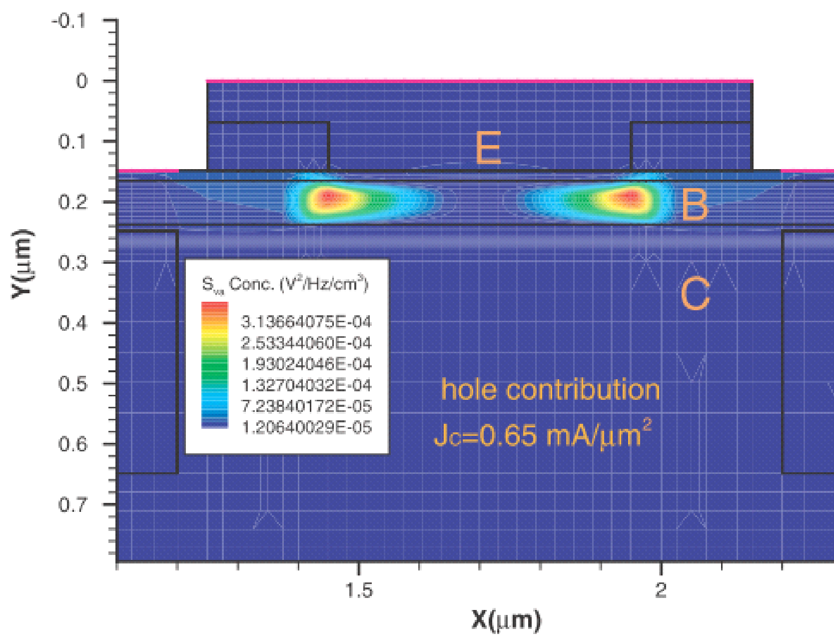
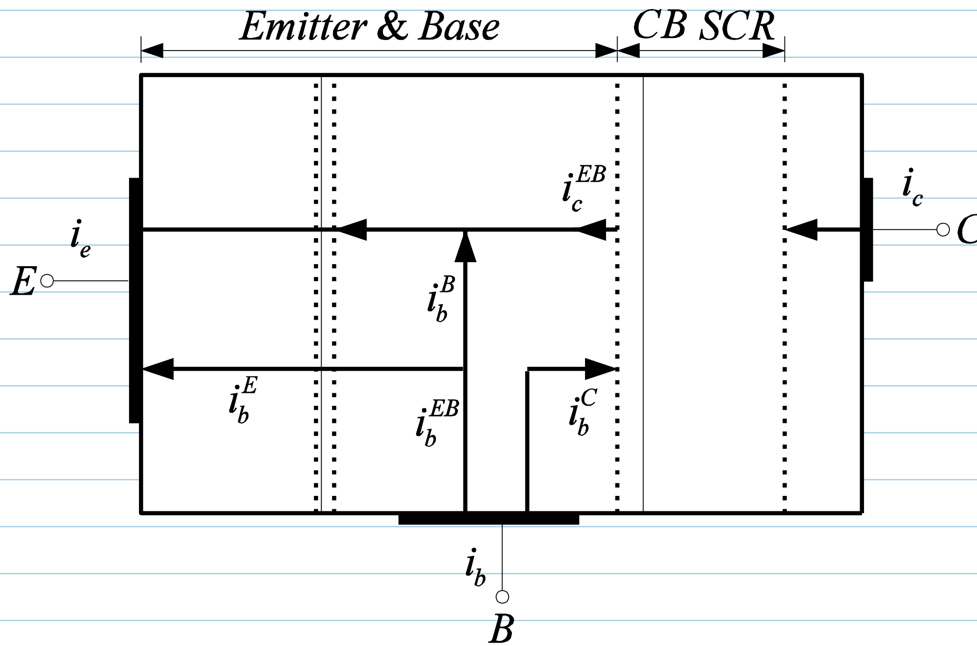


Figure 4.6: 2D distribution of $C^{h}_{S_{v_a,v_a^*}}$ at 2 GHz, J_C=0.65 mA/μm^2.

Essential Physics Important for Modern HBTs - CB SCR effect

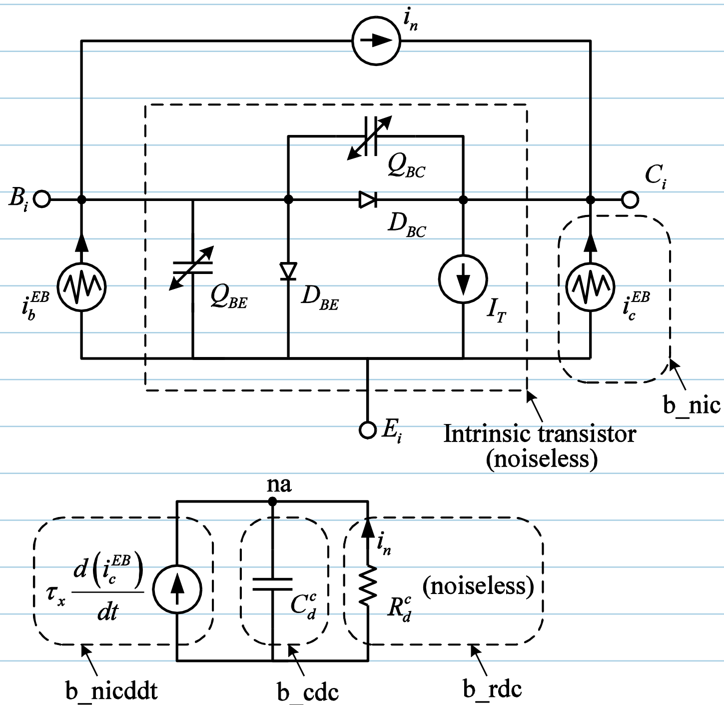
1. Minority carrier velocity fluctuations in the emitter and base will **propagate throughout the device**, causing current fluctuation in every location in the transistor
2. At the entrance of CB SCR, we see electron current noise $i_c^{\{E,B\}}$ - this corresponds to the so-called $2qI_C$ shot noise at low frequency
3. This **noisy electron** current will make its way through CB SCR just like a regular transport current - and hence produce **additional noisy hole current** at the base terminal i_b^C.
4. While current standard practice is to not consider the CB SCR transport induced noise, **CB SCR effect induced noise is actually most important for modern SiGe HBTs** at RF
5. In some compact models, e.g. Mextram, the extended noise model intended for emitter and base noise can actually model CB SCR effect unintentionally to some degree. Again, your typical design kit does not have such "advanced" feature.



$$S_{\rm ib} = S_{\rm ib}^{\rm EB} + 2\Re\left[(1-\lambda)S_{\rm icib*}^{\rm EB}\right] + |1-\lambda|^2 S_{\rm ic}^{\rm EB}$$
$$S_{\rm ic} = |\lambda|^2 S_{\rm ic}^{\rm EB}$$
$$S_{\rm icib*} = \lambda S_{\rm icib*}^{\rm EB} + \lambda(1-\lambda^*) S_{\rm ic}^{\rm EB}.$$

$$\lambda = \frac{1 - e^{-2j\omega\tau_c}}{2j\omega\tau_c}$$

A new implementation compatible with nonlinear circuit simulators



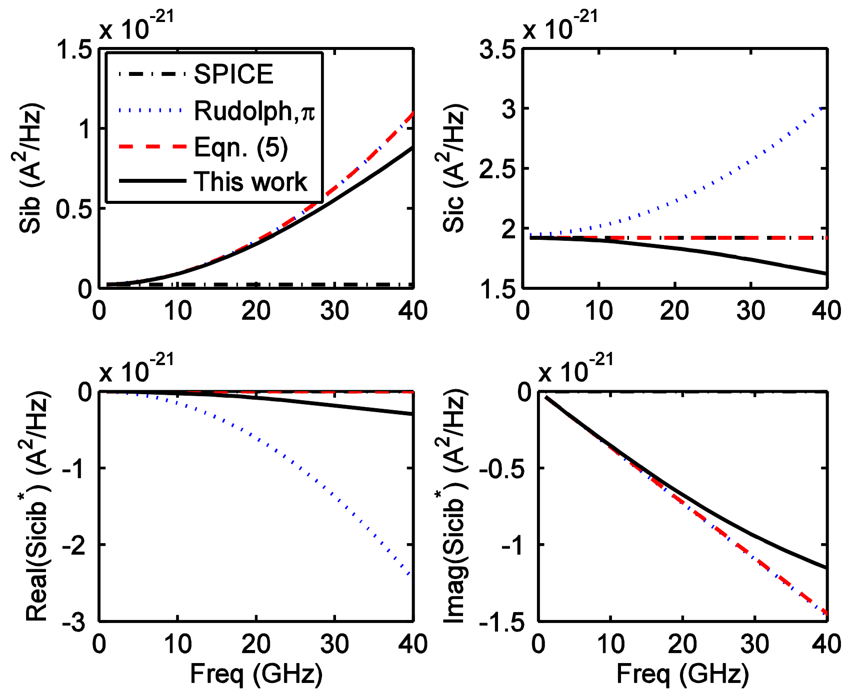
The unique feature is the “in” placed between base and collector, which reproduces lambda.

1. Produces two stage noise transport.
2. Non-white Sic
3. Non-zero Re(Sicib*)

Verilog-a code

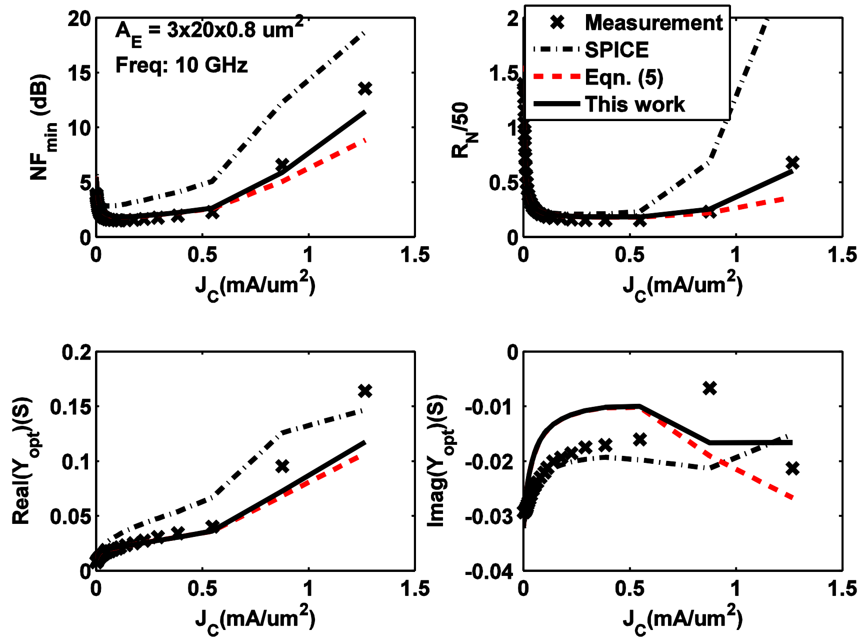
```
electrical na;
branch (na) b_nicddt, b_cdc, b_rdc;
branch (ci, ei) b_nic;
rdc = 2/3;
cdc = taun;
twoq = 2.0 * ‘P_Q;
```

```
sic = twoq * abs(it);
sib = twoq * abs(ibei);
I(b_nic) <+white_noise(sic, “shot”);
I(bi, ei) <+white_noise(sib, “shot”);
I(b_nicddt) <+taun * ddt(I(b_nic));
I(b_cdc) <+cdc * ddt(V(b_cdc));
I(b_rdc) <+V(b_rdc)/rdc;
I(ci, bi) <+I(b_rdc);
```



Implementation Result in HICUM model

(Power SiGe HBT with 36 GHz peak fT)



Low-frequency noise

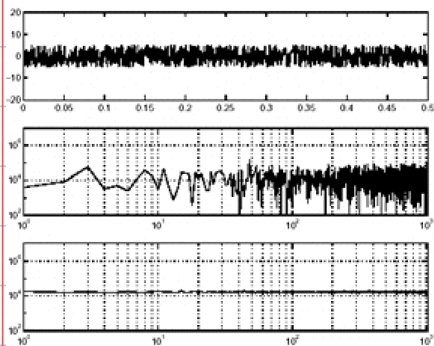
Sunday, April 29, 2012

12:30 AM

What is white and 1/f Noise Like?

White noise

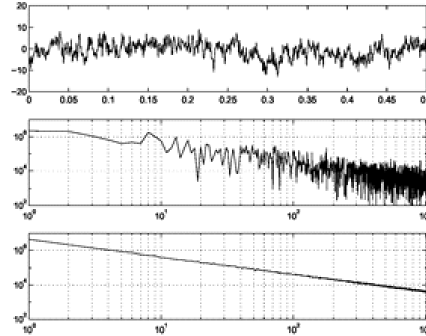
1/f noise



Time domain

Spectrum from single time sequence

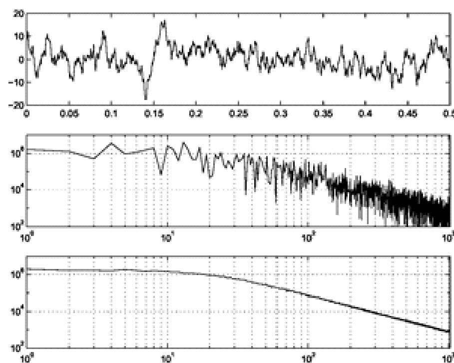
Spectrum from 300 averages



S. Bruce, thesis, 1999

Lorentzian

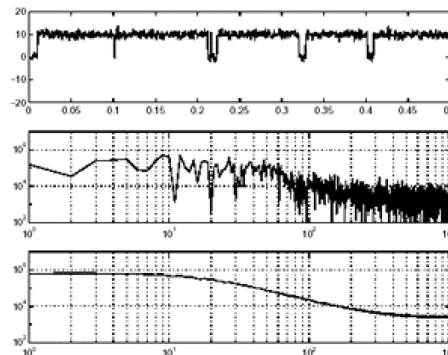
RTS



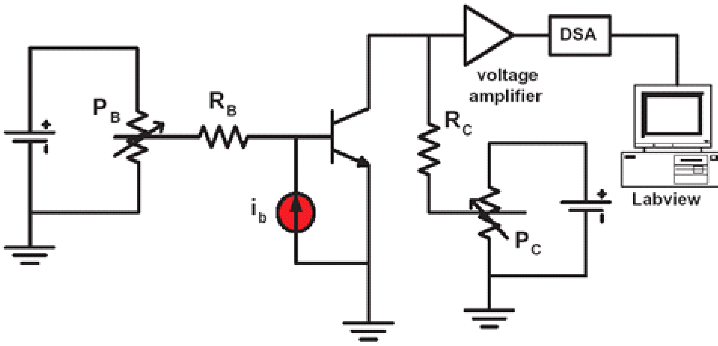
Time domain

Spectrum from single time sequence

Spectrum from 300 averages



1/f noise measurement



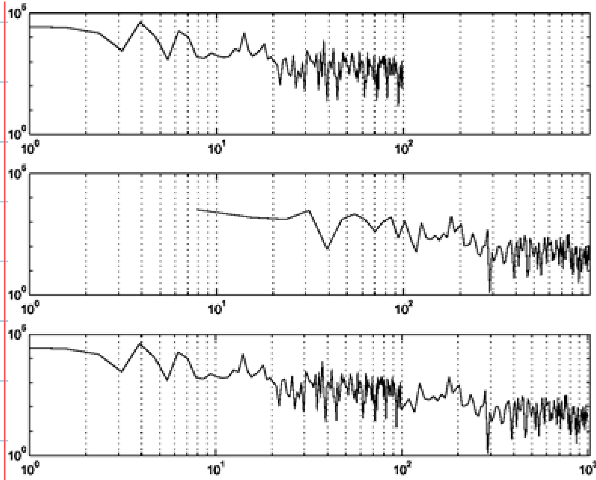
Dynamic Range and Bandwidth of Instrument

- Time domain sampling, A/D, FFT -> PSD spectrum
- Dynamic range – the PSD contains a wide range of signals,
  - we need to resolve the lowest signal in presence of the strongest input,
  - power line and its harmonics can create strong interference
  - Roughly A/D converter dynamic range is 6dB/bit
- Bandwidth
  - Sampler in DSA should be in AC mode

- Typical claims of analyzers are made assuming DC mode

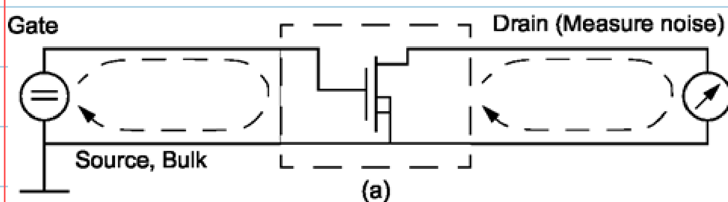
Averaging is Important! But …

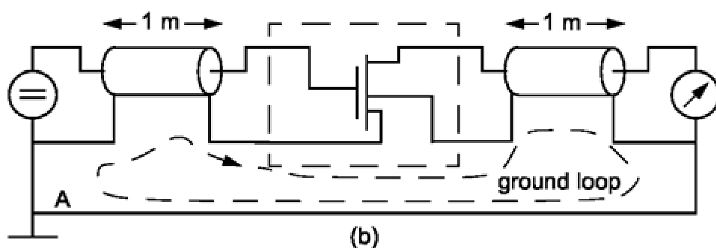
- Averaging is made of non-overlapping multiple time sequences – assuming stationary noise
- Averaging should not be confused with sampling longer time sequence – which only allows lower frequency
- Choose the right number of averages – particularly important when measuring coherence (e.g. correlation of two signals)
- Averaging improves spectrum, but interpreting data at lowest frequency requires care
- FFT assumes repeating the sampled data infinitely in time – PSD values at lowest frequency correspond to very few samples!
- The amount of samples should be chosen so that the first few frequency points can be discarded!
- Measurement of spectrum over several decades is often desired (e.g. from 1Hz to 100 kHz)
- Measurement should be made decade by decade (instead of over the whole band), sub-band spectra are then pieced together



Grounding / Ground Loop Antenna

- Proper grounding, short cable, Substrate/body/ground need to be well planned to avoid picking up signals in the ground loop (antenna)
- Use short cable



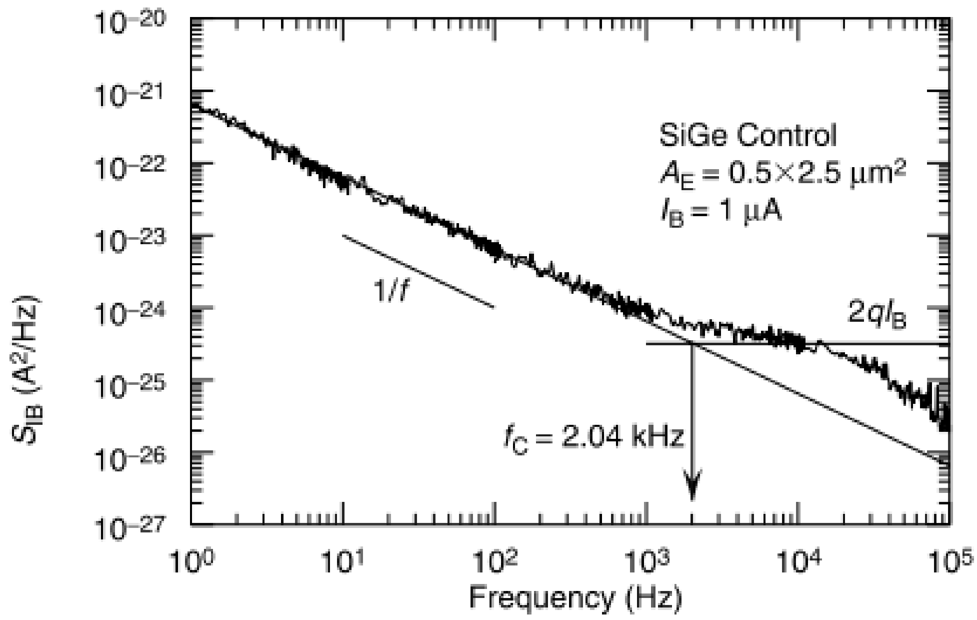


Blaum et al., Agilent/Motorola/ICMTS2001

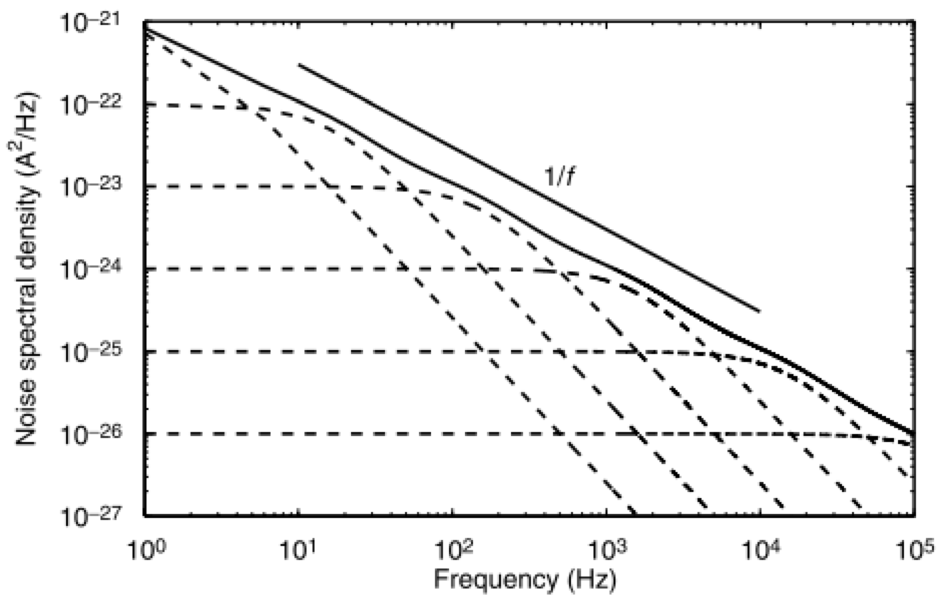
Probe Station / Oscillation / Shielding

- Dc auto prober works ok with proper good shielding
- RF probe station with good shielding will certainly help – enables testing on RF test structures
- New cascade probe stations offer improved shielding –
  - a plus to have
  - Less oscillation problem to deal with
  - When RF probes are used, ground loop antenna effect and oscillation is less likely
- **Oscillation is more likely with higher speed HBTs/CMOS on dc prober**
  - Long, unshielded probes create too much output-input coupling
  - Use Auto prober, best to use RF prober
- For MOSFET, using RF probe prevents you from investigating body effect (requires body biasing)

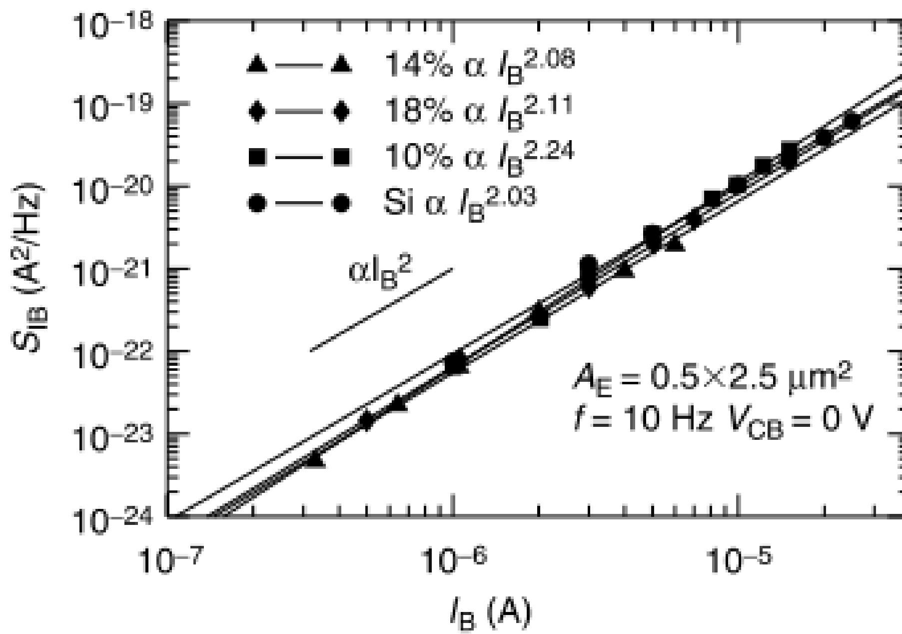
HBT 1/f Noise Data and Current /Size Dependences



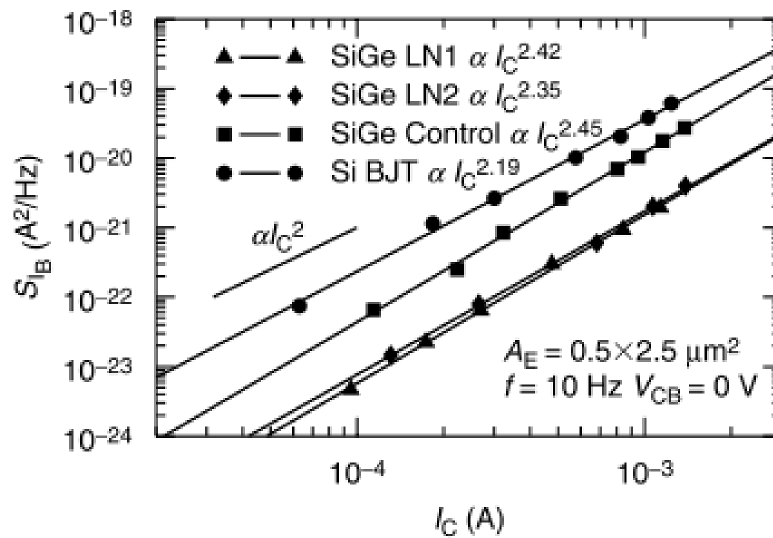
$$f_C = \frac{KI_B}{2qA_E} = \frac{KJ_C}{2q\beta},$$



1/*f* noise as a superposition of Lorentzians.



ed S_{I_B} at 10 Hz as a function of I_B for the Si BJT, the SiGe control, and

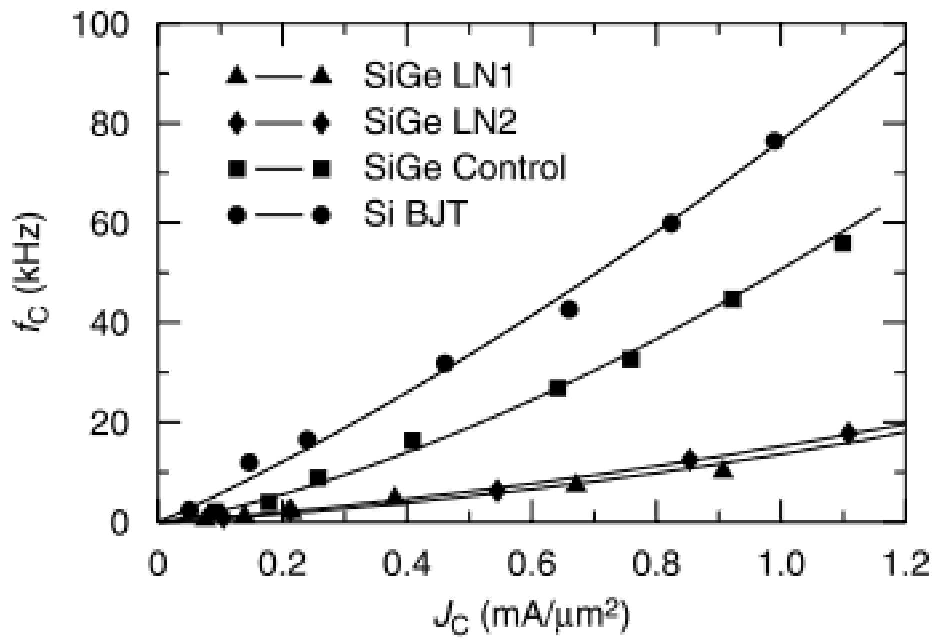


Measured S_{I_B} at 10 Hz as a function of I_C for the Si BJT, the SiGe control, and the two low-nois

$$S_{I_B} = \frac{K}{A_E}\frac{I_B^2}{f} = \frac{K}{\beta^2}\frac{1}{A_E}\frac{I_C^2}{f},$$

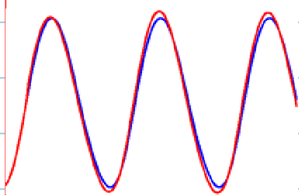
SiGe Profile Dependence (high

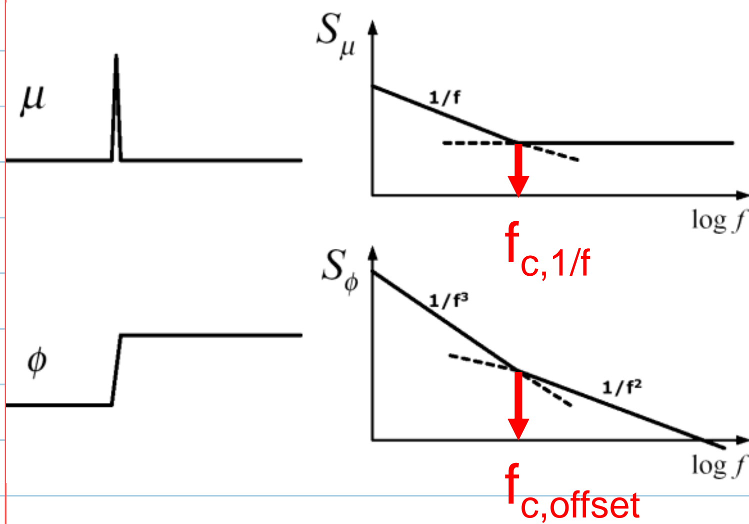
beta naturally reduces corner)



Upconversion to Oscillator Phase Noise

- A pertubation u shifts phase ϕ and magnitude of oscillation
- Amplitude shift will die out, phase shift remains (step like)
- Any time shifted solution remains a solution to oscillators
- Phase shift accumulates





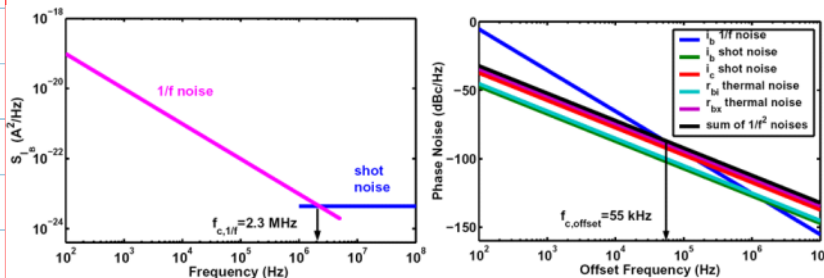
$$\phi(t) \propto \int_{-\infty}^{t} u(\tau)s(t-\tau)d\tau \propto \int_{-\infty}^{t} u(\tau)d\tau$$

1/f Noise Corner ≠ Phase Noise Corner!

Laplace Transform leads to

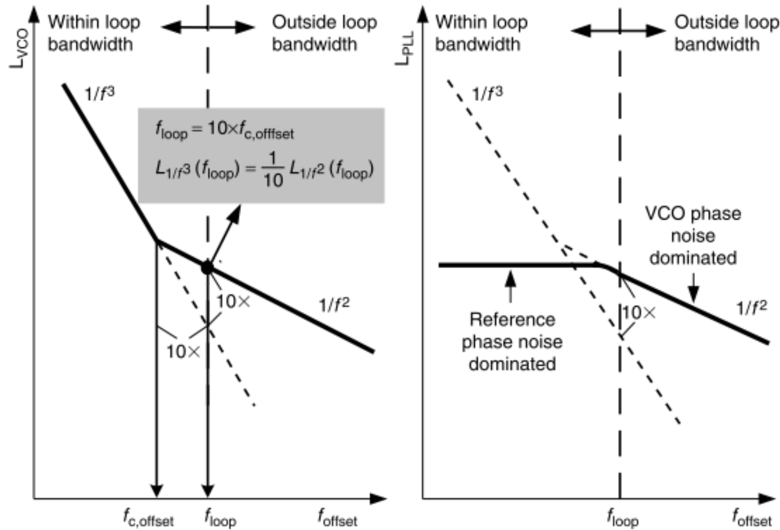
$$S_\phi \propto \frac{S_u}{(2\pi f)^2}$$ If S_u is white, $S_\phi \propto 1/f^2$, if S_u is 1/f, $S_\phi \propto 1/f^3$

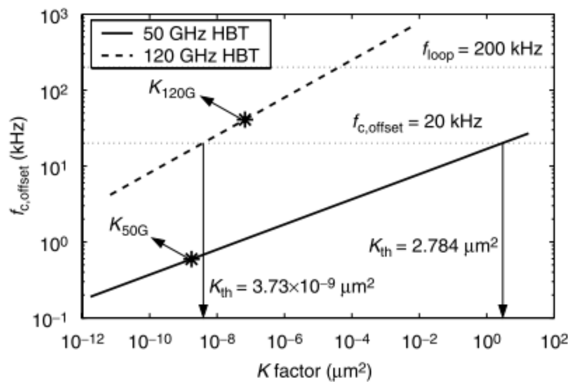
- 1/f noise corner does not indicate phase noise corner
- For typical bipolar, phase noise corner is much lower!!
- The relative importance of 1/f with respect to white noises for phase noise is significantly overestimated by the1/f corner measured under dc bias!!!



Synthesizer Phase Noise

Requirement on 1/f Noise K factor





One can determine the level of "1/f noise" K factor for a given synthesizer design target.

homework

Saturday, August 11, 2012
2:35 PM

1. Based on the information you have, think about areas of interest to you most.

2. Install EDP python (free).

http://www.enthought.com/products/edudownload.php
use your tigermail to request download.

3. Install VPN client from AU install.

4. Install VNC viewer on your pc (realvnc.com has free version) - most of you should already have this. Log on to niu003.eng.auburn.edu using putty.exe (if you use windows) or other ssh program. Start a vnc server process, then log in to niu003 using your pc vnc server.
5. Bring your computer to next class.

Notes access

Thursday, August 16, 2012
12:37 PM

Online onenote