

ELEC 2210 - EXPERIMENT 1

Basic Digital Logic Circuits

The objectives of this experiment:

The experiments in this laboratory exercise will provide an introduction to digital electronic circuits. You will learn how to use the National Instruments myDAQ to build and test circuits using common logic gates. The objectives of this experiment include:



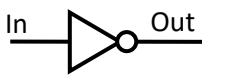
- Review basic principles of digital logic from ELEC 2200
- Learn how to use NI myDAQ
- Develop professional lab skills and written communication skills

I. Introduction





Almost all computers today use binary digital logic circuits. These circuits have just two possible output voltages, which can be called by any contrasting terms; the most common are “HIGH/LOW”, or “TRUE/FALSE”, or “ONE/ZERO.” Such an output is called a “binary digit,” or *bit*. The decimal numbers and alphabet characters we are familiar with are converted to binary bits before they are fed into a computer’s arithmetic logic unit (ALU). Inside the ALU, the computer executes a program and generates binary results. The binary results are converted back to decimal numbers, alphabet letters, graphics, or sound so we can understand them. Most of the fundamental data processing inside computers is done using *logic gates*. Logic gates combine individual bits according to certain rules. These rules, taken together, form the basis of *Boolean algebra*, which you studied in depth in ELEC 2200 Digital Logic Circuits.

Logic Gates

We will introduce the most common logic gates in this section, including the AND, OR, XOR, NOT, NOR, and NAND. For each gate, we will show the circuit symbol, the Boolean algebra logic function, and the truth table. The truth table lists all possible combinations of inputs, and the resulting output for each. The three most common gates are the AND, OR and NOT (inverter) gates from which any digital logic circuit can be constructed. These gates are summarized below in terms of their logic symbol, logic equation, and truth table. It should be noted that the NOT gate has only one input while the AND and OR gates can have two or more inputs.

Logic Gate	AND	OR	NOT (inverter)																																				
Symbol																																							
Logic Equation	$Out = In1 \bullet In2$	$Out = In1 + In2$	$Out = \overline{In}$																																				
Truth Table	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td style="padding: 2px;">In1</td><td style="padding: 2px;">In2</td><td style="padding: 2px;">Out</td></tr> <tr><td style="padding: 2px;">0</td><td style="padding: 2px;">0</td><td style="padding: 2px;">0</td></tr> <tr><td style="padding: 2px;">0</td><td style="padding: 2px;">1</td><td style="padding: 2px;">0</td></tr> <tr><td style="padding: 2px;">1</td><td style="padding: 2px;">0</td><td style="padding: 2px;">0</td></tr> <tr><td style="padding: 2px;">1</td><td style="padding: 2px;">1</td><td style="padding: 2px;">1</td></tr> </table>	In1	In2	Out	0	0	0	0	1	0	1	0	0	1	1	1	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td style="padding: 2px;">In1</td><td style="padding: 2px;">In2</td><td style="padding: 2px;">Out</td></tr> <tr><td style="padding: 2px;">0</td><td style="padding: 2px;">0</td><td style="padding: 2px;">0</td></tr> <tr><td style="padding: 2px;">0</td><td style="padding: 2px;">1</td><td style="padding: 2px;">1</td></tr> <tr><td style="padding: 2px;">1</td><td style="padding: 2px;">0</td><td style="padding: 2px;">1</td></tr> <tr><td style="padding: 2px;">1</td><td style="padding: 2px;">1</td><td style="padding: 2px;">1</td></tr> </table>	In1	In2	Out	0	0	0	0	1	1	1	0	1	1	1	1	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr><td style="padding: 2px;">In</td><td style="padding: 2px;">Out</td></tr> <tr><td style="padding: 2px;">0</td><td style="padding: 2px;">1</td></tr> <tr><td style="padding: 2px;">1</td><td style="padding: 2px;">0</td></tr> </table>	In	Out	0	1	1	0
In1	In2	Out																																					
0	0	0																																					
0	1	0																																					
1	0	0																																					
1	1	1																																					
In1	In2	Out																																					
0	0	0																																					
0	1	1																																					
1	0	1																																					
1	1	1																																					
In	Out																																						
0	1																																						
1	0																																						

Other common gates include the NAND, NOR, exclusive-OR (XOR), and exclusive-NOR (XNOR) gates. While the NAND and NOR gates are functionally complete (meaning that any digital logic circuit can be constructed from either one of these gates), the XOR and XNOR gates are not functionally complete and, therefore, are not considered to an elementary logic gate by most designers. These gates are summarized below in terms of their logic symbol, logic equation, and truth table where it should be noted that the NAND and NOR gates (like their AND and OR counterparts) can have two or more inputs, while the XOR and XNOR gates generally have only two inputs. The NAND and NOR gates are a combination of an AND gate and NOT gate and a combination of an OR gate and NOT gate, respectively, as can be observed by comparing their truth tables. Similarly, the exclusive-NOR (XNOR) gate has the inverse output of the XOR gate truth table.

Logic Gate	NAND	NOR	XOR	XNOR																																																												
Symbol																																																																
Logic Equation	$Out = \overline{In1 \cdot In2}$	$Out = \overline{In1 + In2}$	$Out = In1 \oplus In2$	$Out = \overline{(In1 \oplus In2)}$																																																												
Truth Table	<table border="1"><thead><tr><th>In1</th><th>In2</th><th>Out</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table>	In1	In2	Out	0	0	1	0	1	1	1	0	1	1	1	0	<table border="1"><thead><tr><th>In1</th><th>In2</th><th>Out</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table>	In1	In2	Out	0	0	1	0	1	0	1	0	0	1	1	0	<table border="1"><thead><tr><th>In1</th><th>In2</th><th>Out</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table>	In1	In2	Out	0	0	0	0	1	1	1	0	1	1	1	0	<table border="1"><thead><tr><th>In1</th><th>In2</th><th>Out</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table>	In1	In2	Out	0	0	1	0	1	0	1	0	0	1	1	1
	In1	In2	Out																																																													
	0	0	1																																																													
	0	1	1																																																													
	1	0	1																																																													
1	1	0																																																														
In1	In2	Out																																																														
0	0	1																																																														
0	1	0																																																														
1	0	0																																																														
1	1	0																																																														
In1	In2	Out																																																														
0	0	0																																																														
0	1	1																																																														
1	0	1																																																														
1	1	0																																																														
In1	In2	Out																																																														
0	0	1																																																														
0	1	0																																																														
1	0	0																																																														
1	1	1																																																														

DeMorgan's Theorems also relate the operation of the NAND and NOR gates to AND and OR gates as follows:

$$\overline{(A \cdot B)} = \overline{A} + \overline{B}$$

$$\overline{(A + B)} = \overline{A} \cdot \overline{B}$$

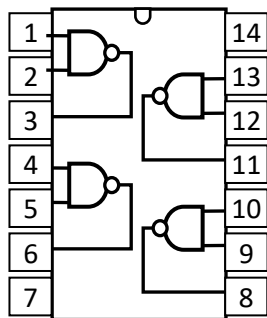
DeMorgan's Theorems in conjunction with the Involution Theorem, which states that $\overline{(\overline{A})} = A$, can be used to convert any 2-level AND-OR implementation of a sum-of-products (SOP) expression to an all-NAND gate implementation of the circuit. Similarly, any 2-level implementation of a product-of-sums (POS) expression can be converted to an all-NOR gate implementation of the circuit.

Logic Families

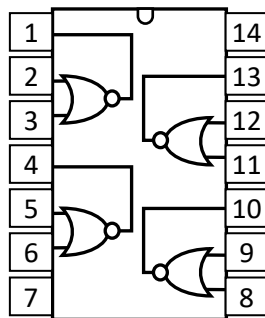
A logic family is a complete set of logic gates that are manufactured using a particular type of electronic circuitry. There are numerous commercially available logic families to suit different design requirements. The most common logic families are listed in the table below, together with their relative advantages and disadvantages.

Acronym	Full name	Advantages	Disadvantages
CMOS	Complementary metal-oxide semiconductor	Lowest power consumption. Most common logic family- used in all microcomputer chips today.	Easily damaged by static discharge and voltage spikes.
TTL	Transistor-transistor logic	Earliest developed. Most rugged – least susceptible to electrical damage.	Consumes more power than CMOS – not suitable for battery operated devices.
ECL	Emitter-coupled logic	Fastest available logic family	Consumes more power than CMOS. Requires extreme care in wiring.

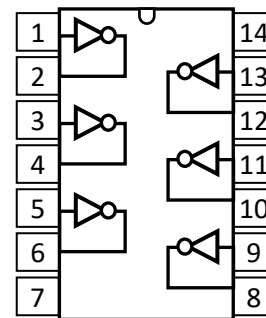
The standard part number for the TTL NAND gate is 7400. However, most manufacturers have their own designation which includes these numbers, but adds some extra characters. The following are examples of valid part numbers you might find on a "7400" chip: SN7400N, MM74C00N, SN74LS00N, SN74H00N, etc. In addition to these, there will often be another part code stamped on the chip by the manufacturer, and there might be a code stamped underneath the chip as well. In general, as long as you can find the digits 7400 somewhere on the chip, you have the right one. Below is a top view of a 7400, which is a quad NAND gate integrated circuit (IC). The term “quad” means there are four separate NAND gates on a single chip (they all share the same power supply, but their inputs and outputs are independent). Note the pin numbering. The chip has an indentation at one end to distinguish the ends (shown in the middle of the top of the package in the figure below). For this chip to operate, you must connect 5V to pin 14 (VCC), and ground to pin 7 (GND). Some standard TTL ICs for basic digital logic functions are illustrated below at the package level for dual-inline packages (DIPs). The pin numbers are shown along with the internal connections to the gates. **Note that in all three cases Pin14 = Vcc and Pin7 = Gnd for all three of these devices.**



7400 Quad 2-input NAND gates



7402 Quad 2-input NOR gates



7406 Hex Inverters

TTL Logic

In this experiment, we will be using TTL logic. All ICs in the TTL logic family have the following specifications:

POWER SUPPLIES: +5 V and Ground (0 V).

LOGIC HIGH: 2.0 to 5 V

LOGIC LOW: 0 to 0.8 V

FAN-OUT (Number of inputs that each output can be connected to): 10

More details can be found in most textbooks on digital electronics, and also on the Internet. Here is a useful website for TTL information: http://en.wikipedia.org/wiki/Transistor-transistor_logic

II. NI myDAQ

The experiments in this lab course will be performed on NI myDAQ, pictured in Figure 1, which is a low-cost portable data acquisition (DAQ) device for experimentation with linear, electronic, and digital logic circuits. NI myDAQ uses NI LabVIEW-based software instruments to enable measurement and analysis of real-world signals. Later in the course, we will also use custom LabVIEW apps written by Dr. Niu to perform various transistor circuit measurements. For digital logic experiments, NI myDAQ provides regulated 5 V power, and 8 digital signals that can be controlled and/or monitored from a graphical user interface on a PC. NI myDAQ also includes the hardware elements of a variety of electrical test instruments, such as oscilloscope, waveform generator, etc., with graphical user interfaces for the instruments on a PC connected to the workstation with a USB cable.

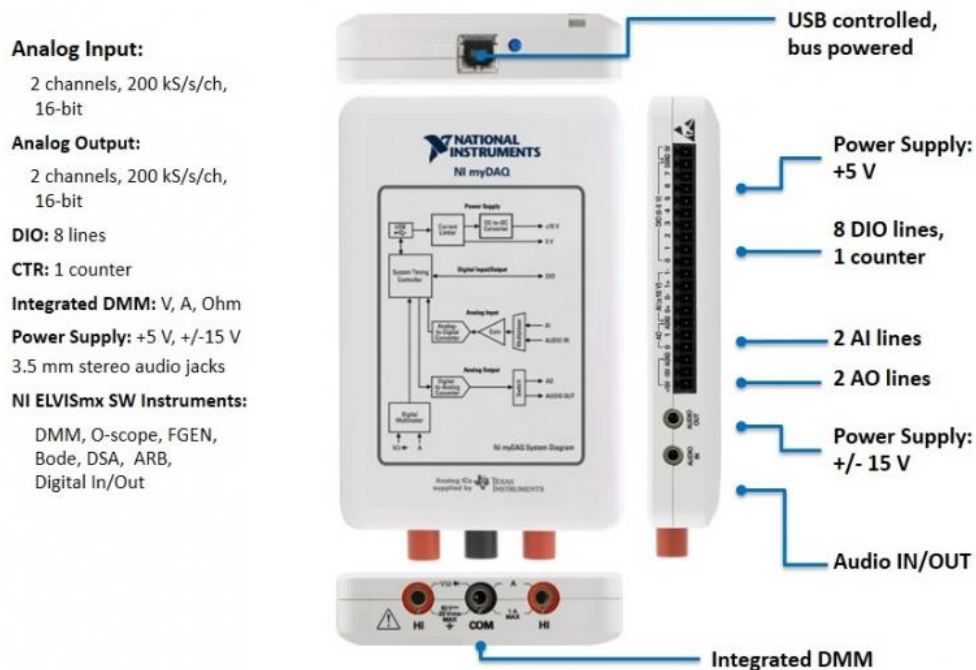


Figure 1. NI myDAQ.

Inputs and Outputs

For studying digital logic circuits we will use several types of inputs and outputs, including switches, clock signals, LED's, and the myDAQ Digital Writer and Digital Reader.

myProto Protoboard

The Digilent myProto accessory board for the NI myDAQ, shown in Figure 2, brings all the NI myDAQ's signals to breadboard connections where they can be easily accessed using simple

ELEC 2210 Experiment 1 (Rev. 05/18/2020)

jumper wires, and even adds several useful I/O devices. The MSP connector on myDAQ provides power (+5 VDC and ± 15 VDC) along with eight configurable digital I/O pins, two analog inputs (AI0 and AI1), and two analog outputs (AO0 and AO1). All these signals are available and clearly labeled on the signal blocks at the top of the breadboard when plugged into the MSP connector.

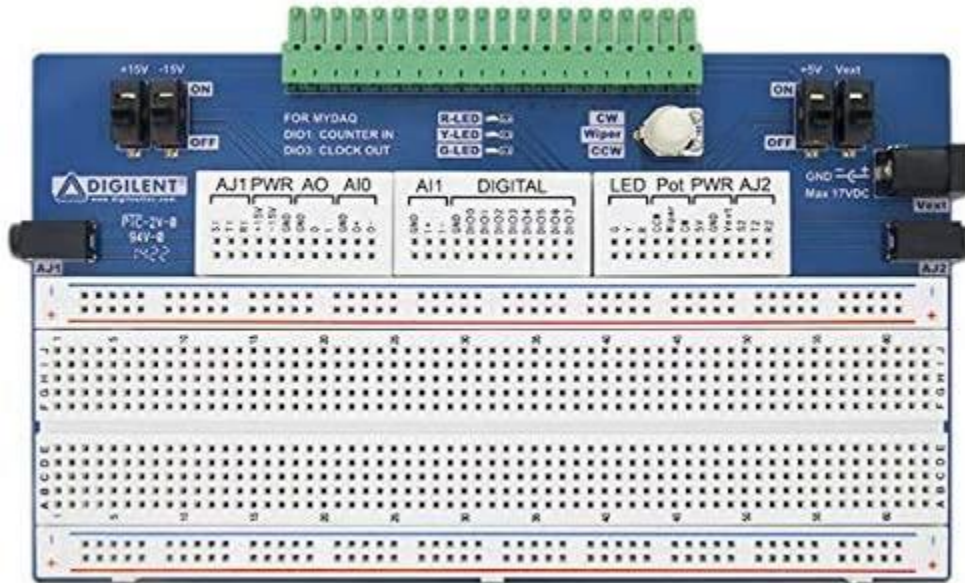


Figure 2. myProto protoboard.

Connect myDAQ to myProto board

Before we start, we need to connect myDAQ to myProto board. The terminal connectors of myProto board should be inserted into the MSP connectors of myDAQ, as shown in Figure 3.

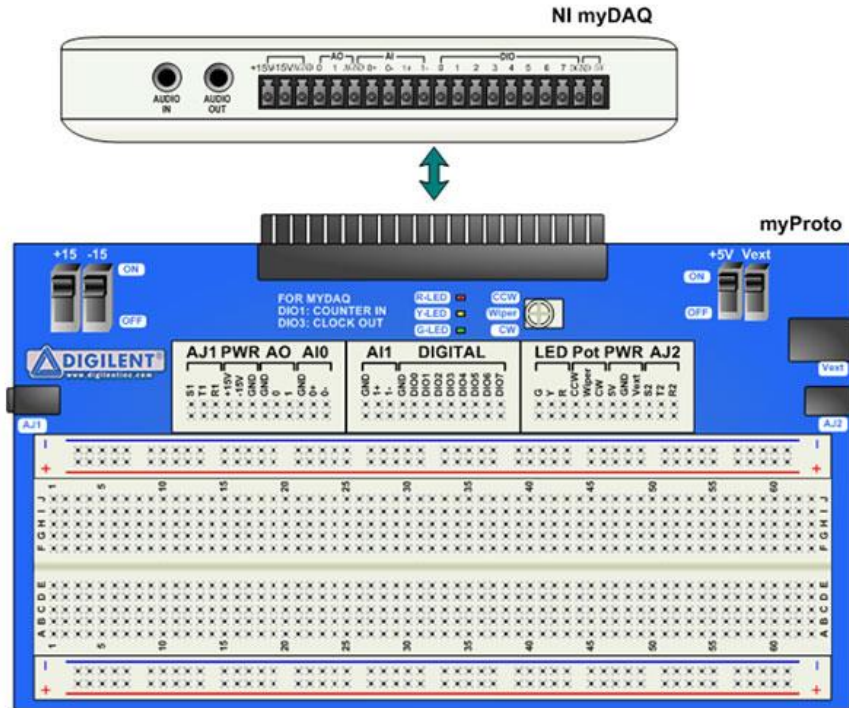


Figure 3. Connecting myDAQ to myProto.

Signal Connections: The NI myDAQ has several sets of signal connectors, three banana plugs for the multimeter, two audio jacks, and a 20-pin connector for various supply and input/output signals which are now available to you on the myProto board. It is beneficial for you to have a basic understanding of the main signals, their reference as well as direction, i.e. it is an input or an output:

Signal	Reference	Direction	Description
+15 V	AGND	Output	15 V supply, 32 mA max, 470 μ F
-15 V	AGND	Output	-15 V supply, 32 mA max, 470 μ F
AGND	N/A	N/A	Analog ground, reference for AO, AI, +15 V, -15 V
AO 0, AO 1	AGND	Output	Analog outputs, ± 10 V, 2 mA, 16 bits, 200 kS/s
AI 0+, AI 0-	AGND	Input	+ and – analog input, channel 0
AI 1+, AI 1-	AGND	Input	+ and – analog input, channel 1
DIO 0 to 7	DGND	Input/output	Digital input/output, 5V LVTTTL, 3.3V LVTTTL, max 4mA
5V	DGND	Output	5 V supply, 100 mA, max. 33 μ F

Grounding: The NI myDAQ (the NI ELVIS board in our lab as well) does not support floating measurements. Because the analog channels are differential, you need a ground point in the signal path. This is generally not a problem if you are working with the myDAQ only. If you use myDAQ’s AI 1+ and AI 1- to measure a floating source, e.g. a battery, you should connect AI 1- and the negative terminal of the battery to the analog ground (AGND). The DMM is ground referenced as well. More details on grounding can be found in the user guide of the NI myDAQ available on NI’s website <https://www.ni.com/pdf/manuals/373060g.pdf>.

Switches: A switch is used to manually connect the input of a gate to a HIGH or LOW voltage. For this lab we will use DIP (dual in-line package) switches, shown in Figure 4. There are 8 independent switches per DIP, labeled 1 to 8 as shown in Figure 4(a). As illustrated in Figure 4(b), in the ON position, the switch is closed, producing a short circuit between its contacts; in the OFF position, the switch is open, producing an open circuit between its contacts. To produce digital HIGH and LOW values, we connect one contact of each switch to ground (0 V) and the other contact to a pull-up resistor, with the other end of the resistor connected to 5 V, as shown in Figure 5. When the switch is OFF (open), the resistor pulls the line up to a HIGH state (hence the name “pull-up resistor”). When the switch is ON (closed), the output line will be connected to ground, and therefore the line will be in the LOW state. Instead of individual resistors, we will use a packaged resistor network, shown in Figure 6, which contains nine 330 ohm resistors. As shown in Figure 6(b), one side of each resistor is connected to a common bus (wire), which connects to pin 1 of the package. Pin 1 is indicated by a triangle on the package, as can be seen in Figure 6(a). We will connect this common bus to 5 V on the breadboard. The other resistor ends are connected to pins 2-10, which we will connect to individual DIP switches to produce the circuit of Figure 5. On the breadboard, the resistor pack should be inserted adjacent to one side of the DIP switches, so that pins 3-10 are shorted to the 8 DIP switch pins on the breadboard. Pin 1 of the resistor pack should extend two breadboard holes past the DIP switch, where it can be connected to 5 V. The resistor connected to pin 2 of the resistor pack will not be used.

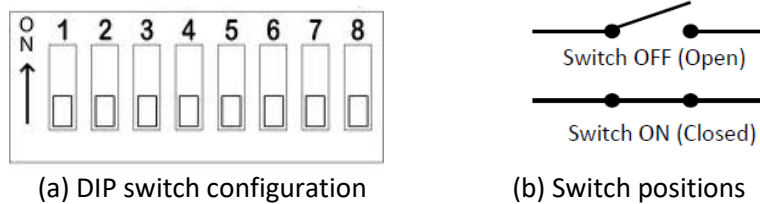


Figure 4. DIP (Dual In-line Package) Switches

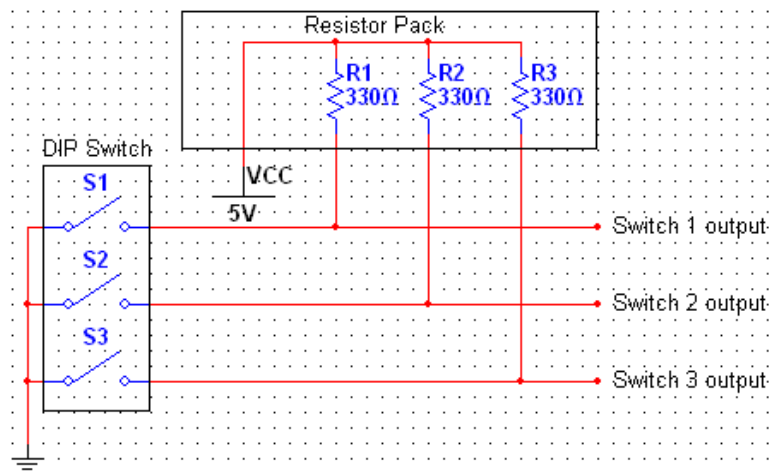
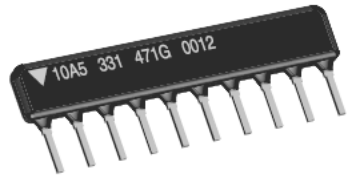
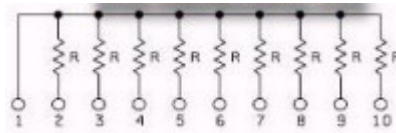


Figure 5. DIP switches with one side tied to ground and the other pulled up to 5 V via resistors.



(a) SIP package – pin 1 at left



(b) Resistor network schematic

Figure 6. SIP (Single In-Line Package) Resistor Network

Clock: A Clock is a circuit that produces a periodic output that alternates between HIGH and LOW voltage. We will use a clock signal to test some of our logic circuits.

LEDs: Light-Emitting Diodes (LEDs) can be used to display the state of any digital signal. Usually, LEDs are connected so that if the state is HIGH, the LED is on. There are only 3 LEDs on the myProto board, as shown in Figure 7. Connections to these LEDs are made via the breadboard holes on the upper side of the board, circled in Figure 7.

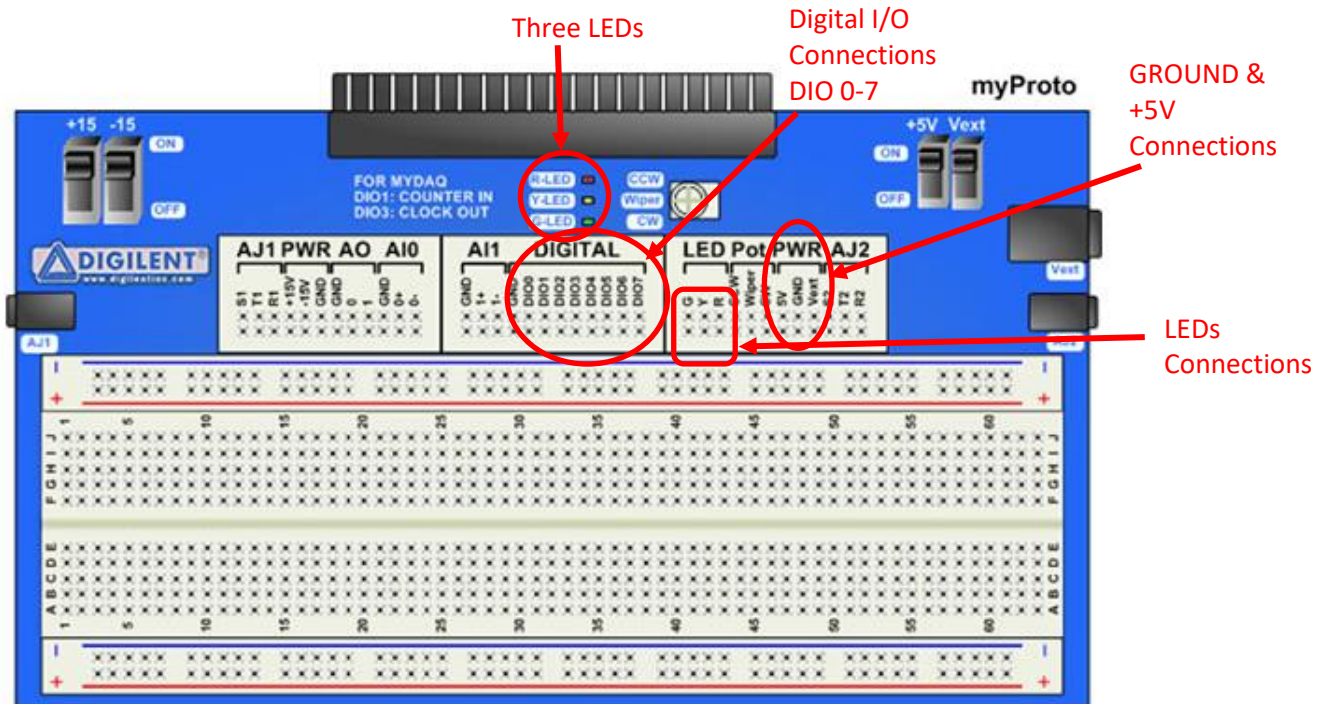


Figure 7. myProto Board

Sometimes we need to use more than three LEDs to display the digital signal, so we need to build a LED section ourselves. The circuit is easy, as shown in Figure 8 below. To provide appropriate current for the LED, a 220 ohms resistor is placed in series with the LED.



Figure 8. LED connection

Please make sure the resistor is in series with the LED before you turn on the power, otherwise there is a chance to blow up the LED which could be dangerous as well. The power controllers are on the left upper corner (+15V and -15V), and the right upper corner (+5V) of the board.

Digital Reader and Digital Writer

The NI myDAQ has a number of built-in instruments, listed in Table 1. The Digital Writer generates digital signals (patterns of 1s and 0s) that can be applied to the inputs of a circuit. This can be used in place of, or in addition to, switches to stimulate the circuit inputs. The Digital Reader can display the logic states of selected digital circuit wires. This can be used in place of, or in addition to physical LEDs.

Table 1. NI ELVISmx Instruments Available on Instrument Launcher

Instrument	Function
DMM	Digital Multimeter
Scope	Oscilloscope
FGEN	Function Generator
Bode	Bode Analyzer
DSA	Dynamic Signal Analyzer
ARB	Arbitrary Waveform Generator
DigIn	Digital Reader
DigOut	Digital Writer

To use the Digital Reader and Digital Writer, the myDAQ base unit must be connected to a PC with a USB cable. Once you install the driver of myDAQ, you can open the NI ELVISmx Instrument Launcher, shown in Figure 9, which contains icons to launch one or more of the instruments listed in Table 1.

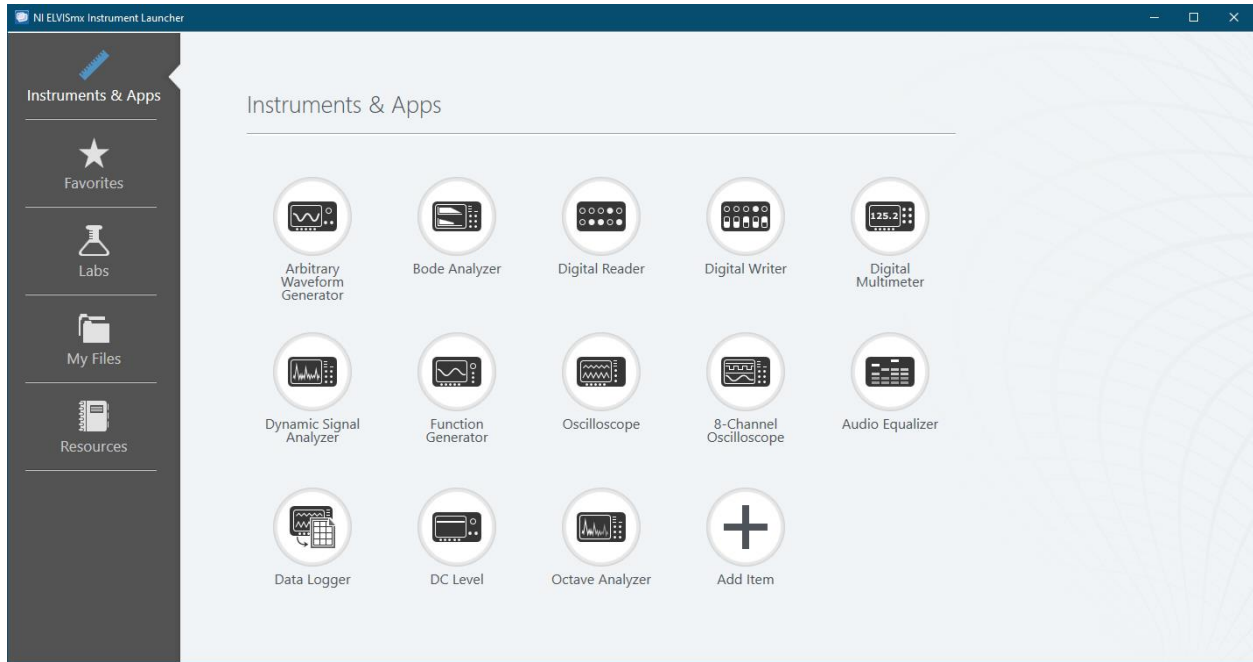


Figure 9. NI myDAQ Built-In Instruments

To launch the Digital Reader, click on “Digital Reader” in the Instrument Launcher. The Digital Reader, shown in Figure 10, displays the states of 8 digital signals connected to the DIO (Digital Input/Output) positions in the header at the upper side of the myProto board (see Figure 7 above.)

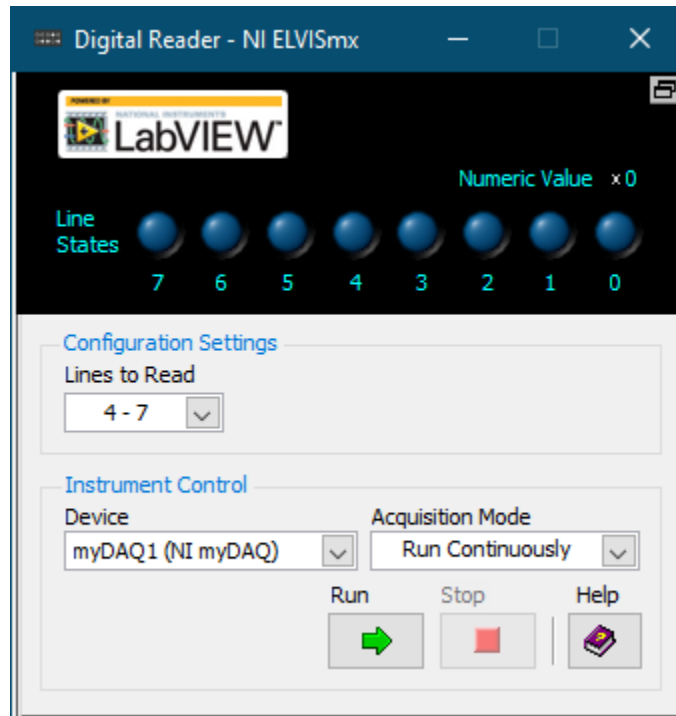


Figure 10. Digital Reader Window

DIO signals are allocated to the Digital Reader and Digital Writer in a group of 8 (DIO 0-7), or two groups of 4 (DIO 0-3, and DIO 4-7). Figure 11 shows an example of configuring DIO 4-7 for reading where other configurations are also visible in the selection menu. Each wire of the test circuit whose state is to be displayed in the Digital Reader should be connected to one of the DIO positions on the breadboard. Clicking the Run button in the Digital Reader initiates acquisition and display of signal states. In the Instrument Control section of the Digital Reader, “myDAQ1 (NI myDAQ)” should be selected as the Device and “Run Continuously” as the Operating Mode.

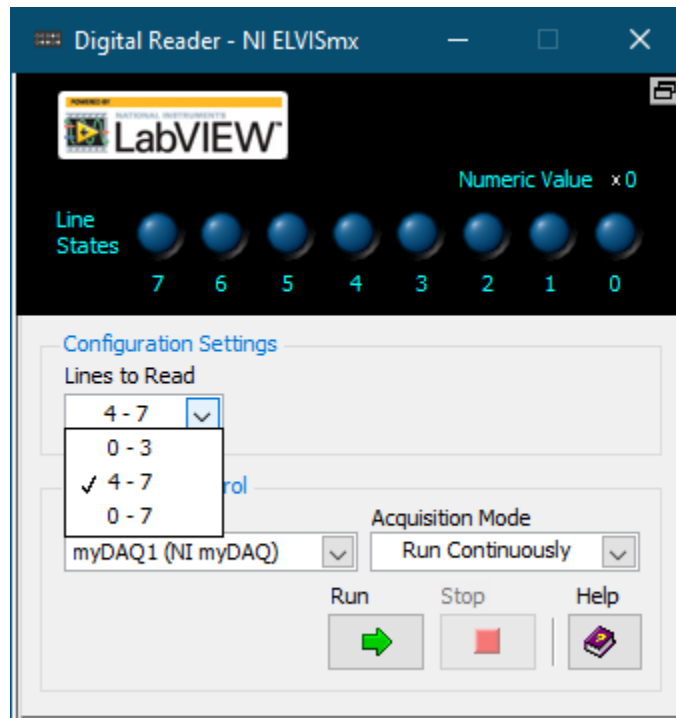


Figure 11. Groups of DIO signals.

The Digital Writer, shown in Figure 12, is launched by clicking on Digital Writer in the Instrument Launcher. Similar to the Digital Reader in its setup, the Digital Writer generates digital patterns on the 8 connected DIO signals. As can be seen in Figure 12, the states of the signals generated on the connected lines (in this case DIO 0-3) are shown at the top of the window. Digital patterns can be created manually by clicking on the slide switches in the center of the window, with “Manual” selected in the “Pattern” box, as shown in Figure 12. Several types of automatically-generated pattern sequences (binary counting, etc.) can also be generated by selecting the desired sequence type in the Pattern box, instead of “Manual”. A pattern can also be toggled, rotated and shifted via the buttons immediately below the slide switches.

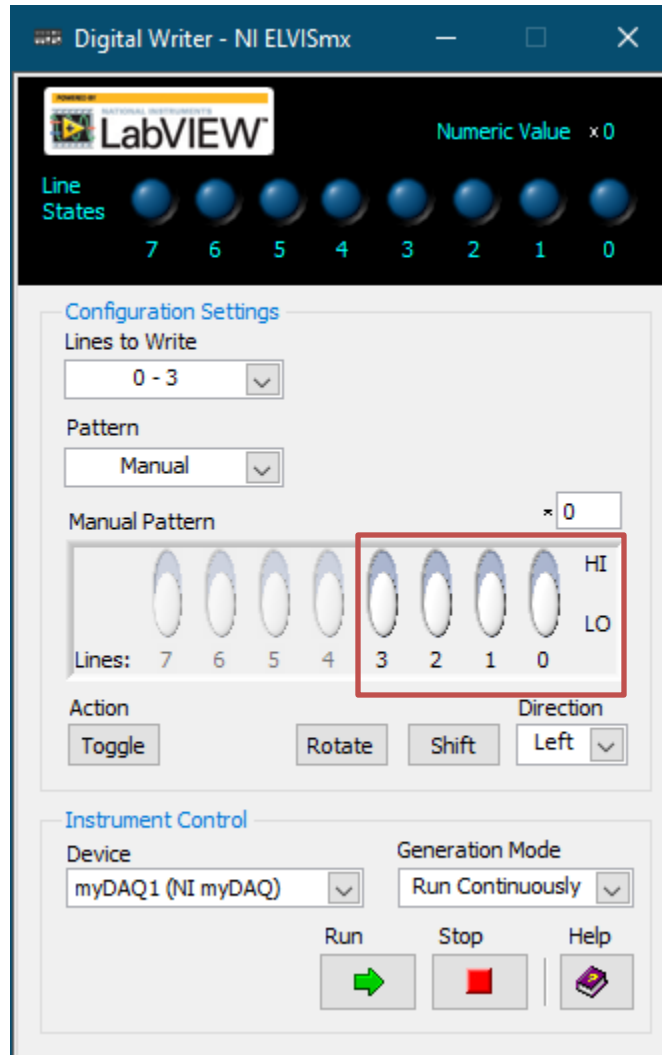


Figure 12. myDAQ Digital Writer Window

III. Pre-Lab

Using only 2-input NAND gates, design an implementation of a 2-to-1 multiplexer which has inputs A, B, and S and output Z, where $Z=A$ when $S=0$ and $Z=B$ when $S=1$. Construct the truth table for the multiplexer and use a Kmap to obtain a minimized SOP expression for the multiplexer. Draw the logic diagram for the 2-level AND-OR implementation for the minimized SOP expression, labeling all inputs and output. Use the Involution Theorem and DeMorgan's Theorems to obtain an all-NAND gate implementation of the circuit and draw the logic diagram labeling all inputs and output. Using the package-level drawing (i.e. the rectangle showing the 14 pins) of a 7400 Quad NAND gate integrated circuit, draw the connections of the various individual gates in the package to construct the multiplexer.

IV. Lab Exercise

Your lab instructor will show you how to insert DIP IC chips into the myProto breadboard, and also how to remove (extract) chips from the breadboard. Note that the myDAQ power supply outputs GROUND and +5V are available in the upper middle part of the board, as shown in Figure 7. ***You should always double-check power supply connections before you turn on the project board, as incorrect connections could damage NI myDAQ and chips.*** Each time you obtain a chip, inspect it to make sure it is the right part number (see the next paragraph), and to make sure all the pins are intact. If a pin breaks, inform your instructor.

STEP 1. DIP Switches

Insert the DIP switch and resistor pack into the breadboard, as described above. Since we need three switches for the experiment, insert wires to connect the opposite sides of three switches to GROUND on the breadboard, and connect the resistor side to the three LEDs on the breadboard, as shown in Figure 5. Turn on the power of the board, and then verify that each of the switches produces a HIGH value when the switch is open/OFF (turning the LED on), and a LOW value when the switch is closed/ON (turning the LED off). Do not take a part the circuit after you have finished Step 1, it will be used in the next step.

Before proceeding, have your GTA check off Step 1 on your checklist.

STEP 2. NAND Gate Truth Table

Connect a 7400 quad NAND gate and verify the truth table (record the truth table for your lab report). Connect two DIP switches to the inputs of one of the NAND gates, and connect the output to a LED in series with a 220 ohms resistor on the breadboard, as shown in Figure 8. The orientation of the NAND or any chip can be determined by locating which side has a “notch.” As demonstrated in Figure 13, the side with the “notch” is the top of the chip and is where Pin 1 is located. Verify the truth table for this gate by stepping through each of the four possible combinations of switch settings and recording the state of the LED.

Draw the circuit, labeling which pin numbers you use for each column of the truth table. Record your truth table and verify that this gate implements the NAND function. Repeat this process for each of the other three NAND gates on the chip (the main purpose of this is to help you learn how to count pins).

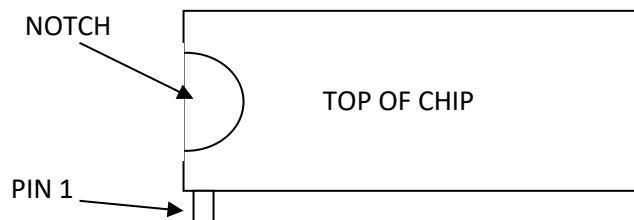


Figure 13. Identifying Pin 1

Before proceeding, have your GTA check off Step 2 on your checklist.

STEP 3. Multiplexer

ELEC 2210 Experiment 1 (Rev. 05/18/2020)

Connect the four NAND gates of the 7400 IC to construct your multiplexer design from the Prelab. Connect three DIP switches to the inputs of the multiplexer and connect the output to the LED in series with a 220 ohms resistor. Record and verify the multiplexer truth table for all possible input combinations, debugging your implementation as needed. Record each truth table and describe the problems and corrections you made to the circuit as you proceed to a working multiplexer.

Have your GTA check off Step 3 on your checklist.

STEP 4. myDAQ Digital Writer/Reader

Disconnect the switches from the circuit inputs from Step 3 (you may leave the LED connected to your circuit output). Open Digital Reader and Digital Writer instruments as described above, connecting the output of your multiplexer to DIO 4 for display in the digital reader and your three circuit inputs to DIO 0-1-2, to be controlled by the Digital Writer. Click Run in both the Digital Reader and Digital Writer windows, and reproduce the multiplexer truth table by manipulating the circuit inputs with the Digital Writer switches, and recording the state of the circuit output shown in the Digital Reader.

Have your GTA check off Step 4 on your checklist.

STEP 5. Cleanup

Return all components, put away all wires, and turn off all equipment.

Have your GTA inspect your workstation and check off the cleanup on your checklist if acceptable.

If your circuit is not operating correctly at the end of the lab period, you may lose some or all of your in-lab points.

Submit your report to your GTA's mailbox prior to the start time of your lab period one week from today. Attach the required cover sheet and your initialed checklist to your report.