Chapter outline

Sunday, June 10, 2012 10:38 AM

MOSFET Chapter Outline

- Describe field effects and operation of MOSFETs.
- Understand cutoff, linear and saturation operation regions for given circuit.
- Develop mathematical models for I-V characteristics of MOSFETs.
- Develop concept of load line for MOSFET circuits
- Analyze operation of resistor load inverter
- Describe sources of capacitance in MOSFETs.
- Master dc/dc sweep simulation of MOSFET circuits using spice, including spice model parameter editing and W/L specification

N-channel (electron channel) MOS Field Effect Transistor

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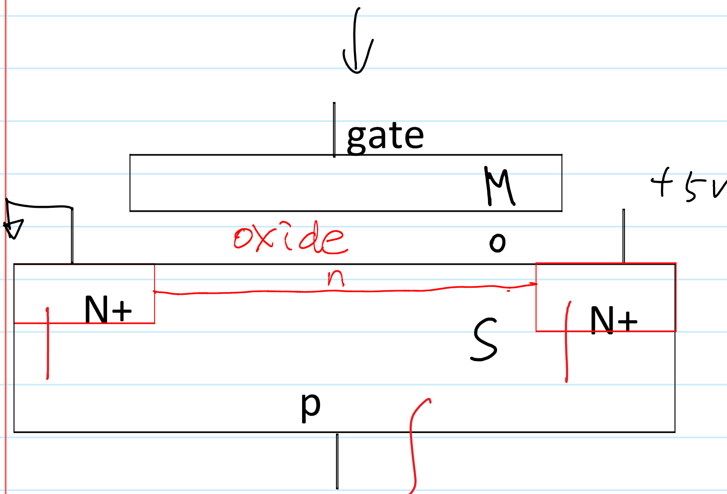
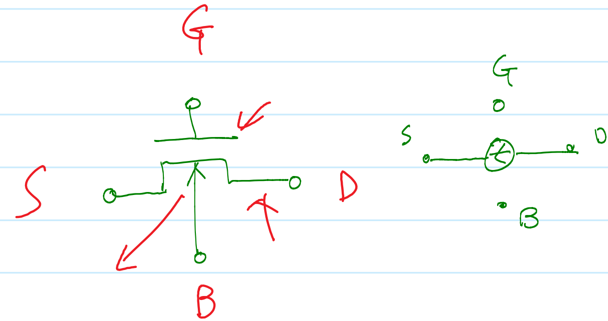


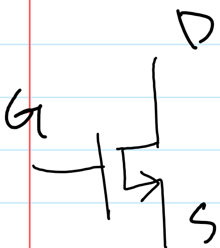


circuit symbol

arrow points from P-body -> N-channel

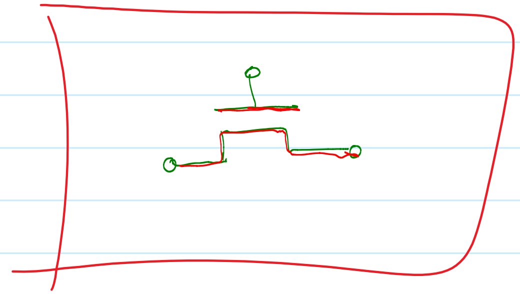
- p-substrate
- gate and gate oxide
- two N+ regions (meaning ND is high)
- Gate bias can be used to invert the surface from p-type to n-type, creating an electron channel connecting the two N+
- we can thus control current flowing between the two N+ using gate bias

Other Symbols of N-MOSFET:



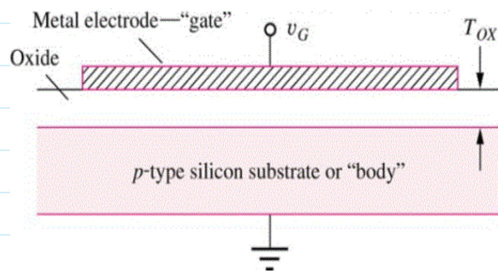
17s

in our text



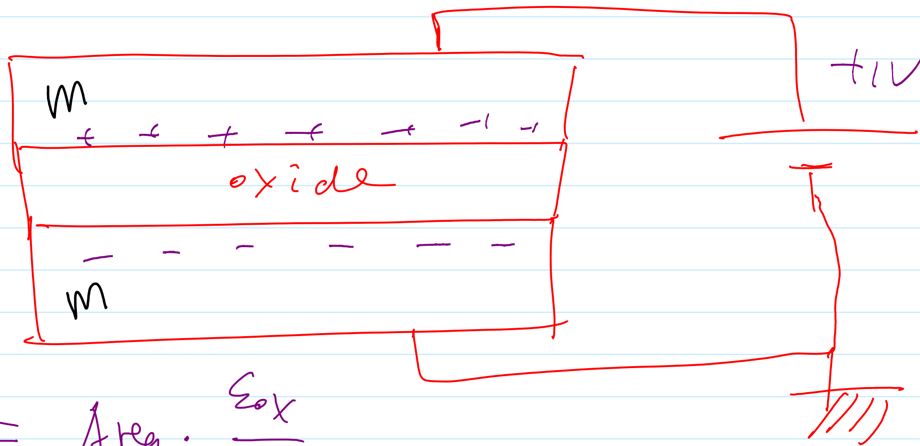
body not shown

2 terminal MOS Capacitor Physical Structure



- (**M**etal) Gate electrode: low-resistivity metal in early days, and later polycrystalline silicon (N+ or P+ for low resistivity) - now metal again in year 2011
- (**O**xide) Silicon dioxide:stable high-quality electrical insulator. T_{ox} is as thin as 1-2nm in state of the art technologies
- (**S**emiconductor) Semiconductor substrate or Body: *n*- or *p*-type Si

What happens in an ordinary capacitor if we apply a voltage difference (vertical field)?



$$Q = C \cdot V$$

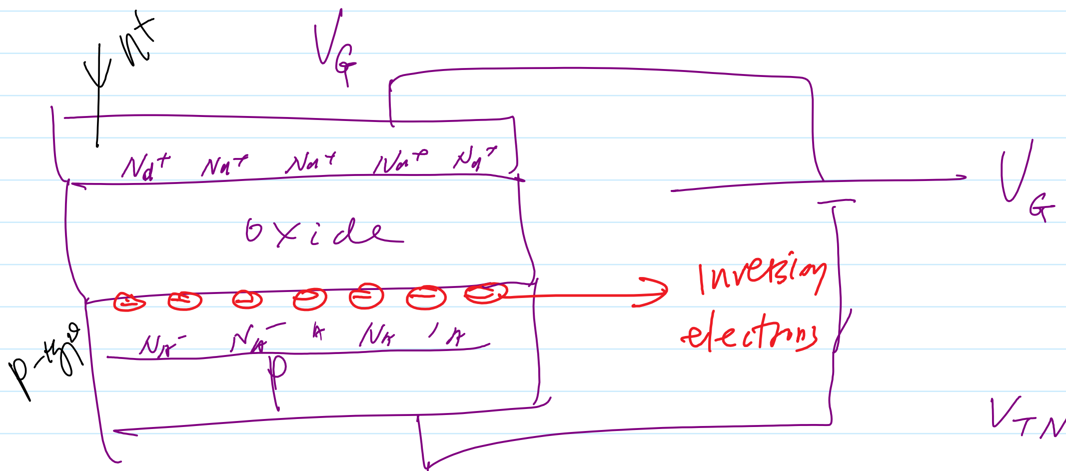
$$C = \text{Area} \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C''_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

We will induce negative charge - electrons on the negative metal plate in an ordinary capacitor.

If the negative plate is p-type semiconductor instead of metal, at lower voltage, the negative charge is initially made of ionized acceptors (Na), when the capacitor voltage exceeds a threshold, electrons are induced at the surface, we say the surface is inverted (as it was p-type at voltages below threshold, now is n-type at voltages above threshold). In fact, the positive electrode is semiconductor too, say, N+ Si.

What happens in an N+/oxide/p-Si capacitor if we apply a voltage difference?

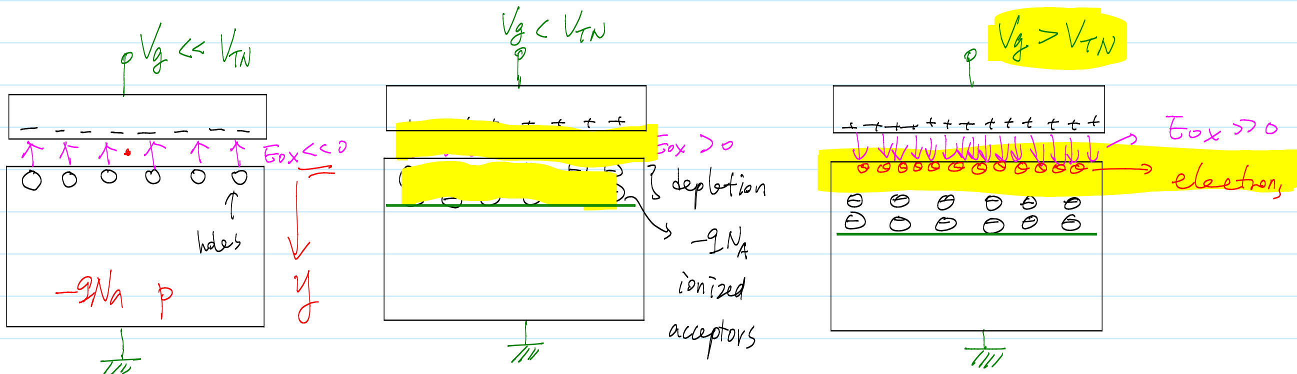


$$C_{ox}'' = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$Q_I' = -C_{ox}''(V_G - V_{TH}) \qquad V_G \geq V_{TH}$$

$$\approx 0 \qquad V_G \leq V_{TH}$$

Vertical Field Effect in nMOS (p-substrate)



If VG is sufficiently small compared to a threshold, surface is accumulated with holes.

Surface is depleted of electrons and holes

At high enough VG, vertical field is strong enough to induce electrons at the surface of p-body.

Surface is now inverted from p-type to n-type electrically.

Vertical Field Induced Inversion Charge Density (charge per unit area)

area)

Inversion electron charge density to first order:
QI' = -Cox''(VG - VTN)
VTN: is called **threshold voltage**, the threshold gate voltage level for creating significant amount of inversion charge

the *negative sign* simply indicates the charge is made of inversion electrons

Cox''=eox/Tox is oxide capacitance per unit area
e ox=oxide permittivity (F/cm)
Tox=oxide thickness (cm)

Equation only applicable when VGS > VTH !!!
That is, the number of inversion electrons must be positive!

Numerical Example:

Consider a state-of-the-art 22nm technology MOS capacitor with VT=0.2V, tox=1nm.
1) Find the number of inversion electrons induced per square nm area (nm^2) at Vg = 1.2V.

2) For a 66nm x 22nm area MOS cap in the 22nm CMOS technology above, how many inversion electrons are induced at Vg=1.2V?

$Q_I' = -C_{ox}''(V_g - V_{TH})$

$C_{ox}'' = \frac{\varepsilon_{ox}}{t_{ox}}$ ← 1nm

$Q_{inv}' = -C_{ox}''(V_g - V_T) = -\frac{\varepsilon_{ox}}{t}(V_g - V_t)$

$$Q'_{inv} = -C''_{ox}(V_g - V_T) = -\frac{\varepsilon_{ox}}{t_{ox}}(V_g - V_t)$$

$$N'_{inv} = \frac{Q'_{inv}}{-q}$$

$$N = N'_{inv} \times 66\,nm \times 22\,nm$$

Solution:

oxide permittivity = 3.9 * epsilion_0

epsilon_0: vacuum permittivity,

$\varepsilon 0 = 8.854187817620\times 10^{-14}$ F/cm

```
    epox_r = 3.9    # dimensionless
    ep0 = 8.85e-14  # F/cm
    nm_to_cm = 1e-7
    cm_to_nm = 1./nm_to_cm
    epox = epox_r * ep0


    tox_nm = 1
    tox_cm = tox_nm * nm_to_cm

    coxpp = epox / tox_cm    # F / cm^2

    vt = 0.2
    vg = 1.2
    vgt = vg - vt

    area_nm2 = 66 * 22

    qinvp = coxpp * vgt # F*V/cm^2, so C/cm^2
    q = 1.6e-19

    num_electrons_per_cm2 = qinvp / q

    num_electrons_per_nm2 = num_electrons_per_cm2 * (nm_to_cm)**2

    print 'For tox = %3.1f nm, VT = %3.1f V, %g electrons are induced per nm^2 area
at %3.1f V gate voltage' % (tox_nm, vt, num_electrons_per_nm2, vg)
```

For tox = 1.0 nm, VT = 0.2 V, 0.215719 electrons are induced per nm^2 area at 1.2 V gate voltage
For an area of 1452.0 nm^2, 313.224 electrons are induced

q	float	1.6e-19
qinvp	float	3.4515000000000003e-06
tox_cm	float	1e-07
tox_nm	int	1
vg	float	1.2
vgt	float	1.0
vt	float	0.2

area_nm2	float	1452.0
cm_to_nm	float	10000000.0
coxpp	float	3.4515000000000003e-06
ep0	float	8.85e-14
epox	float	3.4515e-13
epox_r	float	3.9
main	function	<function main at 0x0377F230>
nm_to_cm	float	1e-07
num_electrons	float	313.223625
num_electrons_per_cm2	float	21571875000000.004
num_electrons_per_nm2	float	0.21571875000000001

4 terminal MOS

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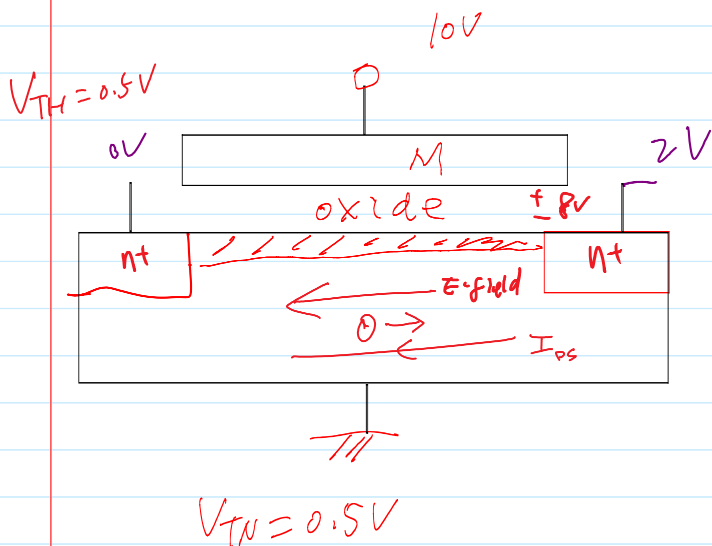
N-MOS Field Effect Transistor (n-MOSFET)

- Substrate is **p-type**, there are two **n+** regions
- assume VTN = 0.5V, if we apply 10V at the gate, such that VGS (10V) > VTN, the surface is **inverted** to n-type

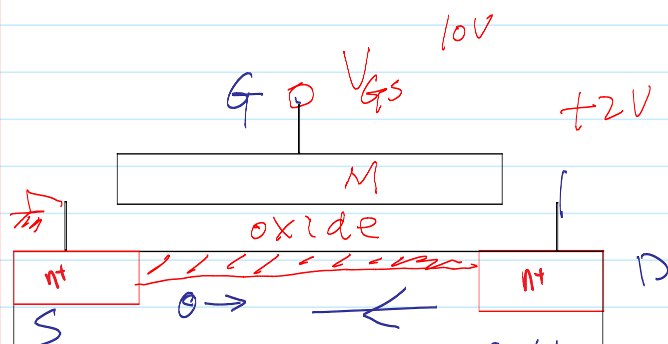
- The two N+ regions are now connected by the inverted n-surface, or channel

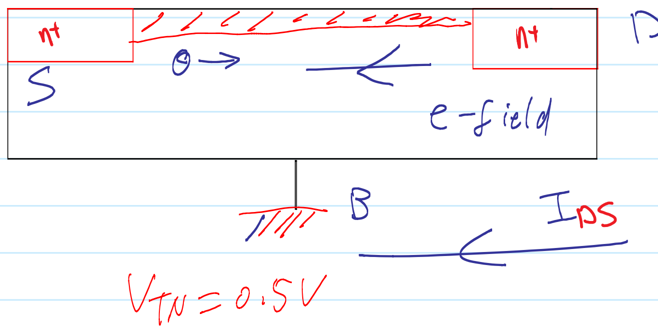
- now let us add 2V to the second N+ region, the first N+ region is grounded, to which direction should electrons drift?



What is direction of electron drift motion?
What is direction of current flow?
Which n+ is source of electron flow? (left, right)
Which n+ is drain of electron flow? (left, right)

- Electrons drift from lower voltage N+ to higher voltage N+
- So the lower voltage N+ region is the Source of electron flow and the higher voltage N+ region is the Drain of electron flow (exit)
- current flows from Drain to Source





In NMOSFET:

Higher Voltage N+ side is (Electrical) Drain

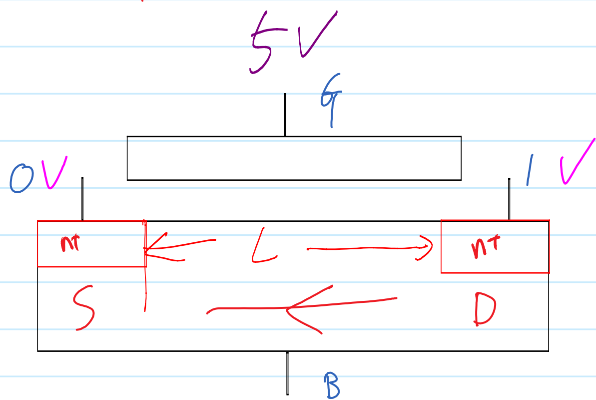
Lower voltage N+ side is (Electrical) Source

Electrical source/drain is determined electrically and can dynamically change from time to time!
Current flows from Drain to Source!

Drain and Source Exercise for n-MOSFET

$V_T = 1V$

$V_{XY} = V_X - V_Y$

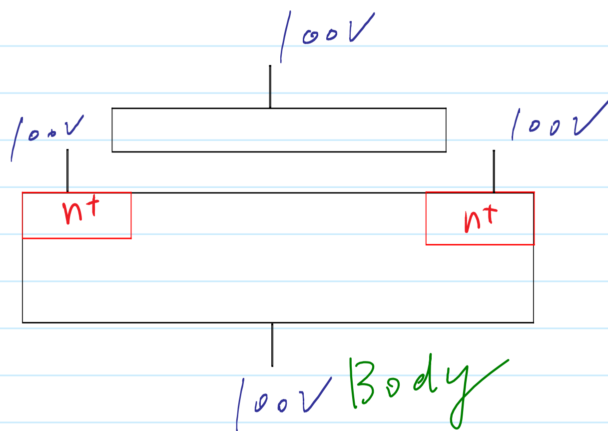


−2V

Body

$V_{GS} = ?$ 5V

$V_{DS} = ?$ 1V



?

$V_{GS} = ?$ 0

$V_{DS} = ?$ 0

W and L

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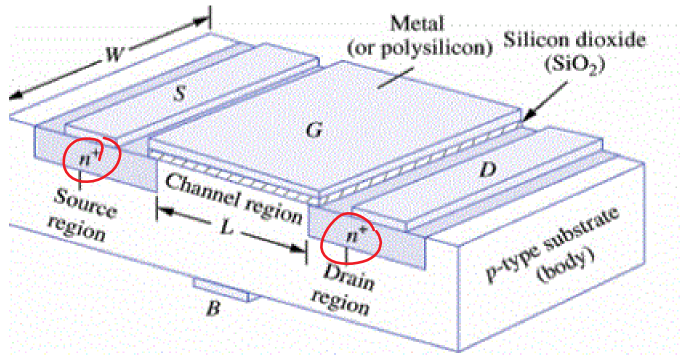
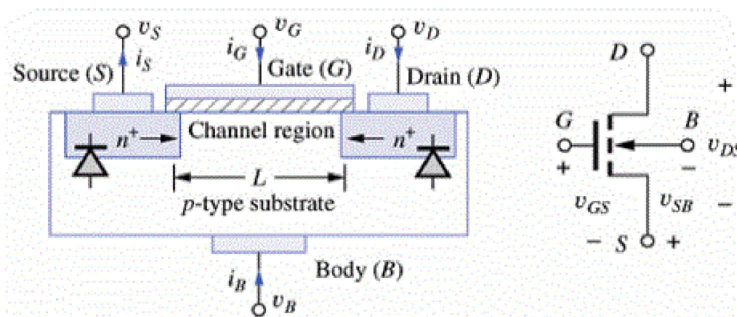
A 3-D Picture / Gate Width



$\frac{W}{L}$



- 4 device terminals: Gate(G), Drain(D), Source(S) and Body(B).
- Source and drain regions form pn junctions with substrate.
- vSB, vDS and vGS always positive during normal operation.
- vSB always < vDS and vGS to reverse bias pn junctions

Cutoff Operation Region (VGS < VTN)

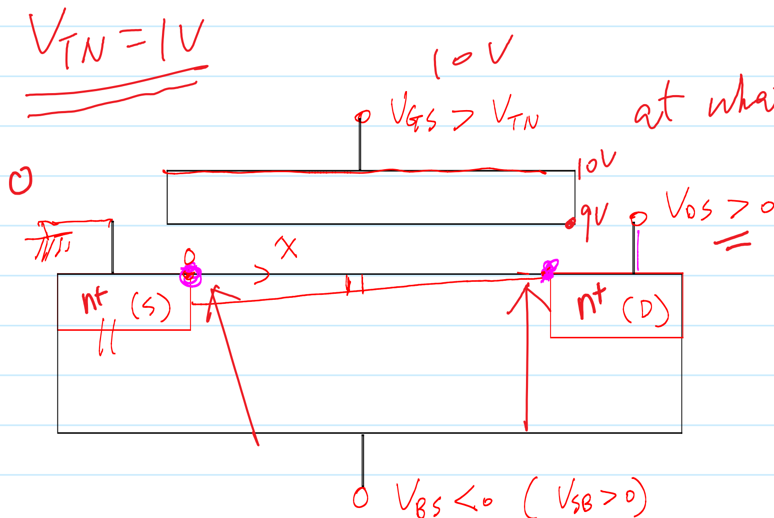
Turn-on Region (VGS >= VTN)

- Linear Region (VDS < VGT)
- Saturation Region (VDS >= VGT)

$V_{GS} - V_{TN}$

V_{TH}

Inversion Charge Density Along channel



at what V_{ds} $Q'_I(x=L)=0$?

thickness of red channel indicates inversion charge density

thicker means higher

$$Q'_I(x) = -C''_{ox}\left(V_{GS} - V(x) - V_{TN}\right)$$

VGS-V(x) : Net voltage available to induce an inversion layer, it decreases from S to D

$V(x)=0$ at $x=0$ (S end)

V(X): potential at x

$V(x) = 0$ at $x = 0$ (S end)

$V(x) = V_{DS}$ at $x = L$ (D end)

$$Q_I'(x=L) = -C_{ox}''(V_{GS} - V_{DS} - V_{TN})$$

layer, it decreases from S to D

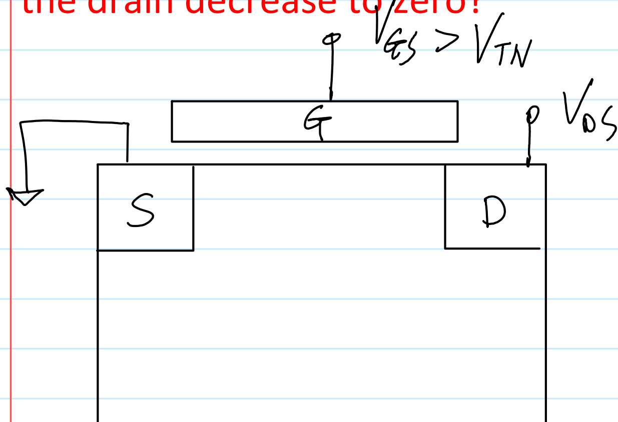
V(X): potential at x with respect to source

Difference between Net Voltage and threshold voltage determines inversion charge density
net voltage must be above threshold to produce inversion charge

Inversion charge density at source is:
QIs' = -Cox''(VGS - VTN)

Inversion charge density at drain is:
QID' = -Cox''(VGS - VDS - VTN)

Question: at what VDS will the inversion charge at the drain decrease to zero?



$V_{DS} = V_{GS} - V_{TN}$

The **linear** or triode **region** of operation is defined as one in which the **entire channel** region between source and drain **is inverted**.

$V_{GS} > V_{TH}$, $0 < V_{DS} < V_{GT}$

$V_{GT} \triangleq V_{GS} - V_{TH}$

Again, for a given VGS, at what VDS does the inversion charge
density at drain become zero?

$V_{DS} < V_{GS} - V_{TN}$

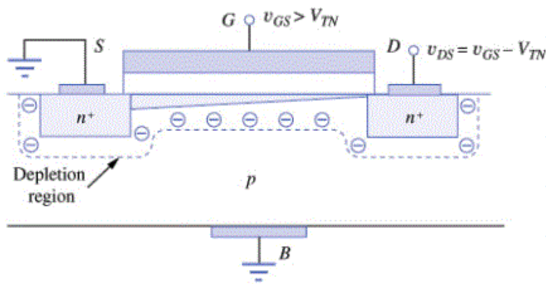
Drain end inversion charge decreases to "zero" or

VGD is just equal to threshold voltage (VTN)

VGD = VGS-VDS
VGD = VTN

So MOSFET is in linear operation region when 0 < VDS < VGS - VTN

or 0 < VDS < VGT



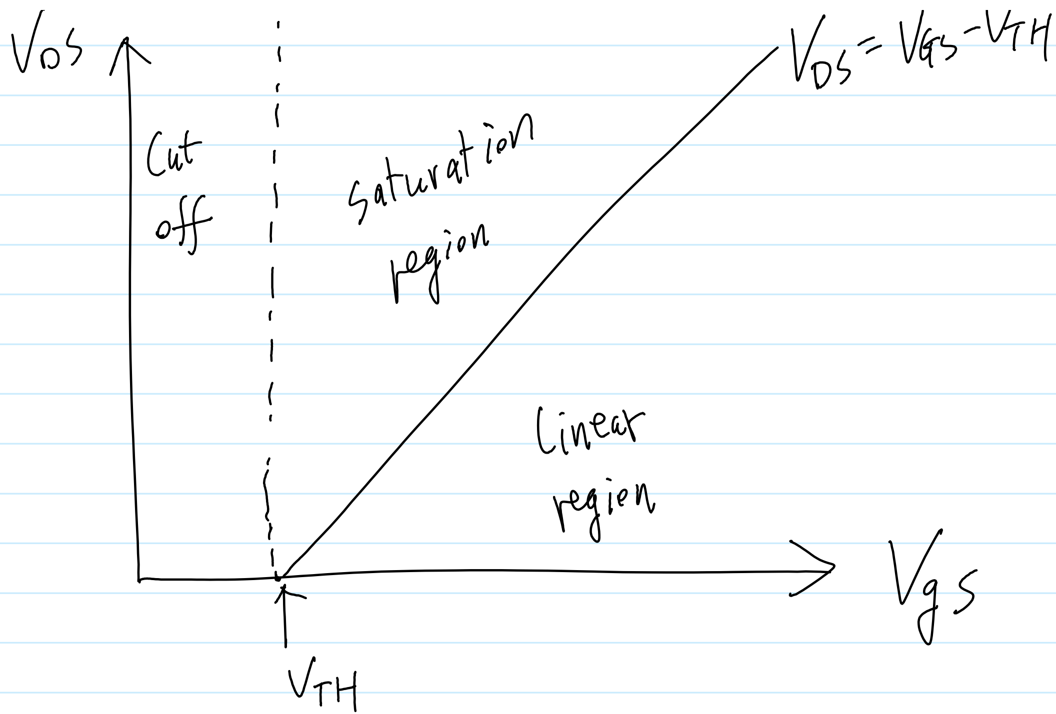
Gate Overdrive VGT:

VGT = VGS - VTN is called the gate bias overdrive, the amount of overdrive with respect to threshold voltage VTN

MOSFET Operation Regions

V_{DS} ↑

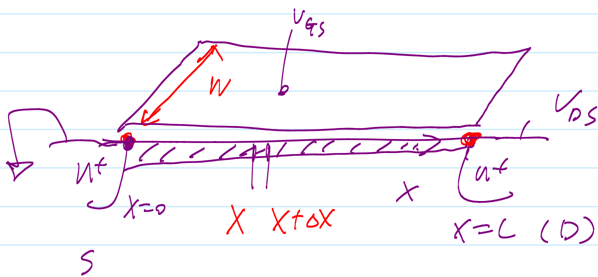
$V_{DS} = V_{GS} - V_{TH}$

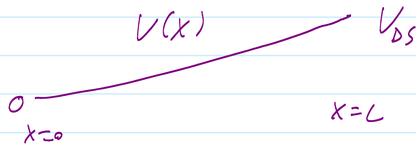


When 0<VDS<VGT, NMOS works in linear region.
When VDS > VGT, NMOS works in saturation region, so VGT is also called Drain Saturation Voltage VDSAT.

MOSFET I-V Equation Derivation Proper

MOSFET I_{DS} Equation derivation



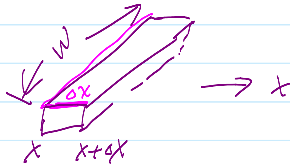


Consider a small segment from x to $x+\Delta x$

$-C_{ox}''(V_{GS}-V(x)-V_T)$

$\downarrow$

$Q_n' \cdot W \cdot \Delta X$



Recall definition of current

$$I = \frac{\text{charge inside the bar}}{\text{time for all charges to move out}}$$

$$= \frac{W \cdot Q_n' \cdot \Delta X}{\frac{\Delta x}{v_n}}$$

$$= W Q_n' v_n$$

$$= W Q_n' v_n$$

Q_n' is electron charge per area

$$Q_n'(x) = -C_{ox}''(V_{GS} - V(x) - V_{TN})$$

$$V_{GT} \triangleq V_{GS} - V_{TN}$$

$$-C_{ox}''(V_{GT} - V(x))$$

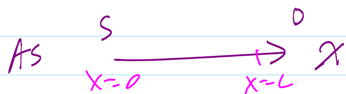
$$v_n = -\mu_n \cdot E = -\mu_n \cdot \left(-\frac{dV}{dx}\right)$$

$$I = -WC_{ox}''\mu_n (V_{GT} - V(x)) \frac{dV}{dx}$$

$$-I\,dx = W C_{ox}''\mu_n (V_{GT} - V(x))\, dV(x)$$

$$V_{GT} \triangleq V_{GS} - V_{TN}$$

gate over drive



define I_{DS} (I from D to S)

so $I_{DS} = -I$

$$K'(KP) = \mu_n C_{ox}''$$

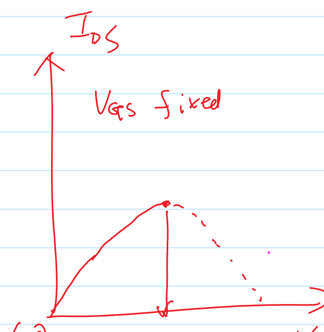
$$\int_0^L I_{DS}\,dx = W C_{ox}''\mu_n \left[\int_{x=0}^{L} V_{GT} \cdot dV - \int_{x=0}^{L} V\,dV\right]$$

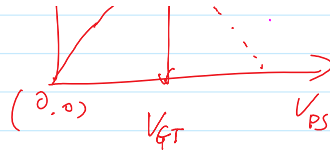
$$I_{DS} \cdot L = W C_{ox}''\mu_n \left[V_{GT}(V_{DS} - 0) - \frac{1}{2}(V_{DS}^2 - 0^2)\right]$$

KP

$$K_n \triangleq K_n' \cdot \frac{W}{L}$$

$$I_{DS} = \frac{W}{L} C_{ox}''\mu_n \left[V_{GT} V_{DS} - \frac{1}{2} V_{DS}^2\right]$$





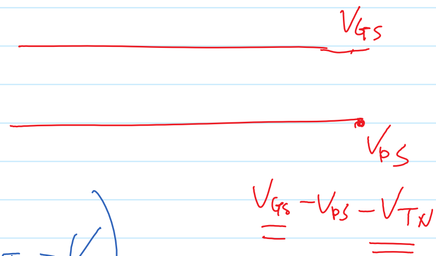
Keep in mind this holds only when

$$Q_n(x) = -C_{ox}''(V_{GT} - V(x)) < 0$$

or the number of inversion electrons > 0.

That is $V_{GT} - V(x) > 0$

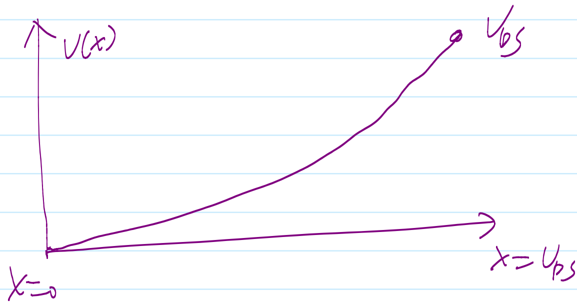
or $V(x) < V_{GT}$



$$Q_n(x=L) = -C_{ox}''(V_{GT} - V_{DS}) < 0$$

$$V_{GT} - V_{DS} > 0$$

$$V_{DS} < V_{GT}$$



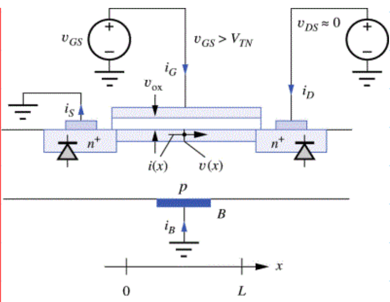
Recall $V(x)$ is highest at $x=L$

So as long as $V_{DS} < V_{GT}$,

This equation holds. That is

$$\boxed{0 < V_{DS} < V_{GT}}$$

linear operation region.



$I_{DS} = 0 \quad$ if $\quad V_{GS} < V_{TN}$

if $0 < V_{DS} < V_{DSAT} \; (V_{GT} \triangleq V_{GS} - V_T)$

$$I_{DS} = K_n \left(V_{GT} - \frac{V_{DS}}{2} \right) V_{DS} \leftarrow$$

(red annotations: V_{GT} above V_{DS} in both places)

$K_n = K_n' \cdot \frac{W}{L}$ $\qquad$ $\underline{\underline{K_n'}} = \mu_n C_{ox}''$

KP

If $\; V_{DS} > V_{DSAT} \; (V_{GT})$

$$I_{DS} = I_{DSAT} = K_n \cdot \frac{V_{GT}^2}{2} \leftarrow$$

Id-Vd output curves

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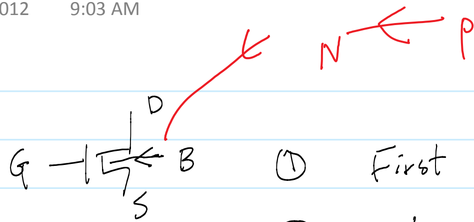


① First identify which n^+ is S and D

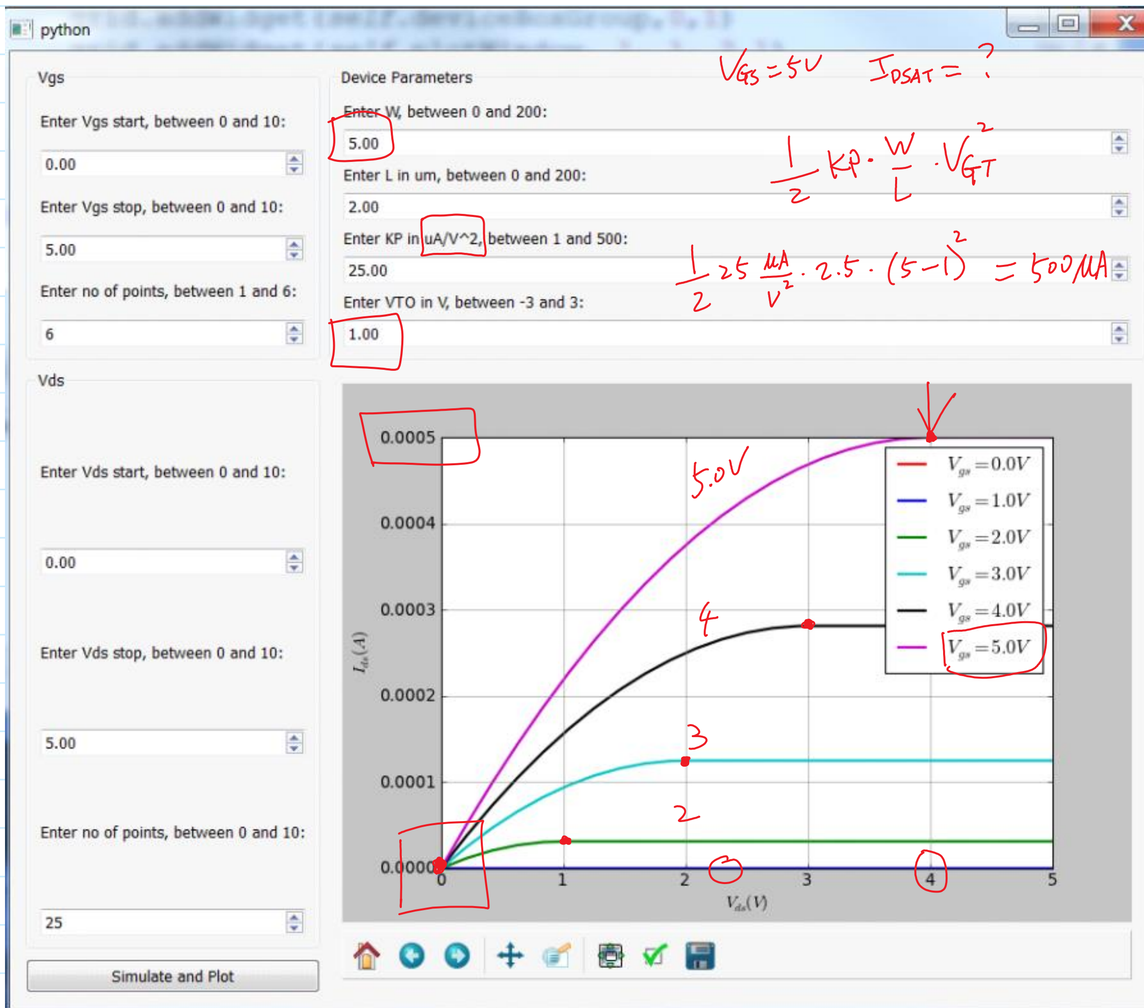
② $V_{DS} > 0$ $V_{SB} > 0$ $K_n = K_n' \frac{W}{L}$ $K_n' = \mu_n C_{ox}''$

If $V_{GS} < V_{TN}$, $I_D \approx 0$, device is "off"

else

if $0 < V_{DS} < V_{GT}$, $I_D = K_n \cdot \left(V_{GT} \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$ Linear

if $V_{DS} \geq V_{GT}$, $I_D = K_n \cdot \frac{V_{GT}^2}{2}$ Saturation



$V_{dsat} = ?$

$V_{GS} - V_{TN}$

Note where the drain current saturates with Vds - it occurs at Vds = Vgt (Vgs - Vt)

In our text, Vt for NMOS is written as Vtn.

I'd like you to remember some critically important biasing conditions at which Ids = 0:

- Vds=0 independent of Vgs
- Vgs < Vt independent of Vds

Determining NMOS current

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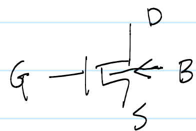
Determining N-MOSFET Current

First figure out S, D, G, B
Figure out VGS, VDS, VTN
Calculate gate overdrive VGT=VGS-VTN
If VGT < 0, device is in cutoff (or off), IDS = 0

If VGT >0, device is on. Vdsat = VGT
    If Vds < Vdsat, Ids follows Ids = Kn * (VGT - Vds/2) * Vds,
    If Vds > Vdsat, Ids saturates at constant value Idsat,
        independent of vDS.
      Idsat is simply Ids at Vds=Vdsat,
      Idsat = kn * Vgt^2 / 2

Summary:



① First identify which n^+ is S and D

② $V_{DS} > 0$ $V_{SB} > 0$ $K_n = K_n' \frac{W}{L}$ $K_n' = \mu_n C_{ox}''$

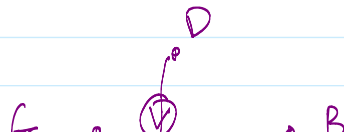
If $V_{GS} < V_{TN}$, $I_D \approx 0$, device is "off"

else

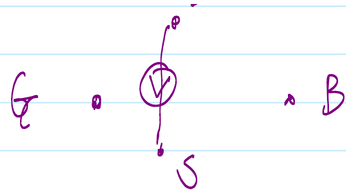
if $0 < V_{DS} < V_{GT}$, $I_D = K_n \cdot \left(V_{GT} \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$ Linear

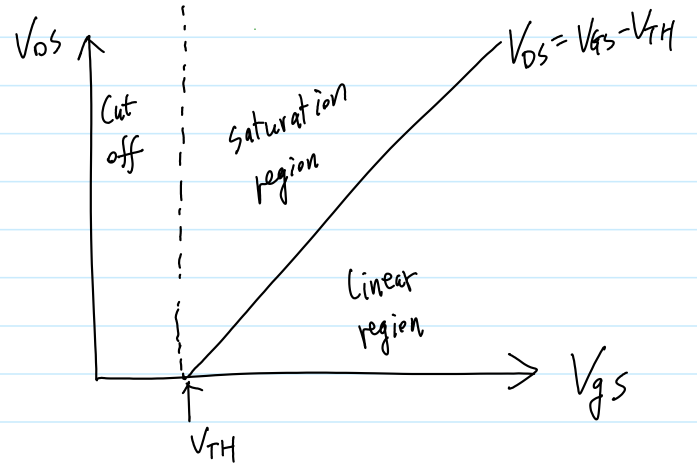
if $V_{DS} \geq V_{GT}$. $I_D = K_n \cdot \frac{V_{GT}^2}{2}$ Saturation

end



V_{DS} ↑ $V_{DS} = V_{GS} - V_{TH}$


G
B
S

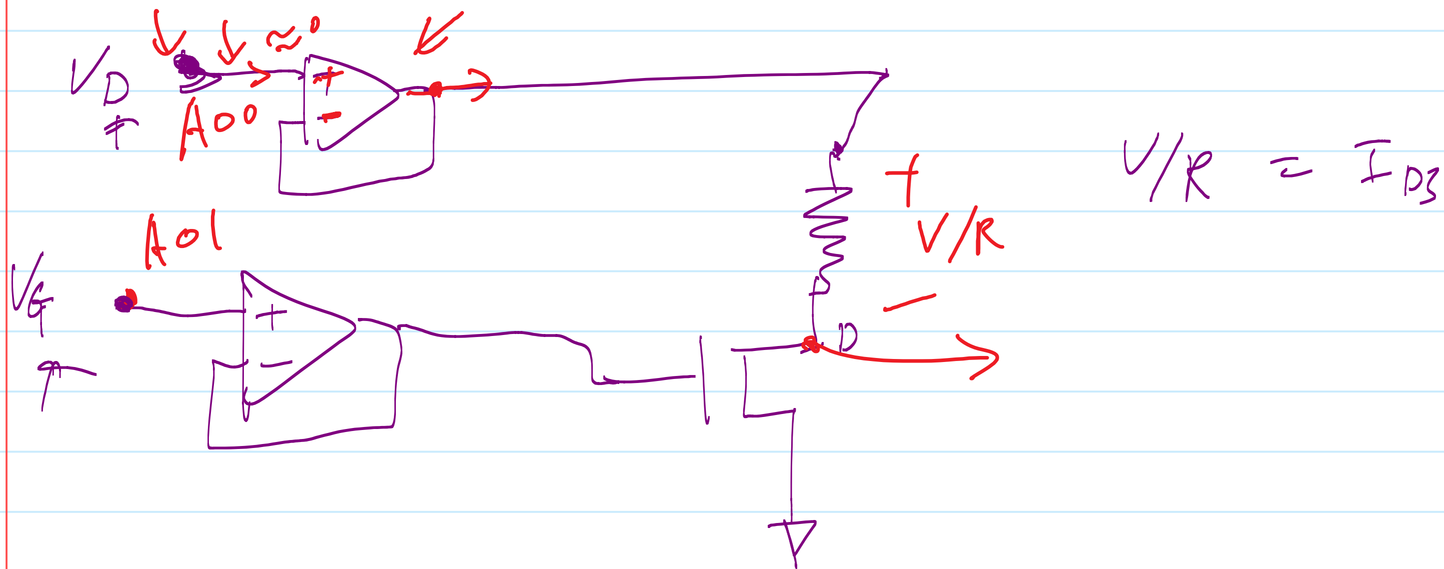

VDS
Cut off
saturation region
VDS = VGS - VTH
linear region
VGS
VTH

Experimental I-V

Sunday, June 10, 2012 12:05 PM

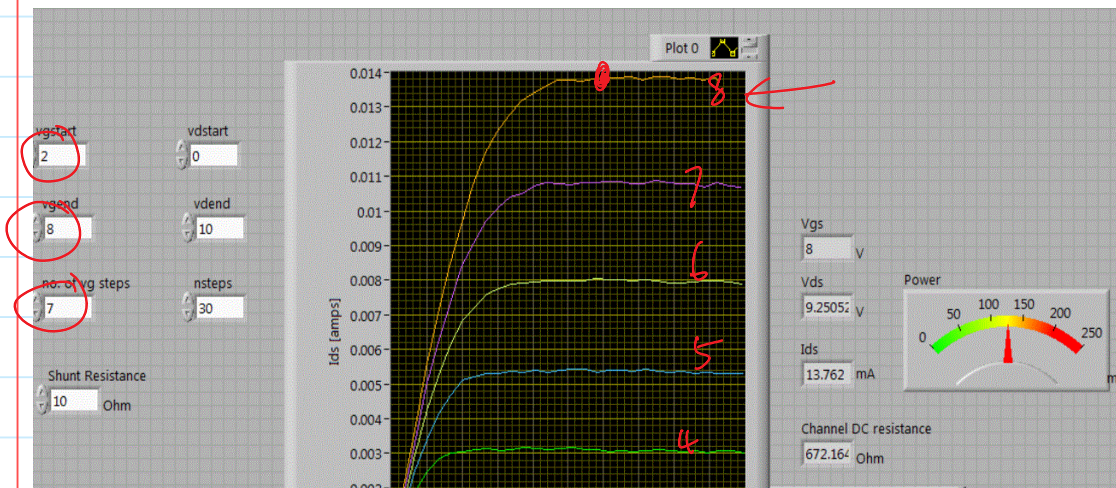
Real MOSFET I-V Characteristics

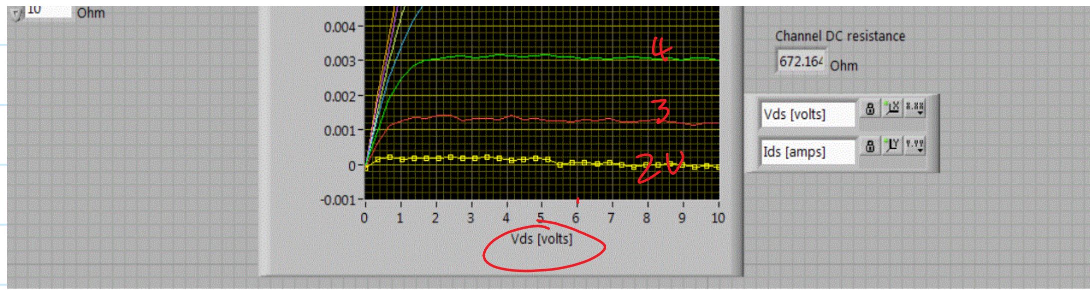
We will make this measurement in our lab with two OPAMP's and a shunt resistor for converting current to voltage



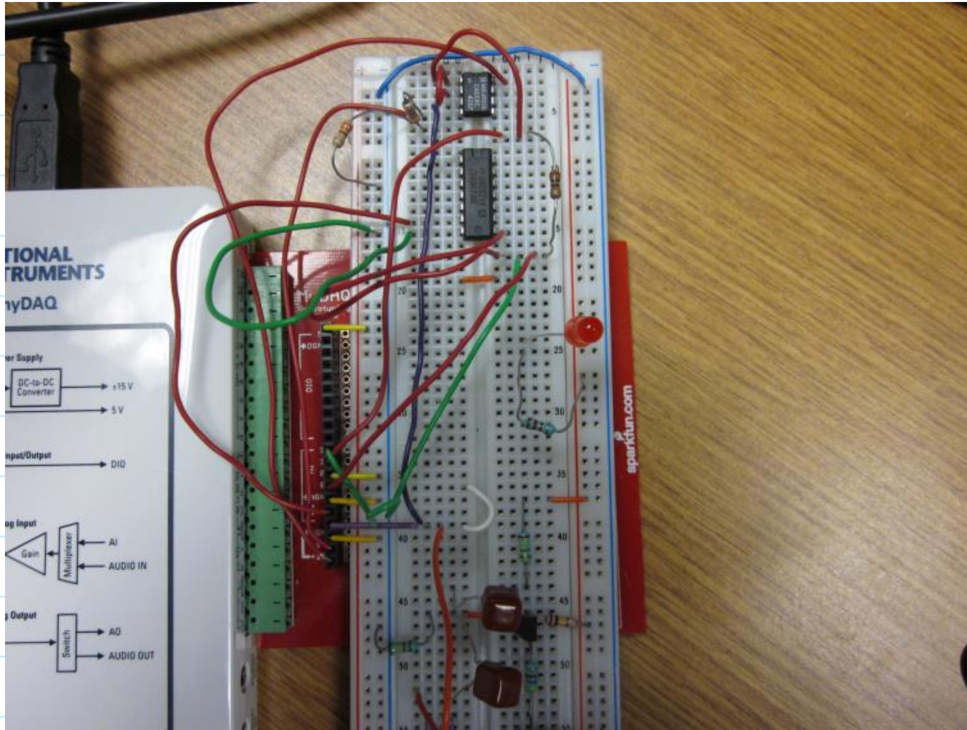
CD4007 NMOS

Can you estimate VTH? What about Vdsat at Vgs=8V?





Circuit used:



Spice simulation and numerical example of I-V

Monday, March 12, 2012 4:42 PM

```
** nmos_id_vd **
*
* NI Multisim to SPICE Netlist Export
* Generated by: GuofuNiu
* Mon, Sep 26, 2011 10:08:53
*

*## Multisim Component V2 ##*
vV2 d 0 dc 12 ac 0 0
+         distof1 0 0
+         distof2 0 0

*## Multisim Component V1 ##*
vV1 g 0 dc 12 ac 0 0
+         distof1 0 0
+         distof2 0 0

*## Multisim Component Q1 ##*
MQ1 d g 0 0 IDEAL_4TEN__TRANSISTORS_VIRTUAL__1__
1 L=2e-006 W=5e-006 AD=0 AS=0 PD=0 PS=0 NRD=1 NRS=
1 M=1


.MODEL IDEAL_4TEN__TRANSISTORS_VIRTUAL__1__1
NMOS
+  (
+ LEVEL= 1
```

K' → KP

K → KP

+ LEVEL= 1
+ VTO= 1
+ KP= 25e-6

25 $\mu A/V^2$ 25×10^{-6} A/V^2

+ ~~GAMMA= 0.0~~
+ PHI= 0.6
+ LAMBDA= 0.0
+ RS= 0.0
+ RD= 0.0
+ CBD= 0.0
+ CBS= 0.0
+ IS= 1.0e-14
+ PB= 0.8
+ CGSO= 0.0
+ CGDO= 0.0
+ CGBO= 0.0
+ RSH= 0.0
+ CJ= 0.0
+ MJ= 0.5
+ CJSW= 0.0
+ MJSW= 0.5
+ JS= 0.0
+ TOX= 1.0e-7
+ NSS= 0.0
+ TPG= 1.0
+ LD= 0.0
+ UO= 600.0
+ KF= 0.0
+ AF= 1.0
+ FC= 0.5

+ TNOM= 27
+)

Multisim Simulation of MOSFET Circuits

.MODEL IDEAL_4TEN__TRANSISTORS_VIRTUAL__1__1
NMOS
+   (
+ LEVEL= 1
+ VTO=   1
+ KP=   25e-6

Note:

the letter "P" in KP does NOT stand for "p-channel"!!!

The "P" stands for "Pri",

KP is the k' parameter in our equation,

Its physical meaning is mu * Cox''

$\mu C_{ox}''$

Its unit is A/V^2.

Use virtual 4 terminal NMOS you can edit model name

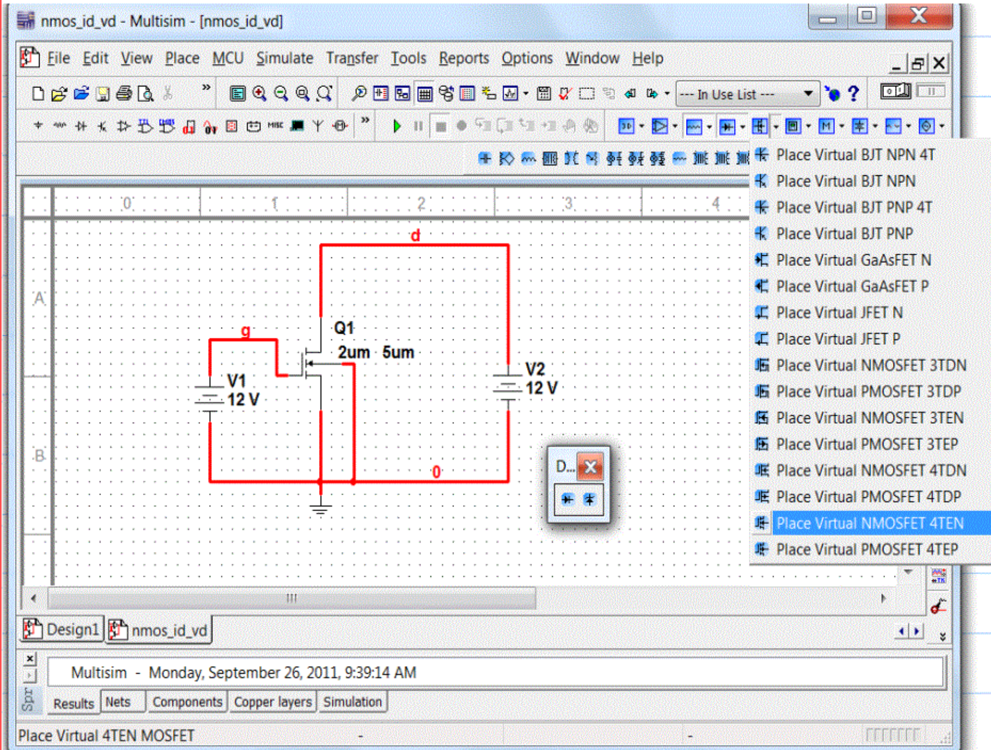
(rename) so that you can have different transistor models in one simulation.

VTO is threshold voltage at zero VSB.
Its unit is Volt.

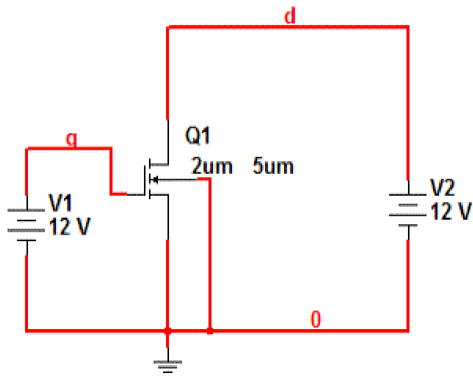
VT depends on substrate bias VSB also, which we will address later.

Simulate NMOS in Multisim

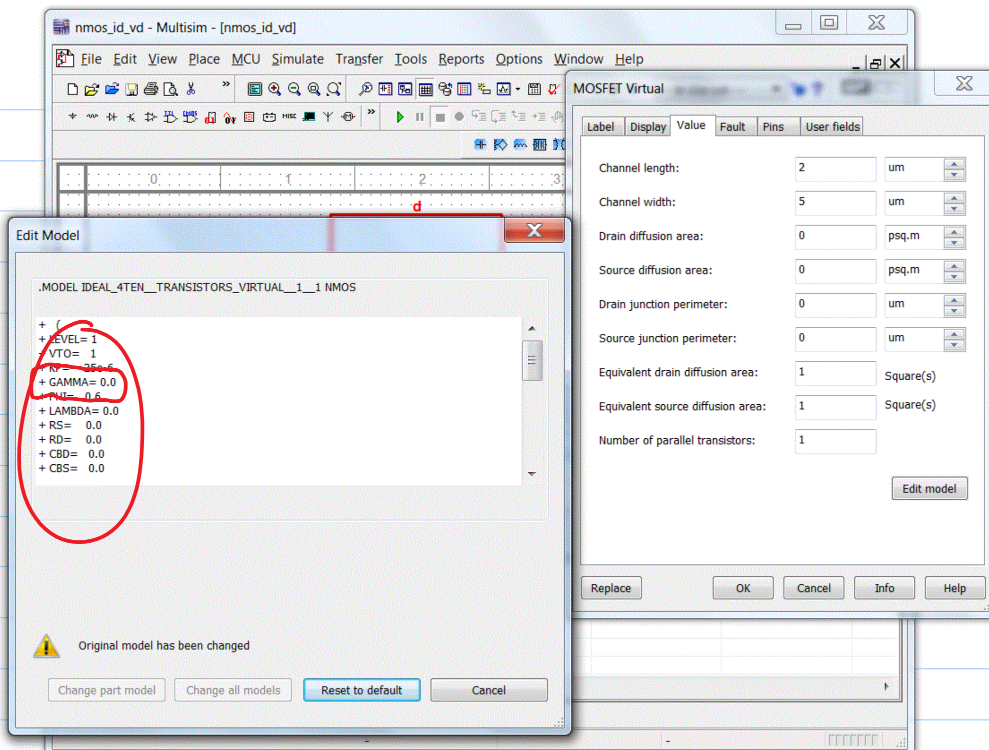
place transistor, wire circuit



double click transistor, specify W, L values,
name g, d nodes as we did for bipolar transistor

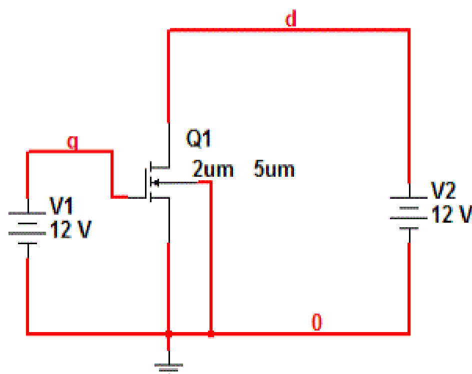


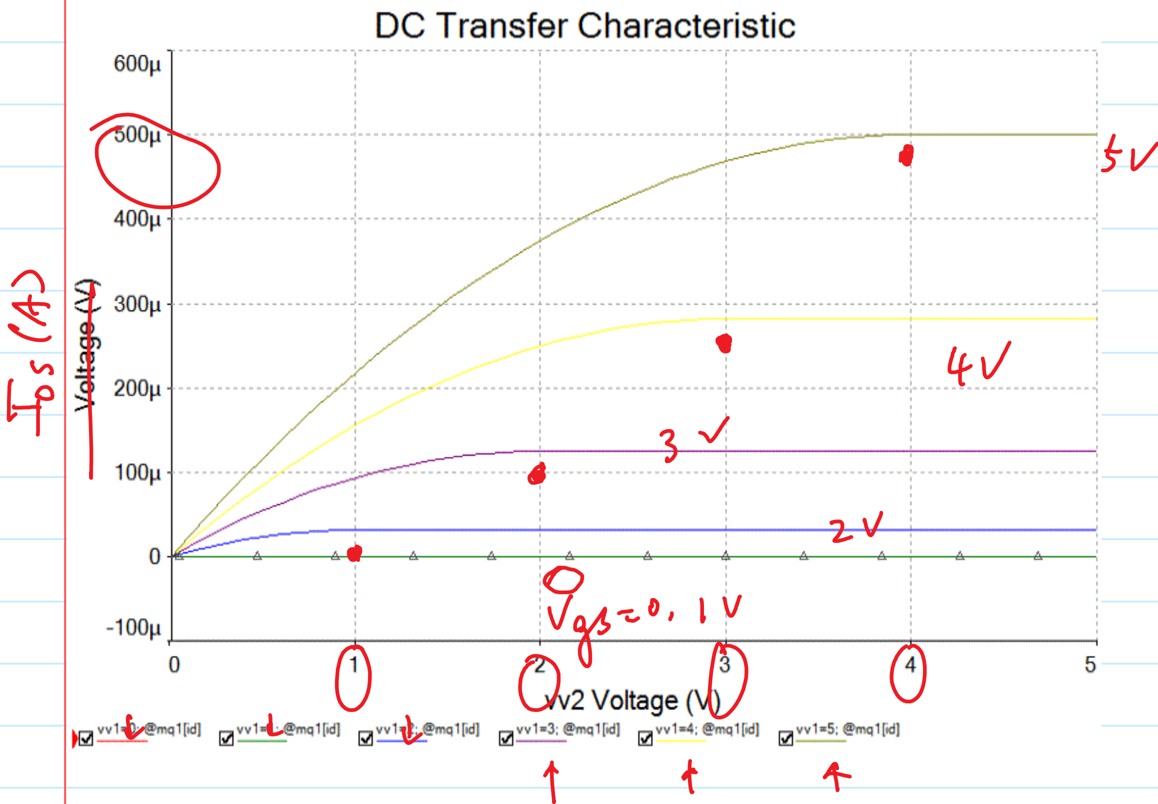
"Edit Model" to edit model parameters



NMOS Ids-Vds (output) Characteristics

Example: simulate Ids-Vds output curves (varying Vgs) for the above transistor in multisim. Can you identify linear and saturation regions on each curve?





Ids-Vds curves for different Vgs

If VGT < 0, device is in cutoff (or off), IDS = 0

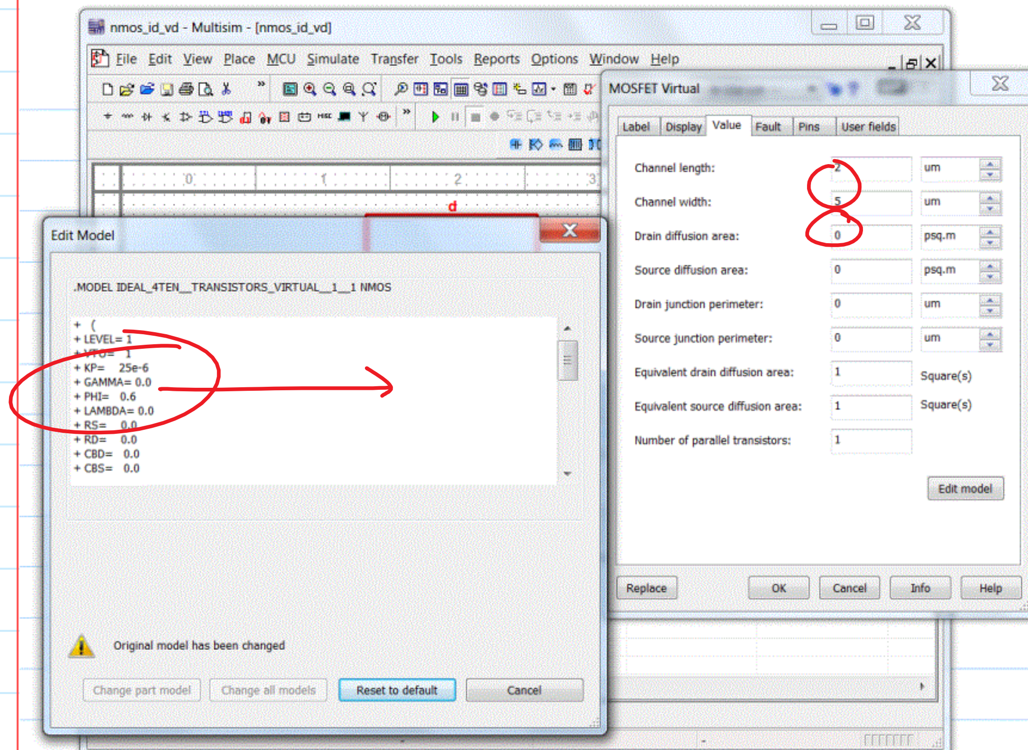
If VGT >0, device is on. Vdsat = VGT

If Vds < Vdsat, Ids = Kn * (VGT - Vds/2) * Vds,

Ids saturates at constant value Idsat, when Vds>Vdsat

Analog amplification is mostly done in Saturation region

Example: compare the simulation above with hand calculation for **Vdsat and Idsat at Vgs=5V**.



$L = 2\,\mu m$

$W = 5\,\mu m$

$$V_{GT} = V_{GS} - V_T = 5 - 1\ V = 4\ V$$

$$V_{dsat} = V_{GT}$$

$L = 2\,\mu m$

$W = 5\,\mu m$

$V_T = 1\ V$

$K' = 25 \times 10^{-6}\ \frac{A}{V^2}$

$= 25\ \mu A / V^2$

$$I_{Dsat} = K_n \cdot \frac{V_{GT}^2}{2} = K_n' \frac{W}{L} \frac{V_{GT}^2}{2}$$

$$V_{DS} \geq V_{DSAT}$$

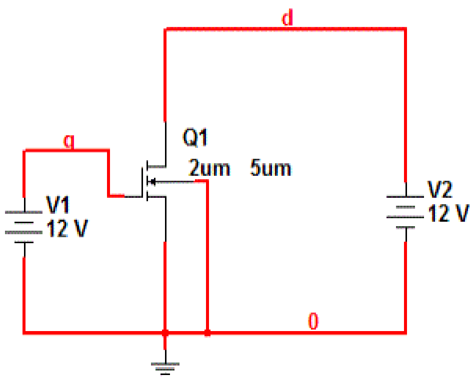
$V_{DSAT} = V_{GT} = V_{GS} - V_{TN}$ $I_{DS} = I_{DSAT}$

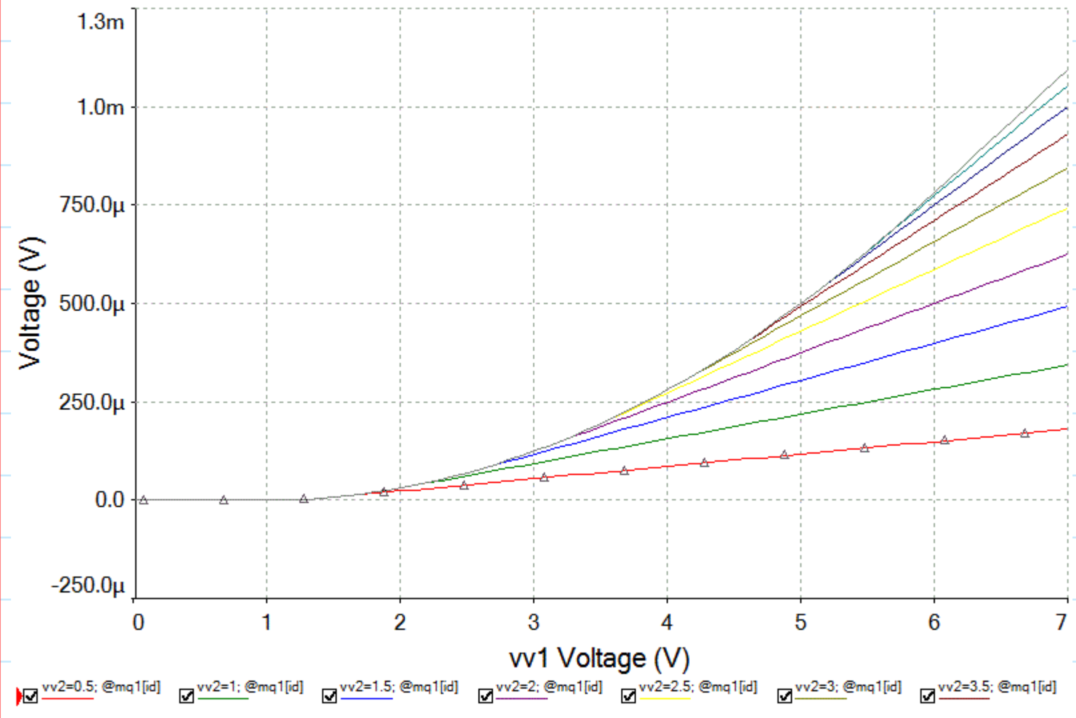
$V_{DSAT} = V_{GS} - V_T$
$= 5V - 1V$
$= 4V.$

$I = \frac{K}{2} \cdot V_{GT}^2$
$= \frac{KP}{2} \cdot \frac{W}{L} \cdot V_{GT}^2$
$= \frac{1}{2} \times 25 \times 10^{-6} \frac{A}{V^2} \cdot \frac{5}{2} \cdot \times (4V)^2$
$= 500 \mu A$

N-MOS Ids-Vgs (transfer) Characteristics

Example: simulate Ids-Vgs curves for various Vds for the above MOSFET. Can you identify the saturation and linear regions on each curve?





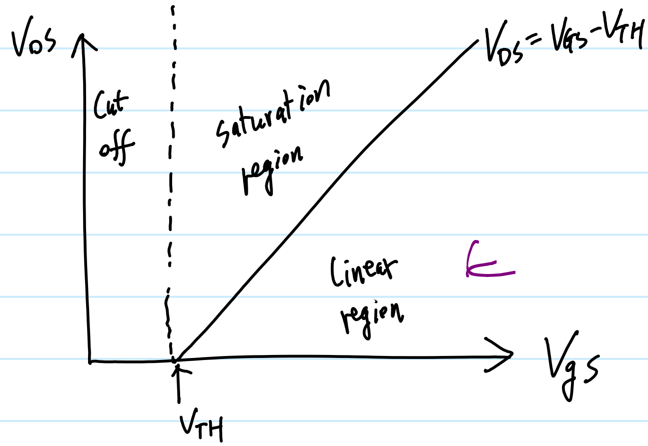
$V_{DS} = 2V$ $V_{TH} = 1V$

$0 < V_{DS} < V_{GS} - V_{TH}$.

linear

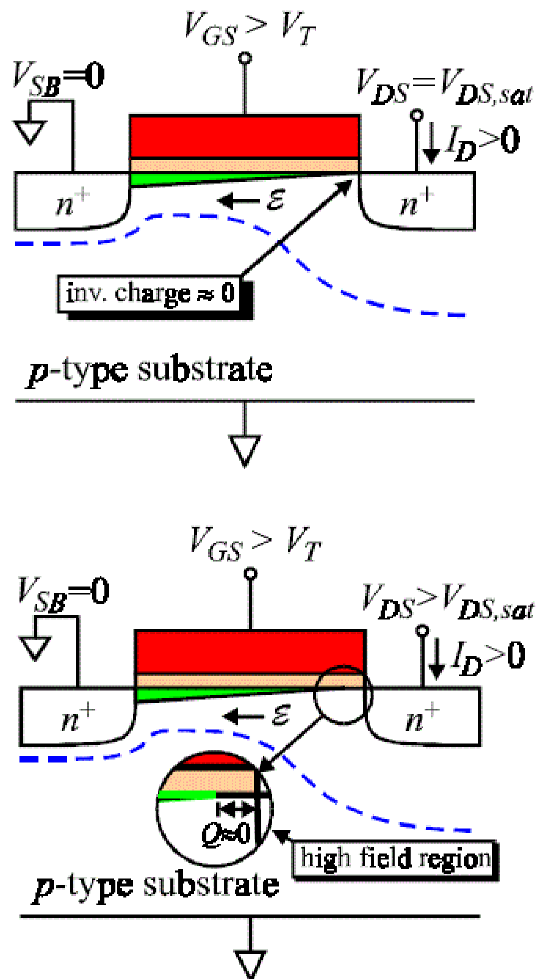
$V_{GS} > V_{DS} + V_{TH}$

$V_{GS} > 3V$ linear



What happens when VDS > VDS,sat ?

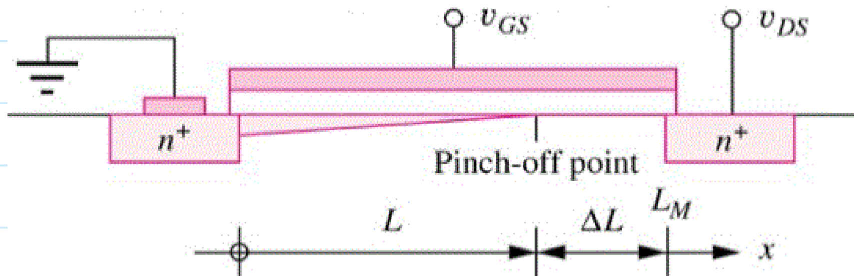
Past pinchoff, further increases in lateral electric field are absorbed by
the creation of a narrow high field region with low carrier density
(Jn=qnµnE, so if n is small E is large)



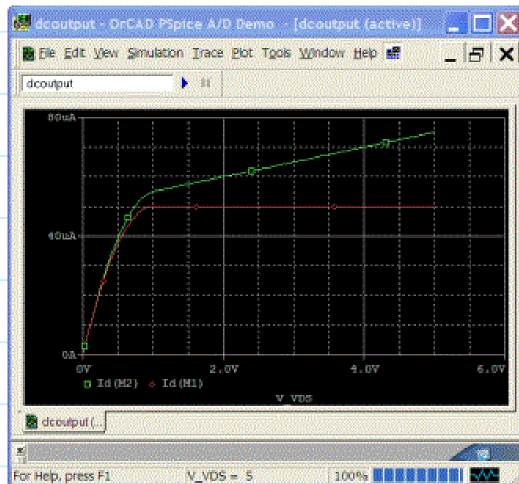
Channel-Length Modulation

As vDS increases above vDSAT, length of depleted channel beyond pinch-off point, DL, increases to support additional voltage and actual L decreases.
This "pinched-off" region is high impedance, and a small

distance can support a large amount of voltage
iD increases slightly with vDS instead of being constant due to reduction of effective electrical channel length (distance overwhich inversion is high)



$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

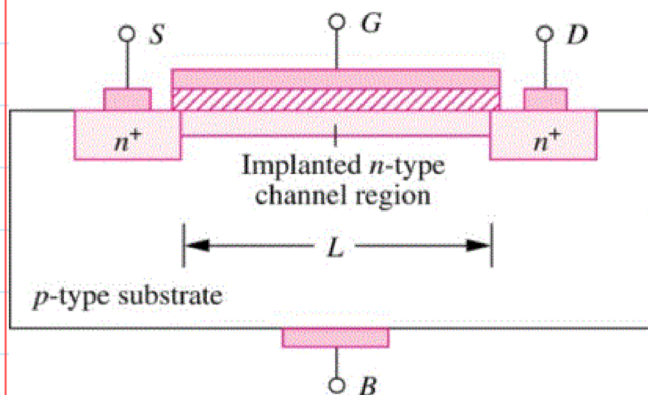


LAMBDA

KP : K_n'

W : L : VTO : V_{TN} for $V_{BS} = 0$

Depletion-Mode MOSFET (VTN<0)
NMOS transistors with
Ion implantation process used to form a built-in n-type channel in device to connect source and drain by a resistive channel
Non-zero drain current for vGS=0, negative vGS required to turn device off.



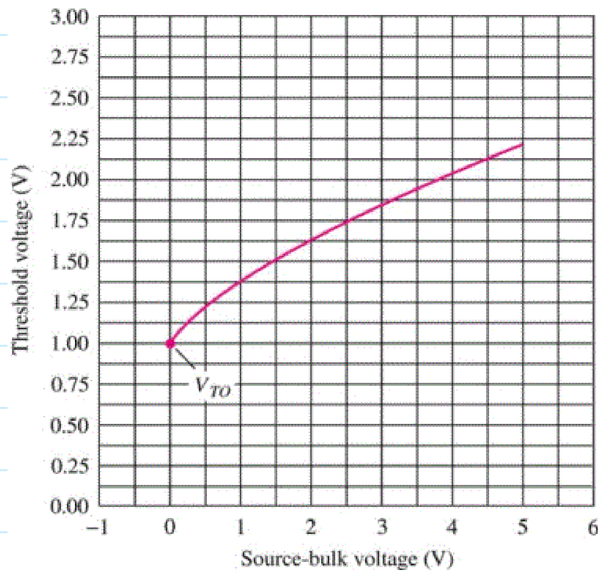
$$\gamma = \frac{\sqrt{2 q \varepsilon_s N_a}}{C''_{ox}}$$

Non-zero vSB changes threshold voltage, causing substrate sensitivity modeled by

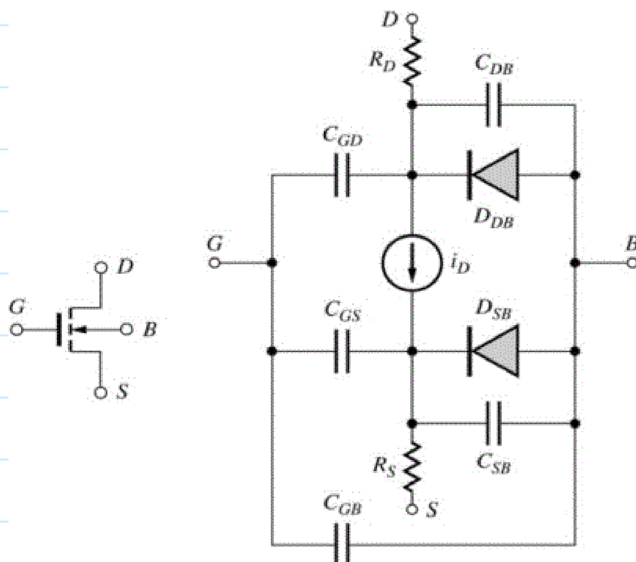
$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

VTO= zero substrate bias for VTN (V)

gamma= body-effect parameter (   )
2phi_F= Fermi potential parameter (V)



Level 1 MOSFET Model in SPICE



Typical default values used by SPICE:

K_n or $K_p = 20\ \mu A/V^2$

$\gamma = 0$

$\lambda = 0$

$V_{TO} = 1$ V

μ_n or $\mu_p = 600$ cm^2/V.s

$2\Phi_F = 0.6$ V

$C_{GDO}=C_{GSO}=C_{GBO}=C_{JSW}= 0$

$T_{ox}= 100$ nm

Transconductance (dIds/dVgs)

Monday, March 12, 2012 4:56 PM

Transconductance of a MOS Device

Transconductance relates the change in drain current to a change in gate-source voltage

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q-pt}$$

Taking the derivative of the expression for the drain current in saturation region,

$$g_m = K_n' \frac{W}{L}(V_{GS} - V_{TN}) = \frac{2I_D}{V_{GS} - V_{TN}}$$

Homework on MOSFET, due Wed, Feb 27 class

Monday, March 12, 2012 5:48 PM

1. 4.25 (a)

2. For a MOSFET with the following process parameters VTO=0.5V, KP=25uA/V^2, W=4um, L=2um.

(a) Using Multisim, simulate IDS versus VDS curves for VGS=0 to 5V in 0.5V step.

Identify the (Vdsat, Idsat) point on each curve with a marker (you can do this by hand on printed plots). VDS range is from 0 to 5V.

Hint: Use the 4 terminal virtual NMOSFET

(b) Calculate by hand the Vdsat and Idsat for VGS=2.5V, compare result with simulation from (a).