ASIC Chip Layout with UofU Cadence Design Kit

References:

- Erik Brunvand, *Digital VHDL Chip Design with Cadence and Synopsys CAD Tools*
- Cadence Virtuoso User Manual

Setup for NCSU/UofU ami06

- .bashrc environment variables

```
# Set up NCSU-CDK and Univ. of Utah Support
export CDK_DIR=/class/ELEC6250/ncsu-cdk-1.6.0.beta
export SYSTEM_CDS_LIB_DIR=/home/nelson/nelsovp
export CDS_NETLISTING_MODE=Analog
# Create alias for Global Foundries BICMOS8HP Digital Kit
export CMOS8HP=/class/ELEC6250/cmos8hp/std_cell/v.20130404
export BICMOS8HP=/class/ELEC6250/IBM_PDK/bicmos8hp/relHP
export TECHDIR=/class/ELEC6250/IBM_PDK/bicmos8hp/relHP/Calibre
```

← Your home directory

BICMOS8HP setup

- From directory /class/ELEC6250/UofUtah
  - Copy cdsinit to your home directory and name it .cdsinit
    (this will load other initialization files)
  - Copy cds.lib.auburn to your home directory or to your project directory
    (or add lines from this file to your current cds.lib file)
    Example on next slide.

cds.lib

- Virtuoso loads **cds.lib** from the directory in which it is invoked
- **cds.lib** in my home directory has the "system library" definitions for the installed libraries (BICMOS8HP, NCSU, UofU, Cadence, etc.)
- **cds.lib** in my project directory references the above and then defines my own project-specific libraries:
  - SOFTINCLUDE /home/nelson/nelsovp/cds.lib
  - DEFINE UofU_tricounter /home/nelson/nelsovp/cadence/Modulo6_UofU/top/UofU_tricounter
  - DEFINE my_new_ami06 /home/nelson/nelsovp/cadence/Modulo6_UofU/top/my_new_ami06
  - DEFINE my_pads /home/nelson/nelsovp/cadence/Modulo6_UofU/top/UofU_Pads

Pads copied from UofU installation

NCSU Cadence Design Kit (CDK)

https://www.eda.ncsu.edu/wiki/NCSU_CDK

- For analog/digital CMOS IC design via the MOSIS IC fabrication service (www.mosis.org)
  - Version ncsu-cdk-1.6.0.beta for Cadence Virtuoso 6.1 and later
- Supports all MOSIS processes based on SCMOS rules
  - ami_06/16, hp_04/06, tsmc_02/03/04
  - GDSII layer maps
  - Diva DRC, LVS support (no PEX)
  - Composer interfaces to HSPICE/Spectre, Verilog
  - Technology-independent libraries for analog & digital parts
    - Transistor models, layouts, etc.
    - But – does <u>not</u> include standard cell layout library
  - MOSIS wirebond pads (AMI 0.6μm, TSMC 0.4 μm, HP 0.6μm)

Installed in /class/ELEC6250/ncsu-cdk-1.6.0.beta

U. of Utah CDK (used in Dr. Brunvand's book)

/class/ELEC6250/UofUtah/

- **UofU_TechLib_ami06** UofU-modified tech library for AMI C5N 0.5 micron CMOS process, in the NCSU CDK framework

  (AMI acquired by ON Semiconductor for $915M in 2008)
- **UofU_Digital_v1_2** Std. Cell library (37 cells, use M1 & M2)
  - UofU_Digital_v1_2.db: compiled library file for Synopsys Design Compiler
  - UofU_Digital_v1_2.lef: abstract layout information file for place and route tools
  - UofU_Digital_v1_2.lib: library characterization file
  - UofU_Digital_v1_2.v: Verilog interface and simulation behavior file
  - UofU_Digital_v1_2_behv.v: Verilog models with timing "specify" blocks
- **UofU_Pads** Pad cells and frames based on the MOSIS-supplied .5μm pads from Tanner, but UofU-modified to pass DRC and LVS
- **UofU_AnalogParts** UofU-modified transistor models that add delay to the switch-level simulation of those devices

UofU_Digital_v1_2 CMOS cell library

Xn = drive strength

- AND3X1: 3-input AND
- AOI21X1, AOI22X1: AND-OR-Invert gates
- BUFX2, BUFX4, BUFX8: non-inverting buffers
- DCBNX1, DCBX1, DCNX1, DCX1: D-type flip flops with active-low clear.

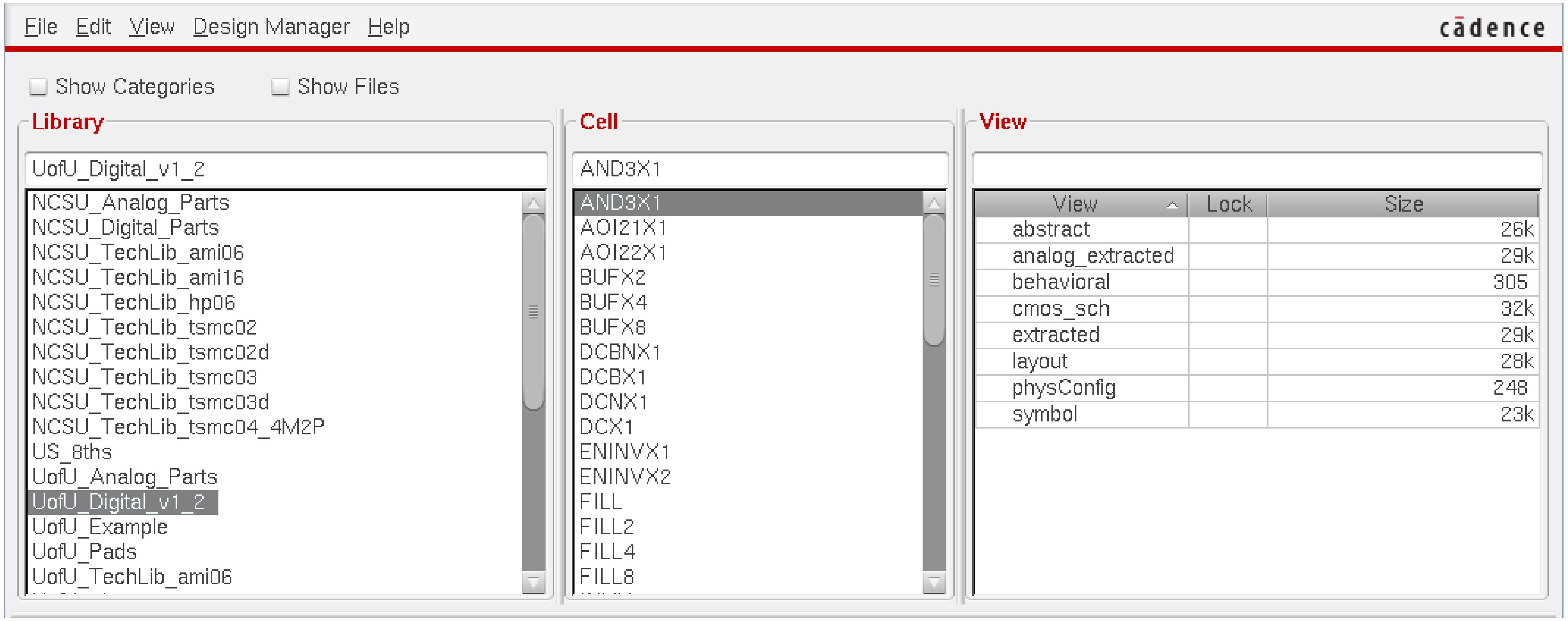
  B means that the device includes both Q and QB outputs.

  N means active-low clock.
- ENINVX1, ENINVX2: enabled (tri-state) inverters
- FILL, FILL2, FILL4, FILL8: filler cells of different widths for filling in std cell rows
- INVX1, INVX16, INVX2, INVX4, INVX8: inverters
- LCNX1, LCX1: level-sensitive (gated) latches with active-low clear.

  N means active-low gate
- MUX2NX1, MUX2X2: 2-way muxes. N means an inverting mux
- NAND2X1, NAND2X2, NAND3X1: NAND gates with 2 and 3 inputs
- NOR2X1, NOR2X2, NOR3X1: NOR gates with 2 and 3 inputs
- OAI21X1 OAI22X1: OR-AND-Invert gates
- TIEHI, TIELO: Cells used to tie inputs high or low
- XNOR2X1: 2-input XNOR
- XOR2X1: 2-input XOR

UofU_Digital_v1_2 cell views

Cells use *UofU_TechLib_ami06* technology library



Library: UofU_Digital_v1_2

- NCSU_Analog_Parts
- NCSU_Digital_Parts
- NCSU_TechLib_ami06
- NCSU_TechLib_ami16
- NCSU_TechLib_hp06
- NCSU_TechLib_tsmc02
- NCSU_TechLib_tsmc02d
- NCSU_TechLib_tsmc03
- NCSU_TechLib_tsmc03d
- NCSU_TechLib_tsmc04_4M2P
- US_8ths
- UofU_Analog_Parts
- UofU_Digital_v1_2
- UofU_Example
- UofU_Pads
- UofU_TechLib_ami06

Cell: AND3X1

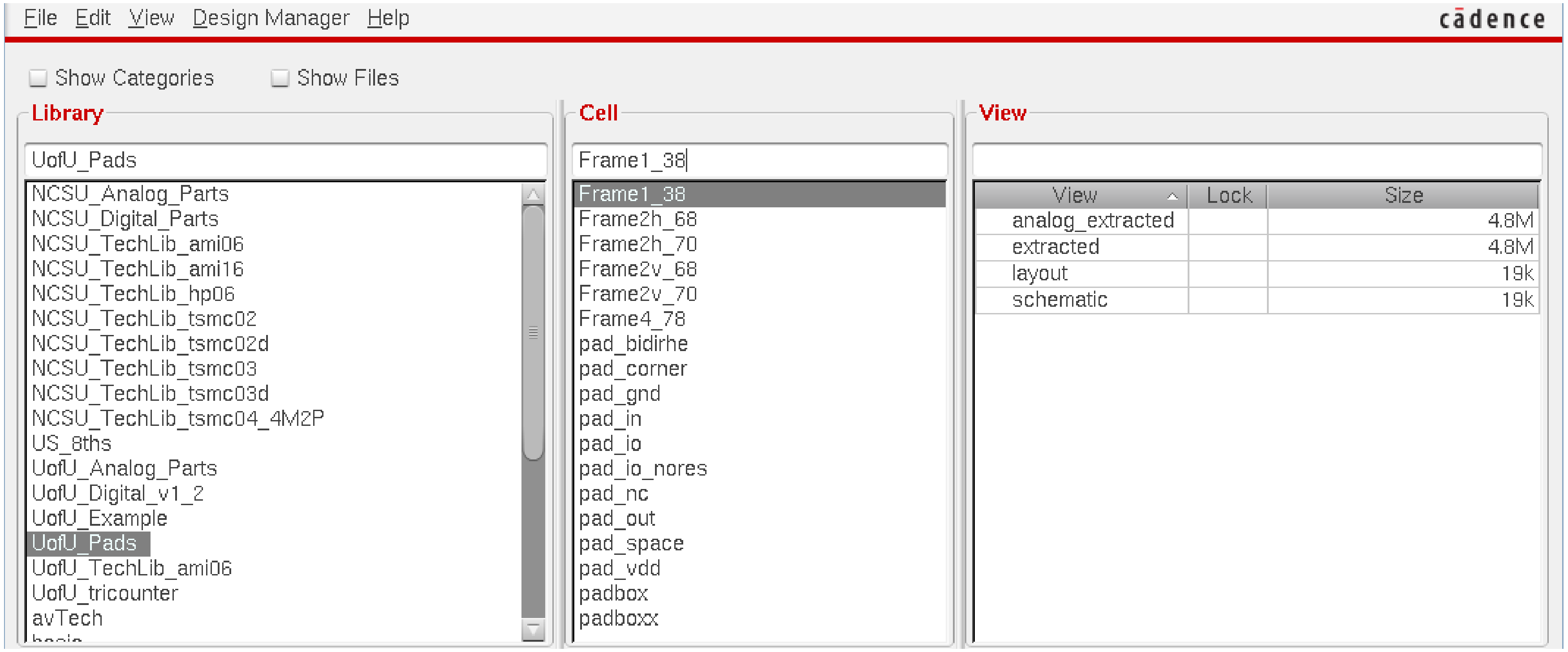
- AND3X1
- AOI21X1
- AOI22X1
- BUFX2
- BUFX4
- BUFX8
- DCBNX1
- DCBX1
- DCNX1
- DCX1
- ENINVX1
- ENINVX2
- FILL
- FILL2
- FILL4
- FILL8

View	Lock	Size
abstract		26k
analog_extracted		29k
behavioral		305
cmos_sch		32k
extracted		29k
layout		28k
physConfig		248
symbol		23k

- **cmos_sch** – schematic of transistors from UofU_Analog_Parts library
- **behavioral** - Verilog with "specify" blocks for SDF simulation
- **layout** – full cell layout
- **symbol** – to use in gate-level schematics
- **extracted** – extracted from layout for LVS verification

UofU_Pads

Based on MOSIS-supplied .5µm pads from Tanner



Library: UofU_Pads

NCSU_Analog_Parts
NCSU_Digital_Parts
NCSU_TechLib_ami06
NCSU_TechLib_ami16
NCSU_TechLib_hp06
NCSU_TechLib_tsmc02
NCSU_TechLib_tsmc02d
NCSU_TechLib_tsmc03
NCSU_TechLib_tsmc03d
NCSU_TechLib_tsmc04_4M2P
US_8ths
UofU_Analog_Parts
UofU_Digital_v1_2
UofU_Example
UofU_Pads
UofU_TechLib_ami06
UofU_tricounter
avTech

Cell: Frame1_38

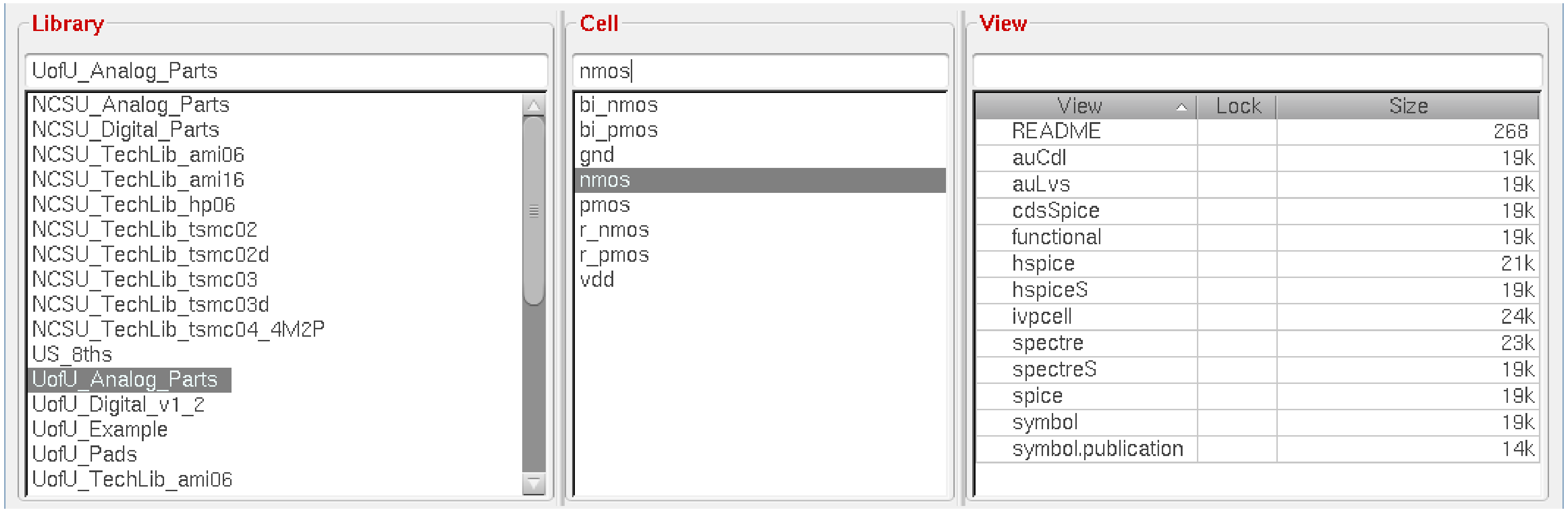
Frame1_38
Frame2h_68
Frame2h_70
Frame2v_68
Frame2v_70
Frame4_78
pad_bidirhe
pad_corner
pad_gnd
pad_in
pad_io
pad_io_nores
pad_nc
pad_out
pad_space
pad_vdd
padbox
padboxx

View	Lock	Size
analog_extracted		4.8M
extracted		4.8M
layout		19k
schematic		19k

- Frame1_38 for MOSIS "TinyChip" (38 signal pins, 2 power/ground pins)
  - Layout and schematic views
  - Edit properties to change pad type within the frame
- Power/ground: pad_vdd, pad_gnd
- Signal: pad_in, pad_out, pad_io
- No connect: pad_nc
- Corner: pad_corner

UofU_Analog_Parts

Based on NCSU_Analog_Parts



Library: UofU_Analog_Parts

- NCSU_Analog_Parts
- NCSU_Digital_Parts
- NCSU_TechLib_ami06
- NCSU_TechLib_ami16
- NCSU_TechLib_hp06
- NCSU_TechLib_tsmc02
- NCSU_TechLib_tsmc02d
- NCSU_TechLib_tsmc03
- NCSU_TechLib_tsmc03d
- NCSU_TechLib_tsmc04_4M2P
- US_8ths
- UofU_Analog_Parts
- UofU_Digital_v1_2
- UofU_Example
- UofU_Pads
- UofU_TechLib_ami06

Cell: nmos

- bi_nmos
- bi_pmos
- gnd
- nmos
- pmos
- r_nmos
- r_pmos
- vdd

View	Lock	Size
README		268
auCdl		19k
auLvs		19k
cdsSpice		19k
functional		19k
hspice		21k
hspiceS		19k
ivpcell		24k
spectre		23k
spectreS		19k
spice		19k
symbol		19k
symbol.publication		14k

- nmos/pmos 3-terminal (bulk to gnd!/vdd!)
- bi_nmos/bi_pmos bidirectional device
- r_nmos/r_pmos weak/resistive transistors
- vdd/gnd

BICMOS8HP/UofU differences

- Synthesis with **Synopsys Design Compiler**
  - Setup file: .synopsys_dc.setup
    - Path to library: /class/ELEC6250/UofUtah
    - Target library: UofU_Digital_v1_2.db
  - Synthesis script references to specific library cells
    - Example: myInputBuf (cell driving inputs)

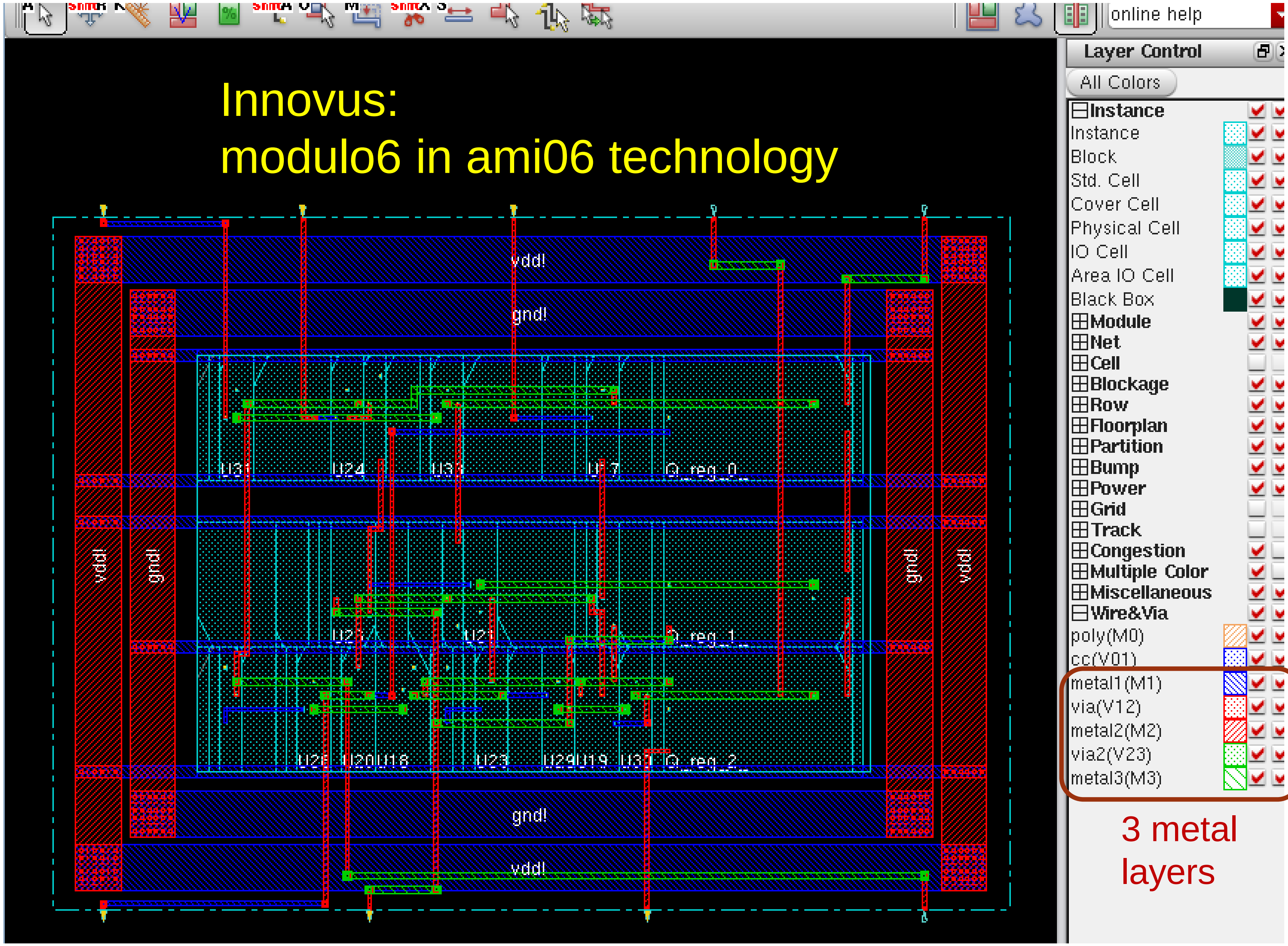
Example: Synthesized Modulo-6 counter netlist

BICMOS8HP/UofU differences

- Block layout with **Innovus**
  - Technology: 500 nm feature size (BICMOS8HP is 130 nm)
  - Wires/spacing may have to be larger
  - Special library cells (filler, clock buffer, etc.)
  - LEF file: UofU_Digital_v1_2.lef
  - Power: vdd!   Ground: gnd!
  - Timing library: UofU_Digital_v1_2.lib (no capacitance table)
  - I/O pins and routing with only 3 metal layers: M1 M2 M3
  - Power planning nets: vdd! gnd!
  - See later slide for exporting layout to Virtuoso

Example: Modulo-6 counter layout (next slide)

Innovus:
modulo6 in ami06 technology

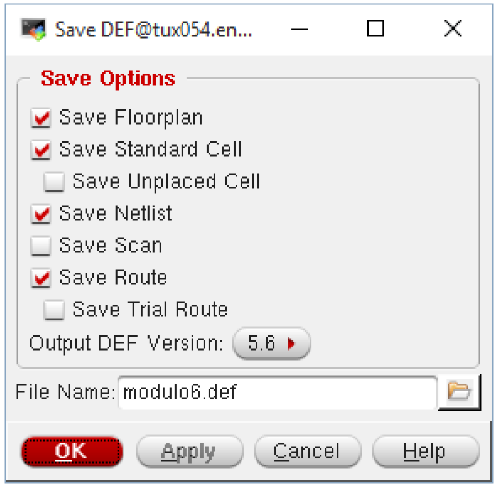


3 metal layers

Innovus: save cell for importing into Virtuoso

- **Export DEF** (Design Exchange Format) file:
  - Menu: File > Save > DEF
  - Command:

```
global dbgLefDefOutVersion
set dbgLefDefOutVersion 5.6
defOut -floorplan -netlist -routing $BASENAME.def
```


Save DEF@tux054.en...

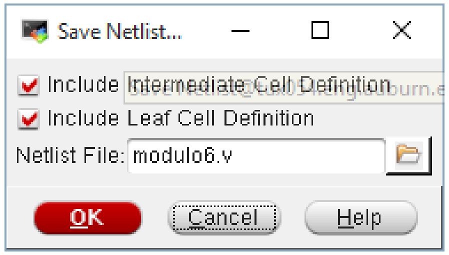
Save Options

- [✓] Save Floorplan
- [✓] Save Standard Cell
- [ ] Save Unplaced Cell
- [✓] Save Netlist
- [ ] Save Scan
- [✓] Save Route
- [ ] Save Trial Route

Output DEF Version: 5.6

File Name: modulo6.def

- **Export Verilog** structural netlist
  - Menu: File > Save > Netlist


Save Netlist...

- [✓] Include Intermediate Cell Definition
- [✓] Include Leaf Cell Definition

Netlist File: modulo6.v

  - Command:

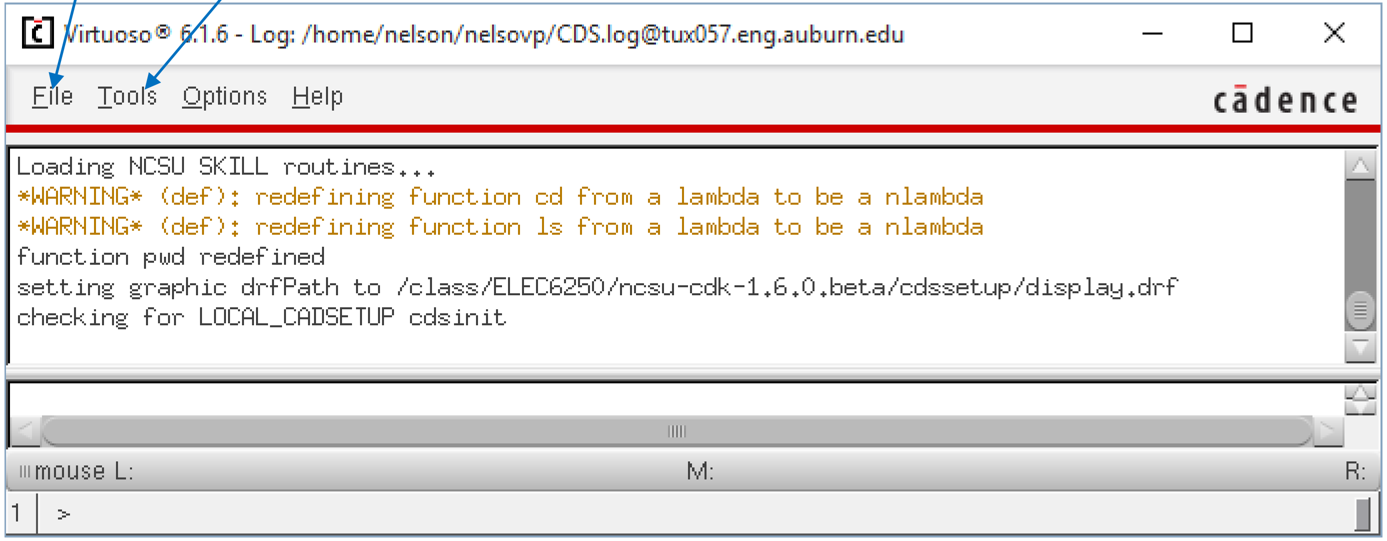
```
saveNetlist -phys -includePowerGround -excludeLeafCell ${BASENAME}_soc.v
```

Virtuoso CIW (Command Interpreter Window)

Cadence libraries and tools are accessed from the CIW

Import/Export designs

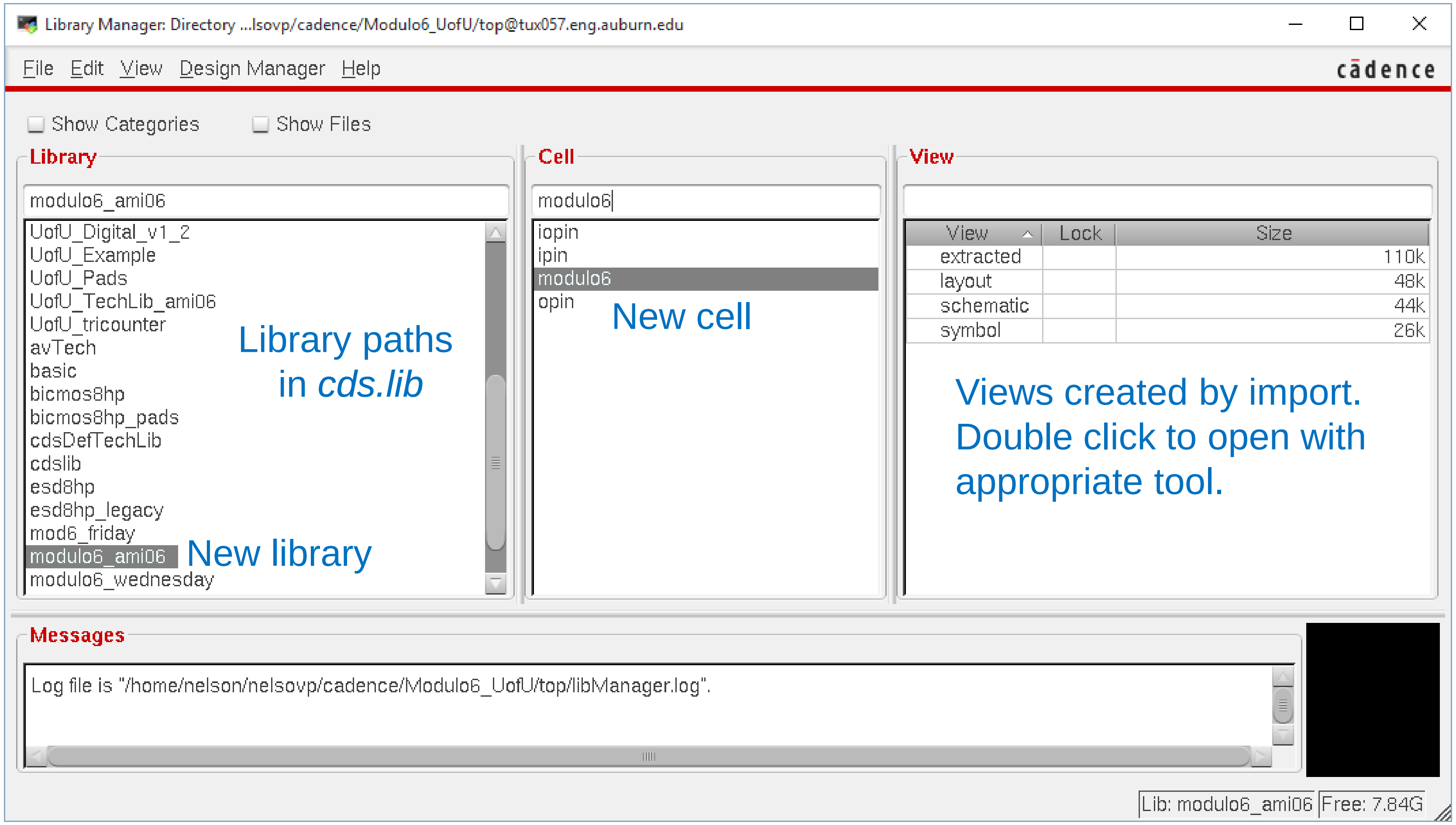
Access libraries



Virtuoso® 6.1.6 - Log: /home/nelson/nelsovp/CDS.log@tux057.eng.auburn.edu
File
Tools
Options
Help
cādence
mouse L:
M:
R:
1
>

```
Loading NCSU SKILL routines...
*WARNING* (def): redefining function cd from a lambda to be a nlambda
*WARNING* (def): redefining function ls from a lambda to be a nlambda
function pwd redefined
setting graphic drfPath to /class/ELEC6250/ncsu-cdk-1.6.0.beta/cdssetup/display.drf
checking for LOCAL_CADSETUP cdsinit
```

Library Manager


Library Manager: Directory ...lsovp/cadence/Modulo6_UofU/top@tux057.eng.auburn.edu
File Edit View Design Manager Help
cādence
Show Categories
Show Files
Library
Cell
View
Messages

Library	Cell
modulo6_ami06	modulo6
UofU_Digital_v1_2	iopin
UofU_Example	ipin
UofU_Pads	modulo6
UofU_TechLib_ami06	opin
UofU_tricounter	
avTech	
basic	
bicmos8hp	
bicmos8hp_pads	
cdsDefTechLib	
cdslib	
esd8hp	
esd8hp_legacy	
mod6_friday	
modulo6_ami06	
modulo6_wednesday	

View	Lock	Size
extracted		110k
layout		48k
schematic		44k
symbol		26k

```
Log file is "/home/nelson/nelsovp/cadence/Modulo6_UofU/top/libManager.log".
```

Lib: modulo6_ami06 Free: 7.84G

Library paths in *cds.lib*

New library

New cell

Views created by import. Double click to open with appropriate tool.

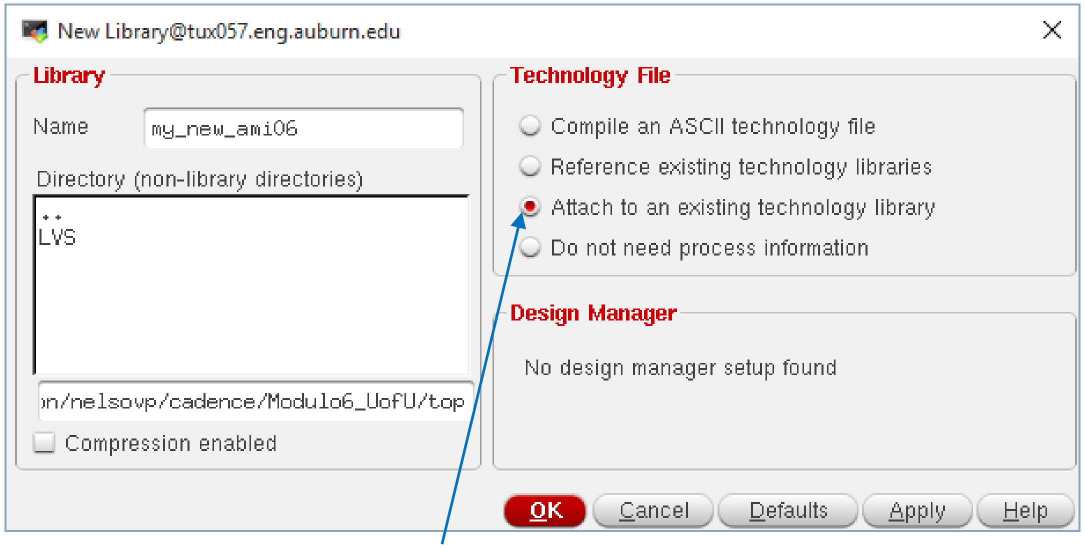
Import digital block into Virtuoso

- Create a new Cadence library for the cell
  - Attach technology library UofU_TechLib_ami06
- Import DEF layout information into Virtuoso:
  - Innovus saved: mydesign.def
  - Import into a the new Cadence library
    - File > Import > DEF
  - Results in cell "layout" view
- Import circuit netlist into Virtuoso:
  - Gate-level netlist saved by Innovus: mydesign.v
  - Import netlist into a Cadence Library
    - File > Import > Verilog
  - Results in cell "schematic" and "symbol" views

In Virtuoso CIW:
File > New > Library

My library name

Directory for library files



New Library@tux057.eng.auburn.edu

Library

Name: my_new_ami06

Directory (non-library directories)

```
..
LVS
```

on/nelsovp/cadence/Modulo6_UofU/top

[ ] Compression enabled

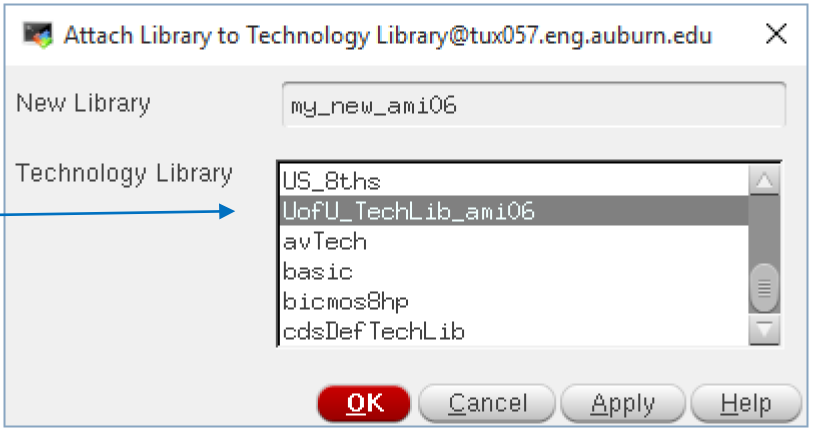
Technology File

- ○ Compile an ASCII technology file
- ○ Reference existing technology libraries
- ● Attach to an existing technology library
- ○ Do not need process information

Design Manager

No design manager setup found

Attach to an existing library



Attach Library to Technology Library@tux057.eng.auburn.edu

New Library: my_new_ami06

Technology Library:

```
US_8ths
UofU_TechLib_ami06
avTech
basic
bicmos8hp
cdsDefTechLib
```

Select UofU_TechLib_ami06

In Virtuoso CIW:
File > Import > DEF

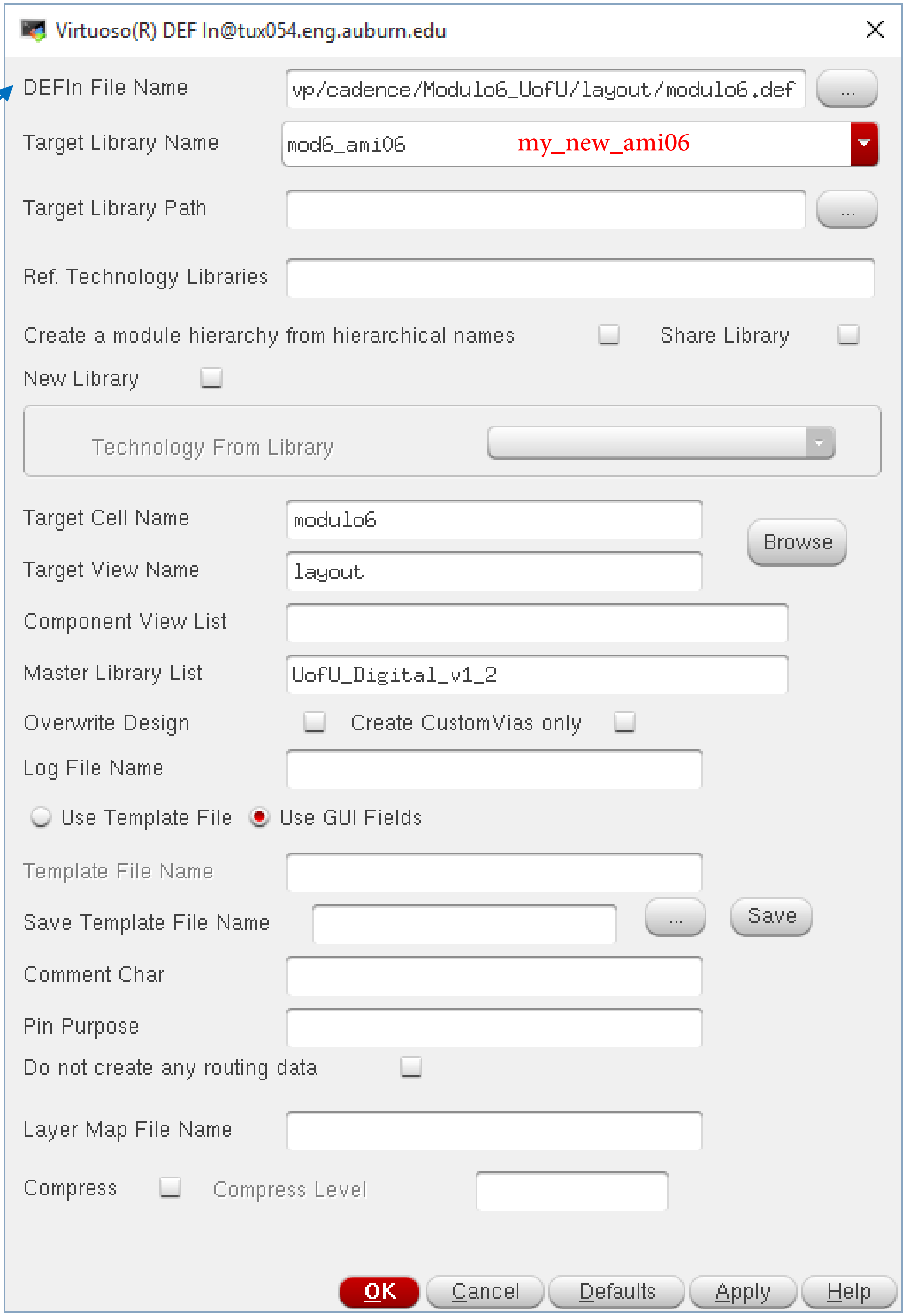
DEF file from Innovus

My library for this cell

Name of top design cell

Cell view type

Technology library
(Contains std. cells & .lib/.lef/.v files)



Virtuoso(R) DEF In@tux054.eng.auburn.edu

DEFIn File Name	vp/cadence/Modulo6_UofU/layout/modulo6.def
Target Library Name	mod6_ami06 my_new_ami06
Target Library Path	
Ref. Technology Libraries	
Create a module hierarchy from hierarchical names	☐
Share Library	☐
New Library	☐
Technology From Library	
Target Cell Name	modulo6
Target View Name	layout
Component View List	
Master Library List	UofU_Digital_v1_2
Overwrite Design	☐
Create CustomVias only	☐
Log File Name	
Use Template File [✓ Use GUI Fields]	
Template File Name	
Save Template File Name	
Comment Char	
Pin Purpose	
Do not create any routing data	☐
Layer Map File Name	
Compress	☐
Compress Level	

In Virtuoso CIW:
File > Import > Verilog

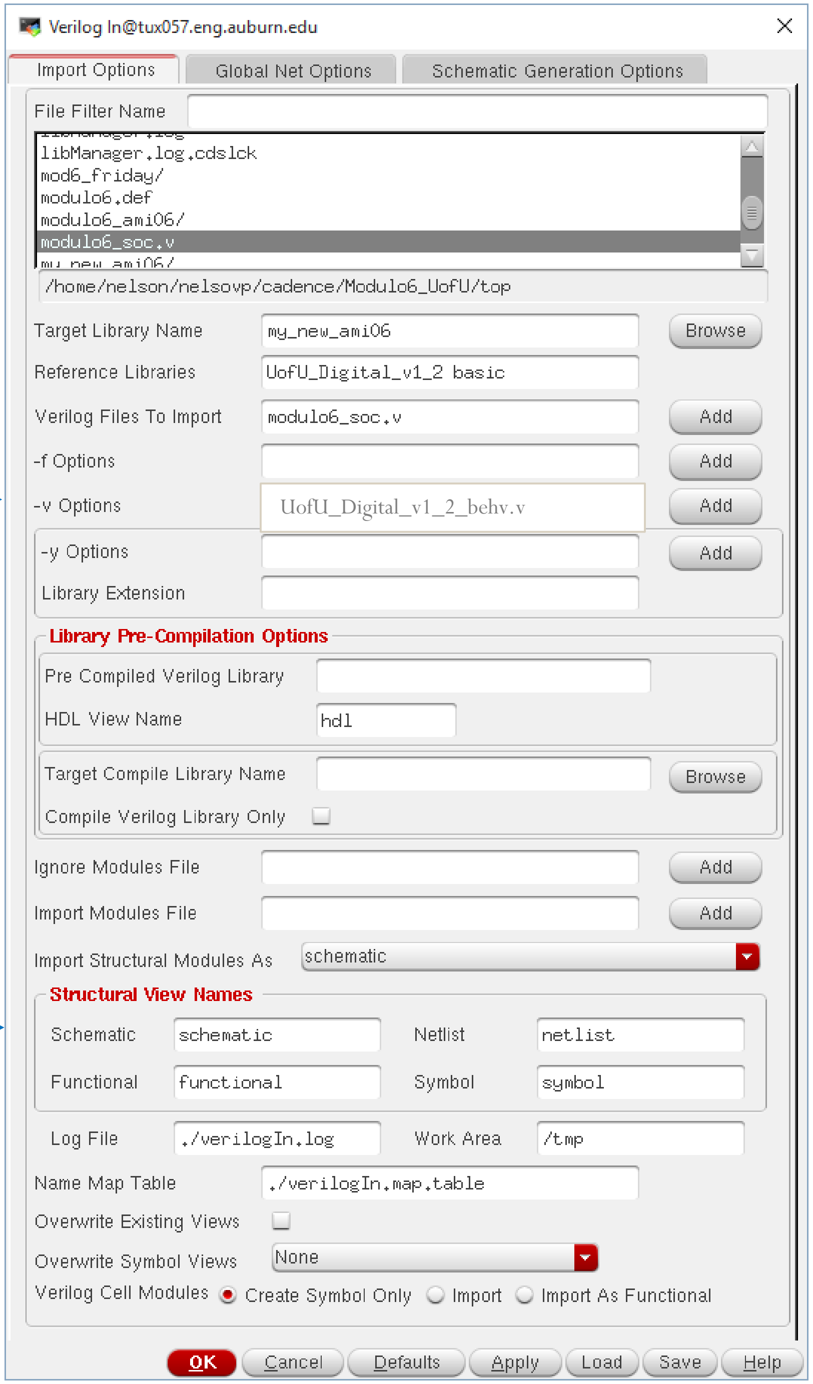
My library for this cell

Reference tech libraries

Verilog file(s)

Verilog models of the standard cells (copy to your directory)

Create schematic and symbol views



Verilog In@tux057.eng.auburn.edu

Import Options | Global Net Options | Schematic Generation Options

```
libManager.log.cdslck
mod6_friday/
modulo6.def
modulo6_ami06/
modulo6_soc.v
my_new_ami06/
/home/nelson/nelsovp/cadence/Modulo6_UofU/top
```

File Filter Name	
Target Library Name	my_new_ami06
Reference Libraries	UofU_Digital_v1_2 basic
Verilog Files To Import	modulo6_soc.v
-f Options	
-v Options	UofU_Digital_v1_2_behv.v
-y Options	
Library Extension	

Library Pre-Compilation Options

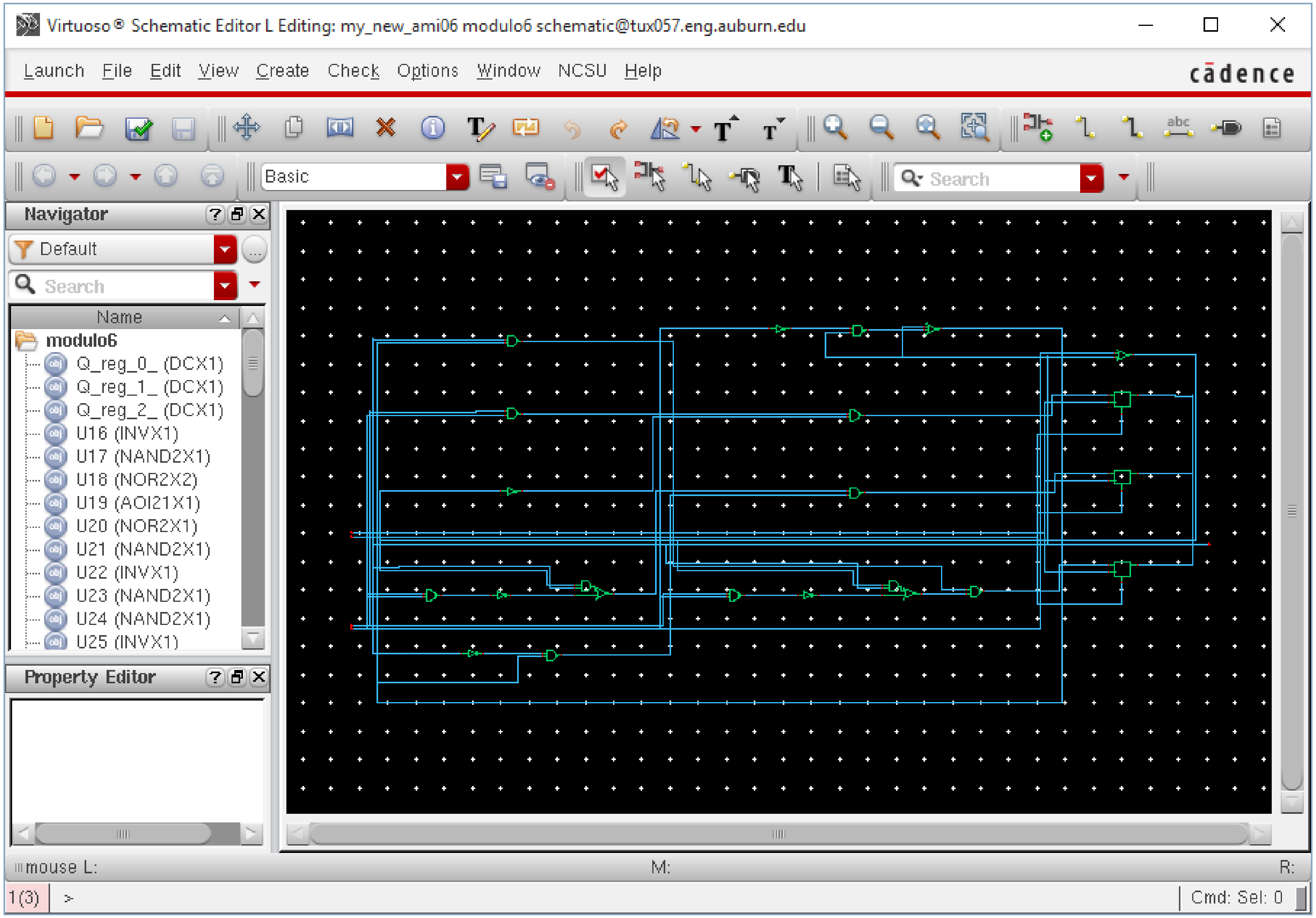
Pre Compiled Verilog Library	
HDL View Name	hdl
Target Compile Library Name	
Compile Verilog Library Only	☐
Ignore Modules File	
Import Modules File	
Import Structural Modules As	schematic

Structural View Names

Schematic	schematic	Netlist	netlist
Functional	functional	Symbol	symbol
Log File	./verilogIn.log	Work Area	/tmp

Name Map Table	./verilogIn.map.table
Overwrite Existing Views	☐
Overwrite Symbol Views	None
Verilog Cell Modules	[✓ Create Symbol Only] Import Import As Functional

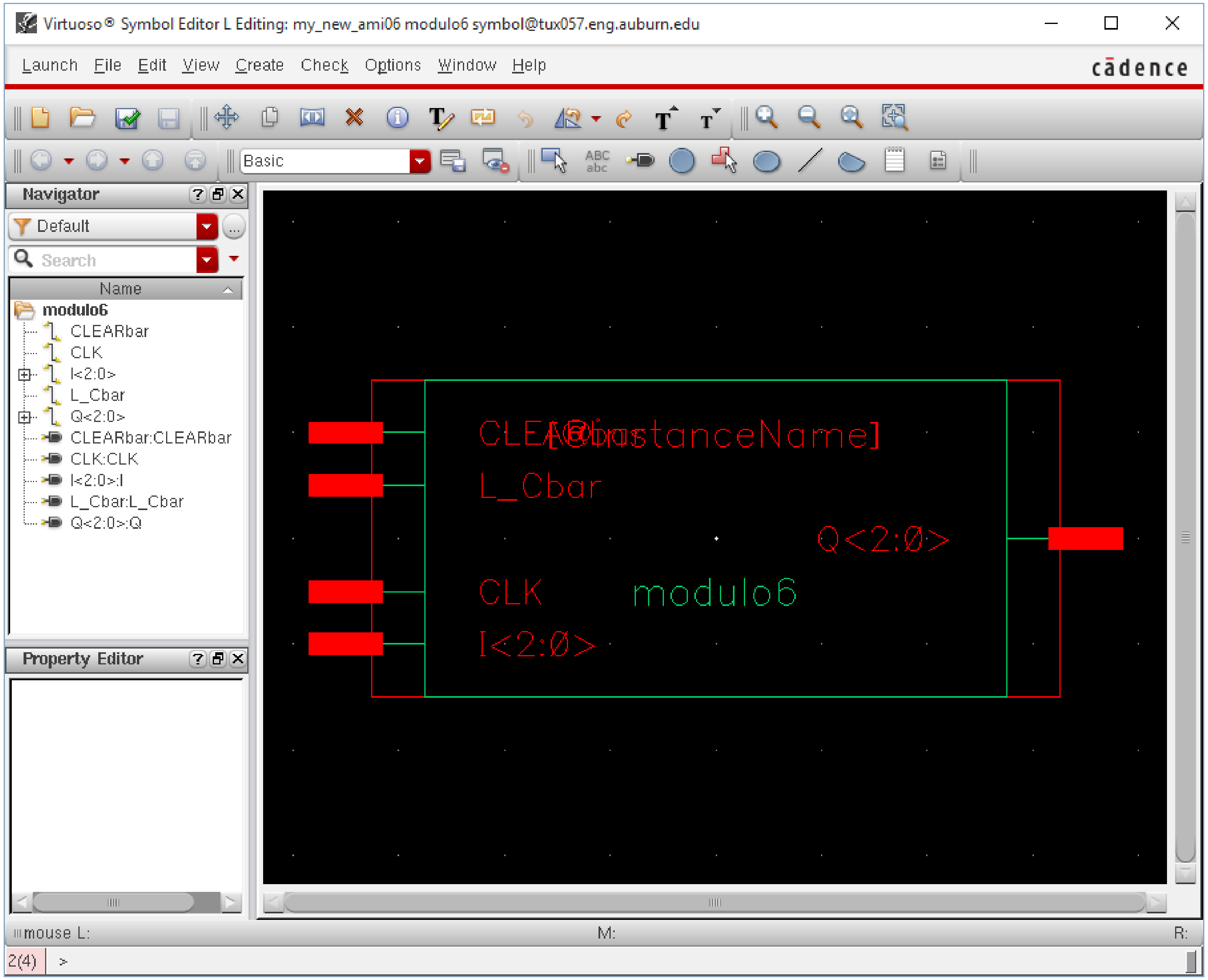
Schematic view of "modulo6"



Virtuoso® Schematic Editor L Editing: my_new_ami06 modulo6 schematic@tux057.eng.auburn.edu

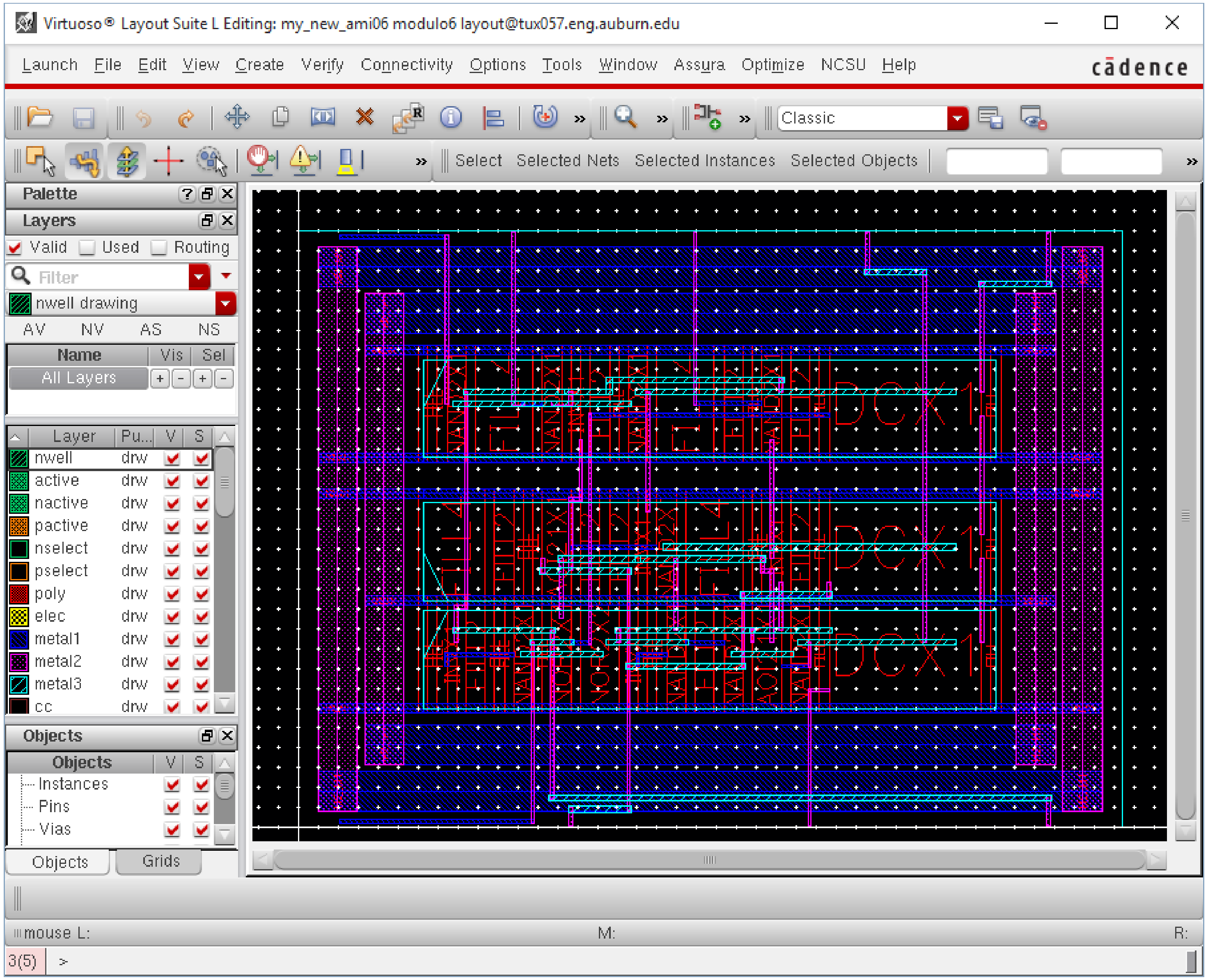
modulo6
- Q_reg_0_ (DCX1)
- Q_reg_1_ (DCX1)
- Q_reg_2_ (DCX1)
- U16 (INVX1)
- U17 (NAND2X1)
- U18 (NOR2X2)
- U19 (AOI21X1)
- U20 (NOR2X1)
- U21 (NAND2X1)
- U22 (INVX1)
- U23 (NAND2X1)
- U24 (NAND2X1)
- U25 (INVX1)

Symbol view of “modulo6”



Layout view of "modulo6"

Abstract view- no cell layout details



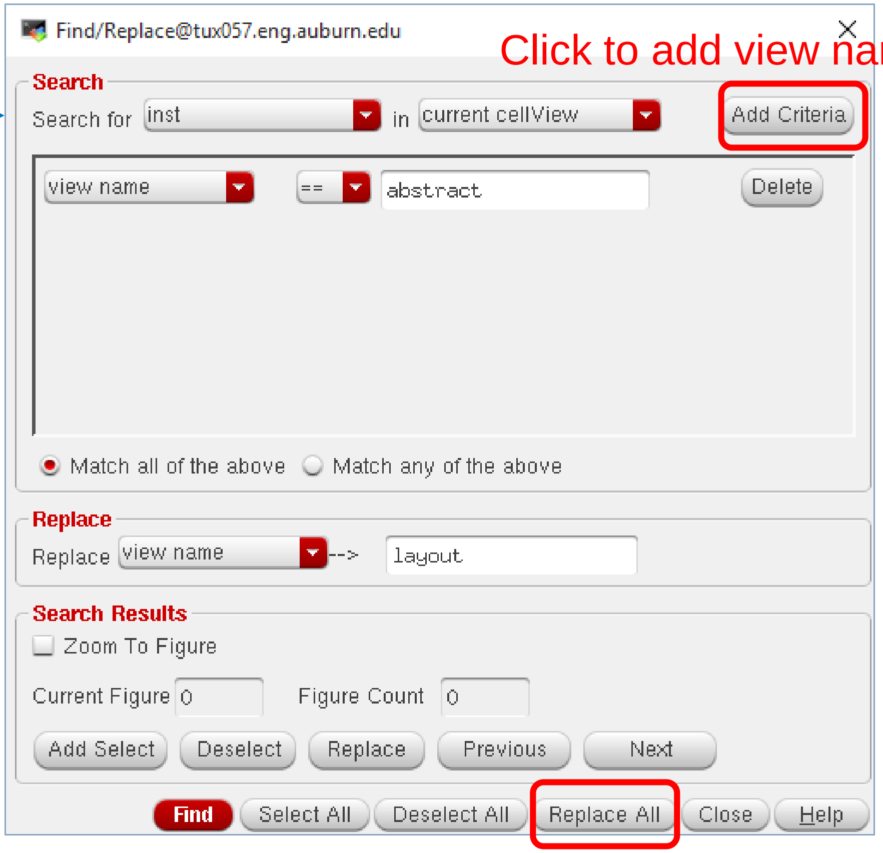
Verify the layout (DRC-Extract-LVS)

- First - change cellviews of instances from abstract to layout
  - Tools > Find/Replace

Instances (inst)

Change view name **from abstract**

to layout



Find/Replace@tux057.eng.auburn.edu

Search

Search for: inst in: current cellView

view name == abstract

[✓ Match all of the above] Match any of the above

Replace

Replace: view name --> layout

Search Results

Zoom To Figure: ☐

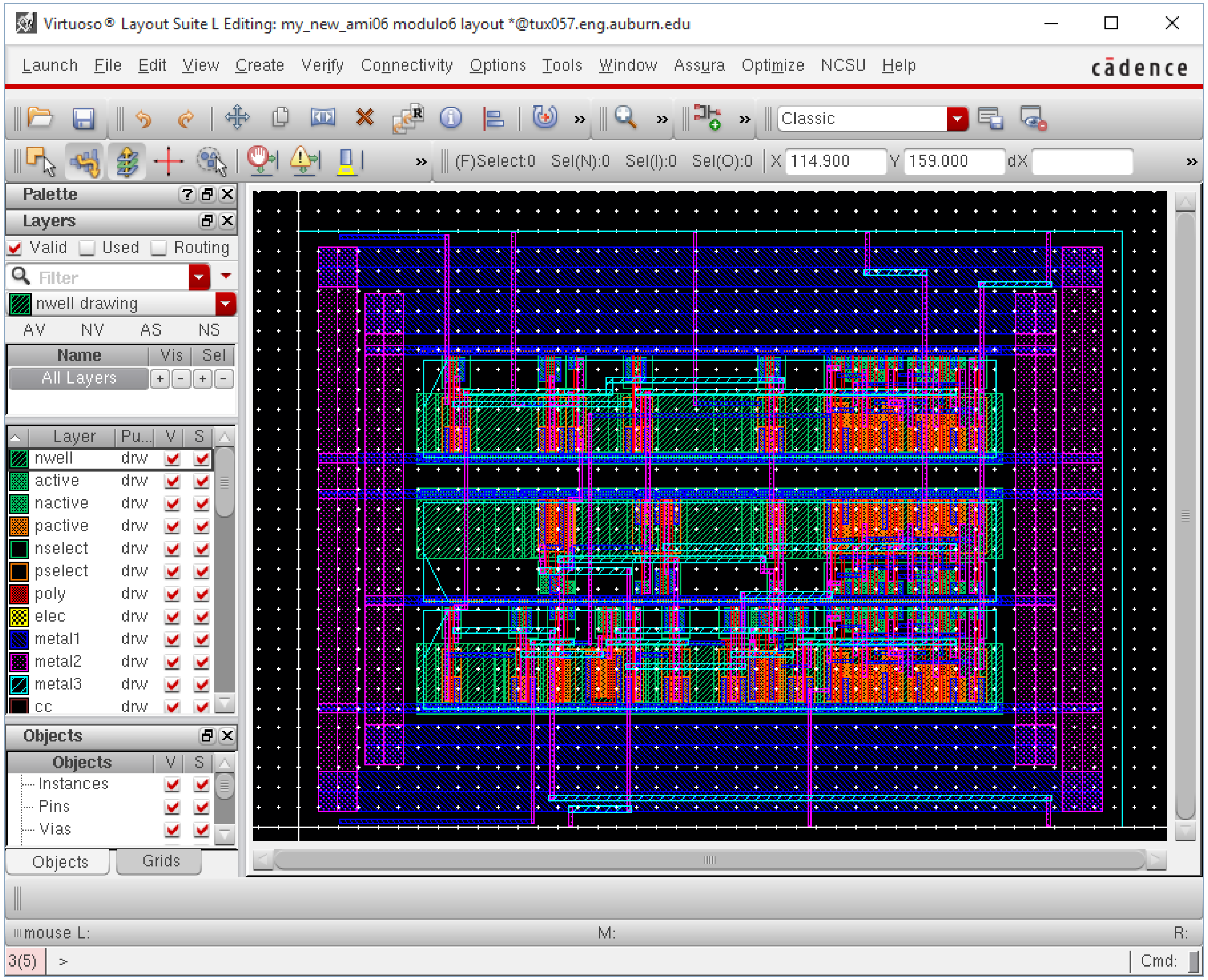
Current Figure: 0 Figure Count: 0

Click to add view name

Replace all

Layout view of "modulo6"

Layout details now shown



Virtuoso® Layout Suite L Editing: my_new_ami06 modulo6 layout *@tux057.eng.auburn.edu

Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize NCSU Help
cādence
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 114.900 Y 159.000 dX
Palette
Layers
Valid Used Routing
Filter
nwell drawing
AV NV AS NS
Name Vis Sel
All Layers
Objects
Grids
mouse L: M: R:
3(5) > Cmd:

Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓

Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

To see all layers:

Options>Display

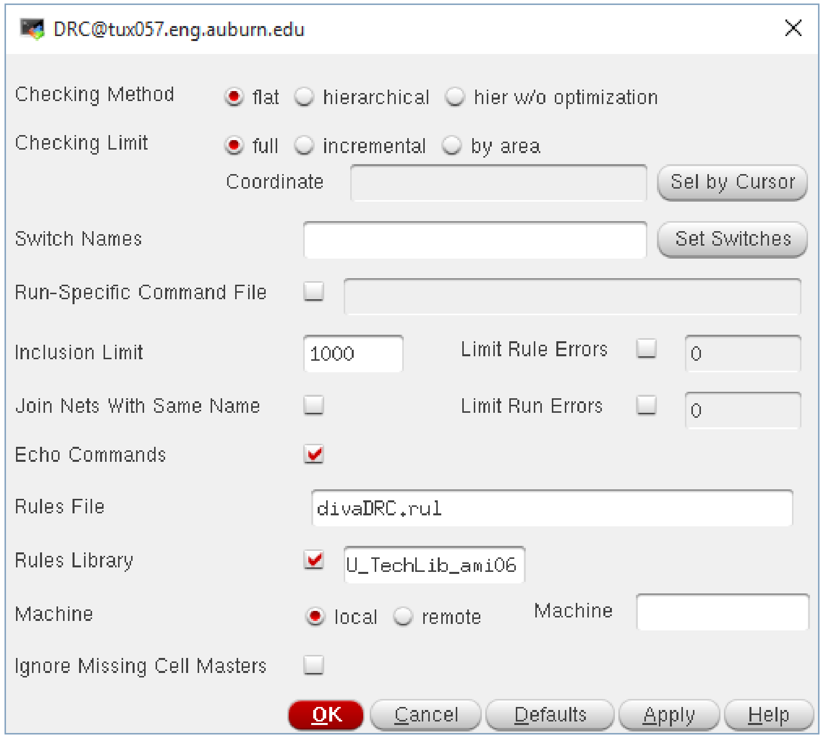
Display levels
- Start 0
- Stop 30

Design rule check to ensure correct layout

Verify > DRC

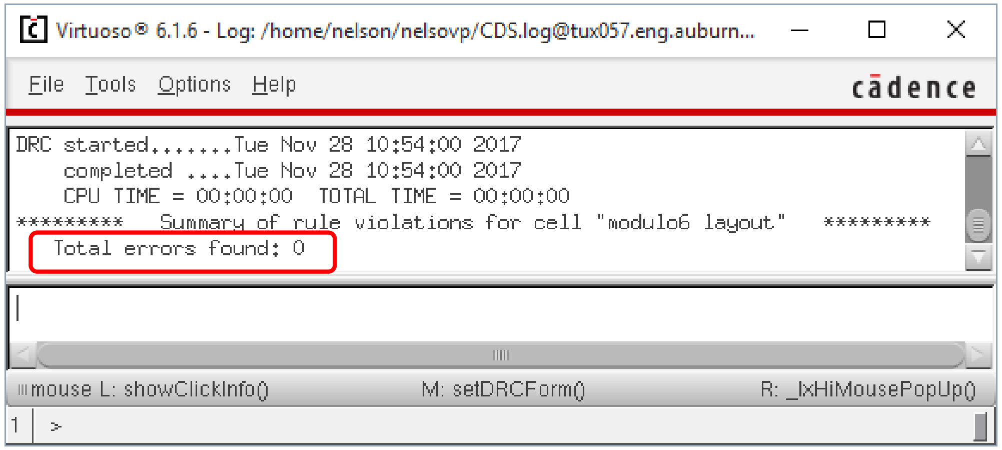
Design rules file →

No violations! →



DRC@tux057.eng.auburn.edu

Checking Method	[✓ flat] hierarchical / hier w/o optimization
Checking Limit	[✓ full] incremental / by area
Coordinate	
Switch Names	
Run-Specific Command File	☐
Inclusion Limit	1000
Limit Rule Errors	☐ 0
Join Nets With Same Name	☐
Limit Run Errors	☐ 0
Echo Commands	✓
Rules File	divaDRC.rul
Rules Library	✓ U_TechLib_ami06
Machine	[✓ local] remote
Machine	
Ignore Missing Cell Masters	☐



Virtuoso® 6.1.6 - Log: /home/nelson/nelsovp/CDS.log@tux057.eng.auburn...

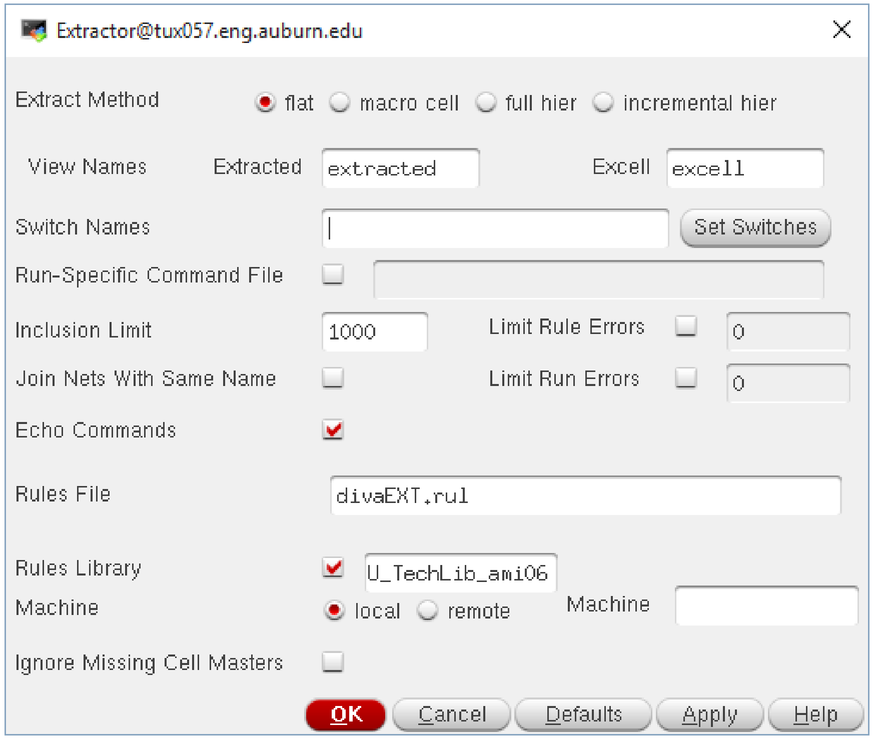
```
DRC started.......Tue Nov 28 10:54:00 2017
    completed ....Tue Nov 28 10:54:00 2017
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********  Summary of rule violations for cell "modulo6 layout"  *********
  Total errors found: 0
```

```
mouse L: showClickInfo()        M: setDRCForm()        R: _lxHiMousePopUp()
1  >
```

Extract to prepare for LVS

Verify > Extract

Extraction rules file ⟶


Extractor@tux057.eng.auburn.edu

Extract Method: [✓ flat] macro cell full hier incremental hier

View Names: Extracted extracted Excell excell

Switch Names:

Run-Specific Command File: ☐

Inclusion Limit: 1000 Limit Rule Errors ☐ 0

Join Nets With Same Name ☐ Limit Run Errors ☐ 0

Echo Commands ✓

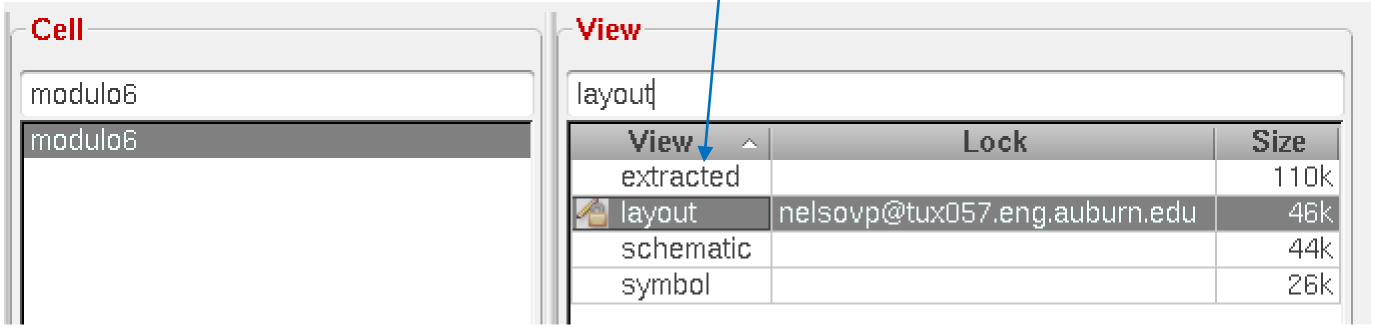
Rules File: divaEXT.rul

Rules Library ✓ U_TechLib_ami06

Machine: [✓ local] remote Machine

Ignore Missing Cell Masters ☐

"extracted" view added to cell


Cell: modulo6

modulo6

View: layout

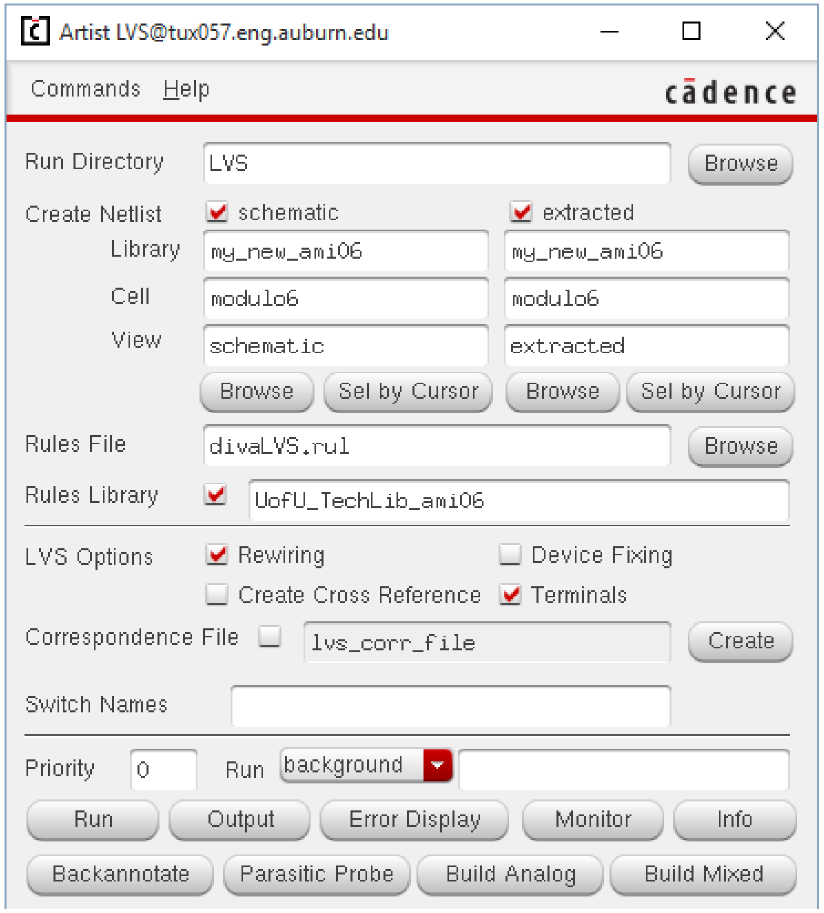
View	Lock	Size
extracted		110k
layout	nelsovp@tux057.eng.auburn.edu	46k
schematic		44k
symbol		26k

Perform layout vs schematic check

Verify > LVS

Browse to select schematic & extracted cell views from library →

LVS rules file →



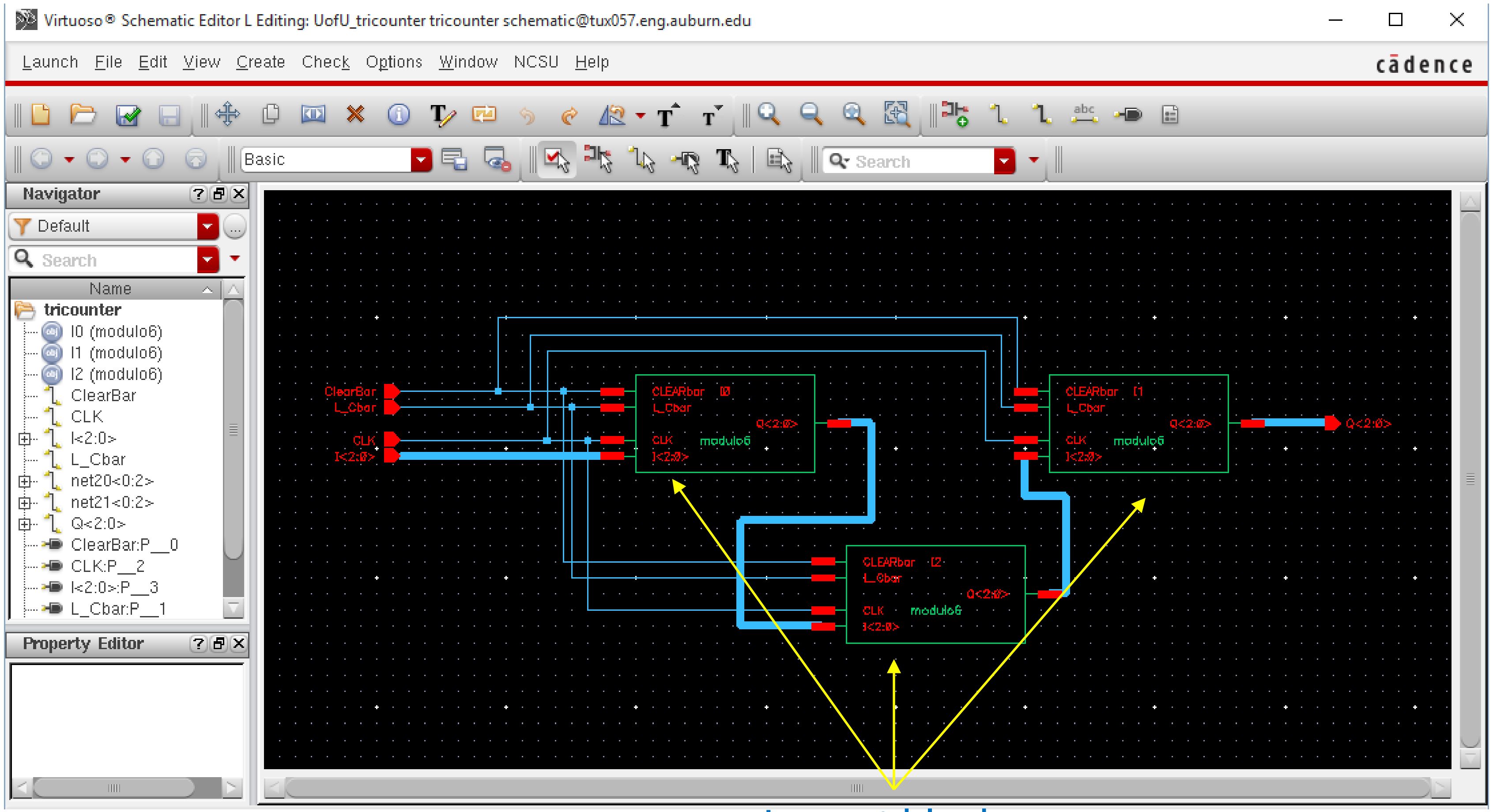
Artist LVS@tux057.eng.auburn.edu

Run Directory	LVS	
Create Netlist	✓ schematic	✓ extracted
Library	my_new_ami06	my_new_ami06
Cell	modulo6	modulo6
View	schematic	extracted
Rules File	divaLVS.rul	
Rules Library	✓ UofU_TechLib_ami06	
LVS Options	✓ Rewiring	Device Fixing
	Create Cross Reference	✓ Terminals
Correspondence File	lvs_corr_file	
Switch Names		
Priority	0	Run background

Top-level bottom-up design process

- Generate block layouts and <u>for</u> <u>each</u> <u>block</u>:
  - Create a Virtuoso library for each block
  - Import DEF file and Verilog netlist
  - Perform DRC-Extract-LVS on each block until "clean"
- Create a block diagram schematic in Virtuoso Schematic
  - Create a library for the top-level block
  - Create a schematic view
  - Instantiate schematic symbols from the library
  - Interconnect with nets and add pins
  - Check and save
- Create a layout from the schematic diagram

Top-level block schematic in “Schematics XL”



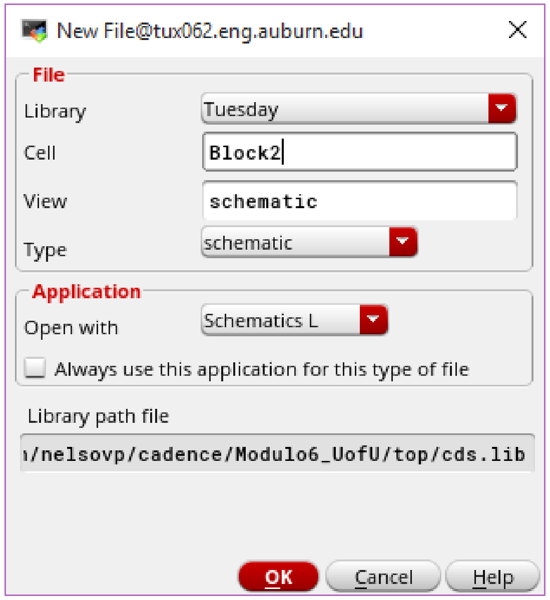
Layout blocks

Creating the block diagram

- Library Manager: File > New > Library

  (new library for the block diagram and its layout)

- Library Manger:
  - Select the new library
  - File > New > Cell View
  - Fill in the form
  - OK to open “Composer”



New File@tux062.eng.auburn.edu

File

Library	Tuesday
Cell	Block2
View	schematic
Type	schematic

Application

Open with: Schematics L

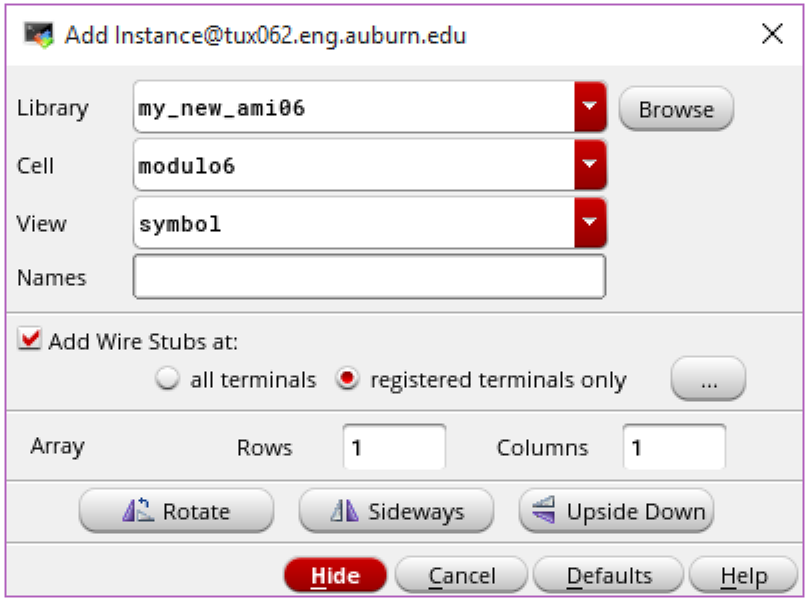
Always use this application for this type of file

Library path file

```
ı/nelsovp/cadence/Modulo6_UofU/top/cds.lib
```

Drawing schematics

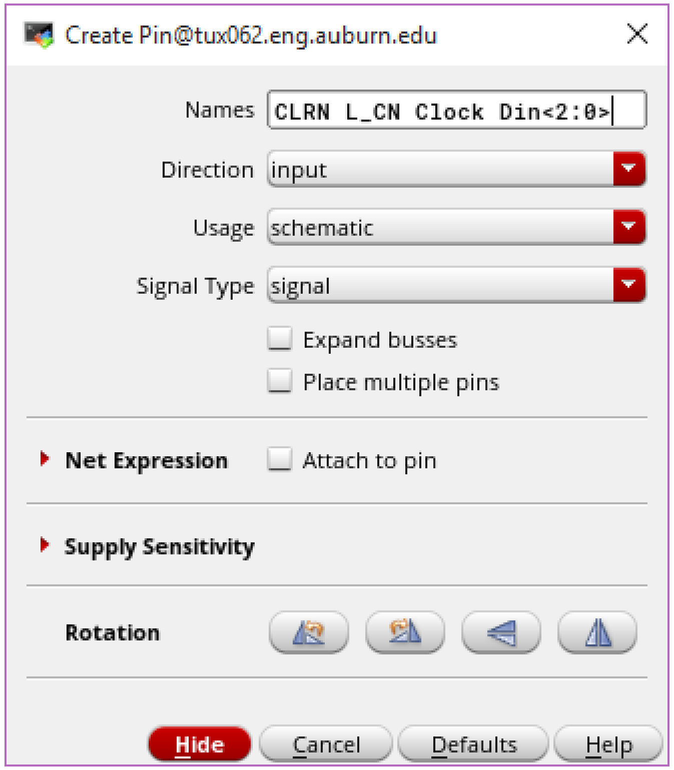
- Add instances:
  - Create > Instance
  - Select cell from lib.
  - Move cell to position
  - Left click to place
  - Repeat for more inst's
  - ESC to exit



Library: my_new_ami06
Cell: modulo6
View: symbol
Names:
[✓] Add Wire Stubs at:
all terminals [✓ registered terminals only]
Array Rows: 1 Columns: 1

Drawing schematics

- Add pins:
  - Create > Pin
  - Enter name(s)
  - Move cursor to position
  - Left click to place first
  - Repeat for each pin
  - ESC to exit



Create Pin@tux062.eng.auburn.edu

Names: CLRN L_CN Clock Din<2:0>

Direction: input

Usage: schematic

Signal Type: signal

☐ Expand busses

☐ Place multiple pins

Net Expression ☐ Attach to pin

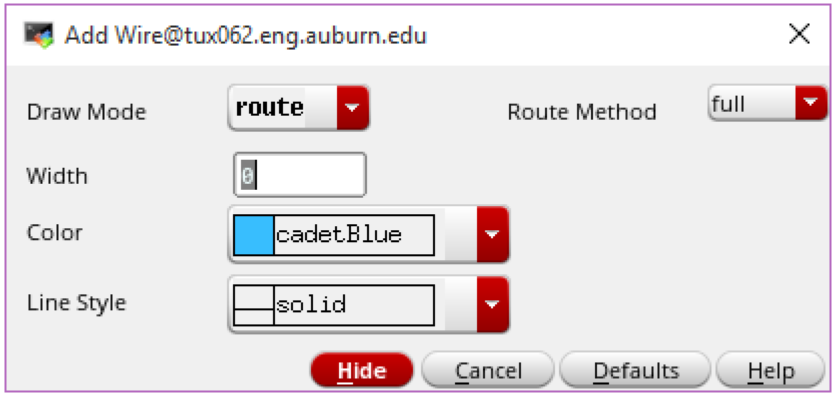
Supply Sensitivity

Rotation

Drawing schematics

- Add wires:
  - Create > Wire (narrow)
  - Cursor to pin
  - Left click to begin
  - Cursor to other pin
  - Left click to end

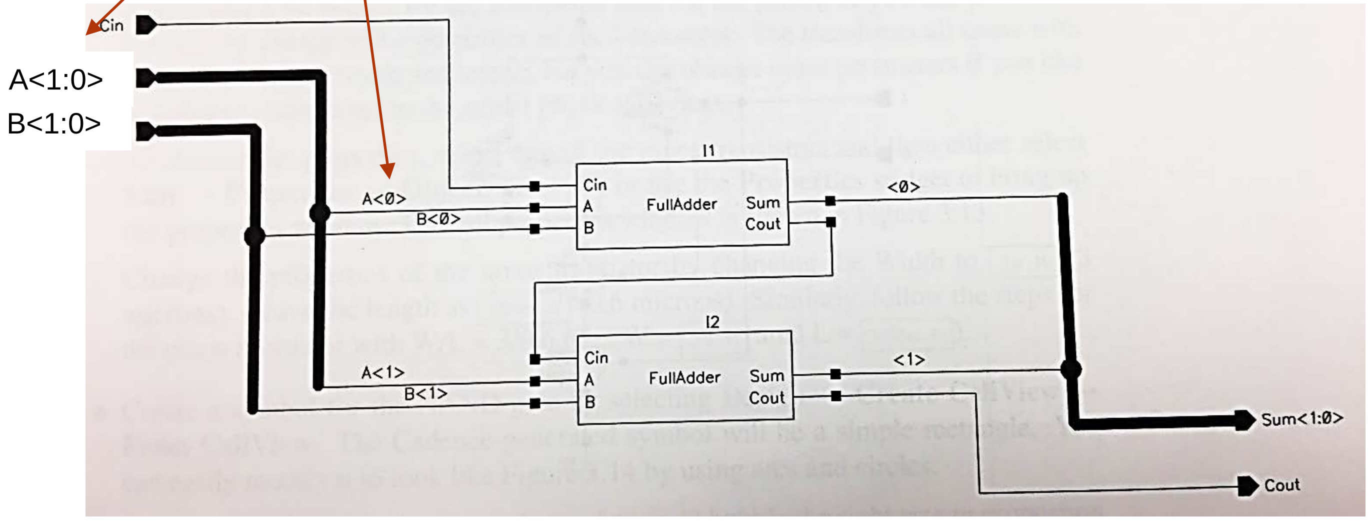
    (Left click in between for "bends")
  - Add more wires.
  - ESC (Cancel) when finished
- Create > Wire (wide) for buses
- Create > Wire Name to name a wire
- Check > Current Cellview to detect drawing errors
- File > Save (Schematic) and Close


Add Wire@tux062.eng.auburn.edu

Draw Mode: route
Route Method: full
Width: 0
Color: cadetBlue
Line Style: solid

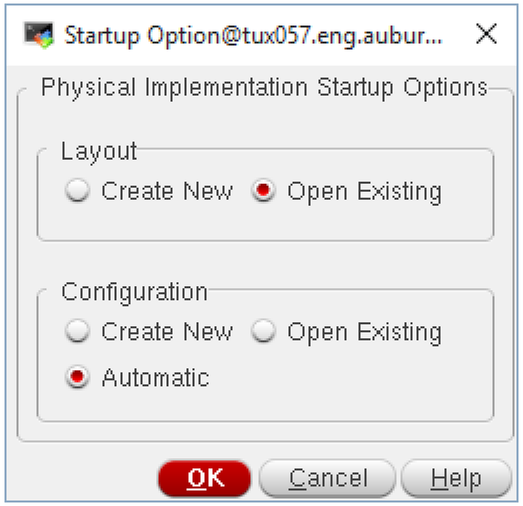
Individual wires from buses

- Buses inherit pin names
  - Bus A<1:0> contains wires A<1> and A<0>
  - Use ***Create > Wire name*** to change wire name(s)
- Use individual wire name from bus to connect to single-wire pin



Generate layout from the schematic

From Schematics Menu:
Launch > Layout GXL

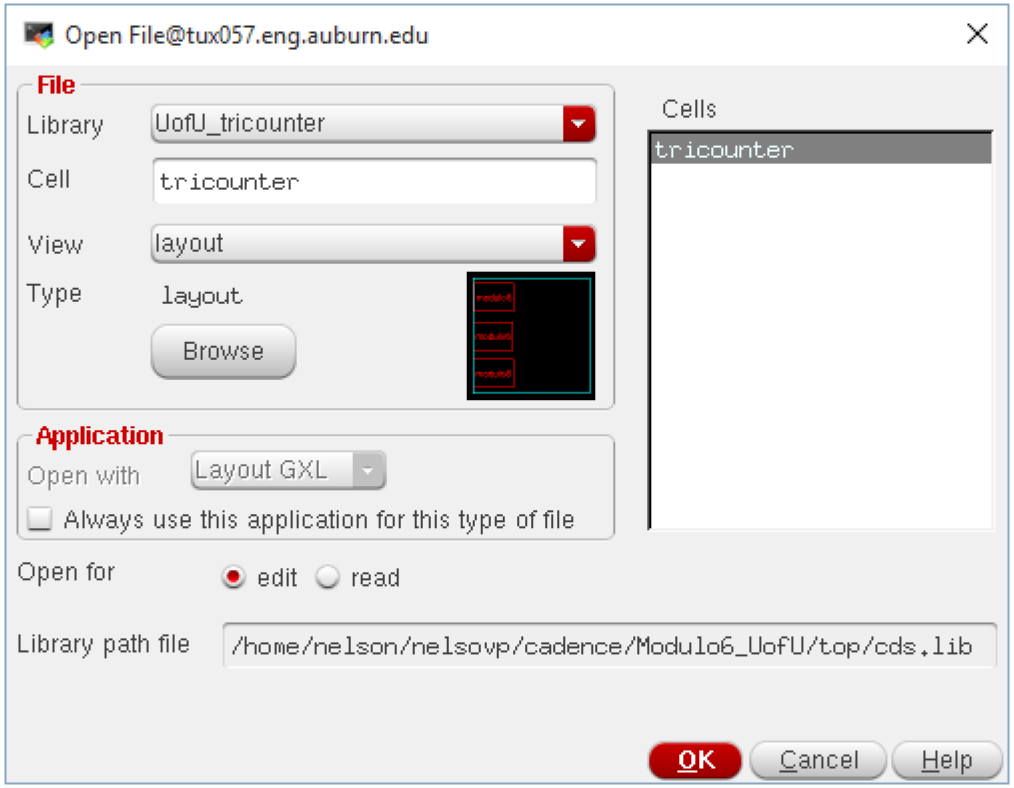


Startup Option@tux057.eng.aubur...

Physical Implementation Startup Options

Layout
Create New [✓ Open Existing]

Configuration
Create New Open Existing [✓ Automatic]



Open File@tux057.eng.auburn.edu

File

Library	UofU_tricounter
Cell	tricounter
View	layout
Type	layout

Cells: tricounter

Application

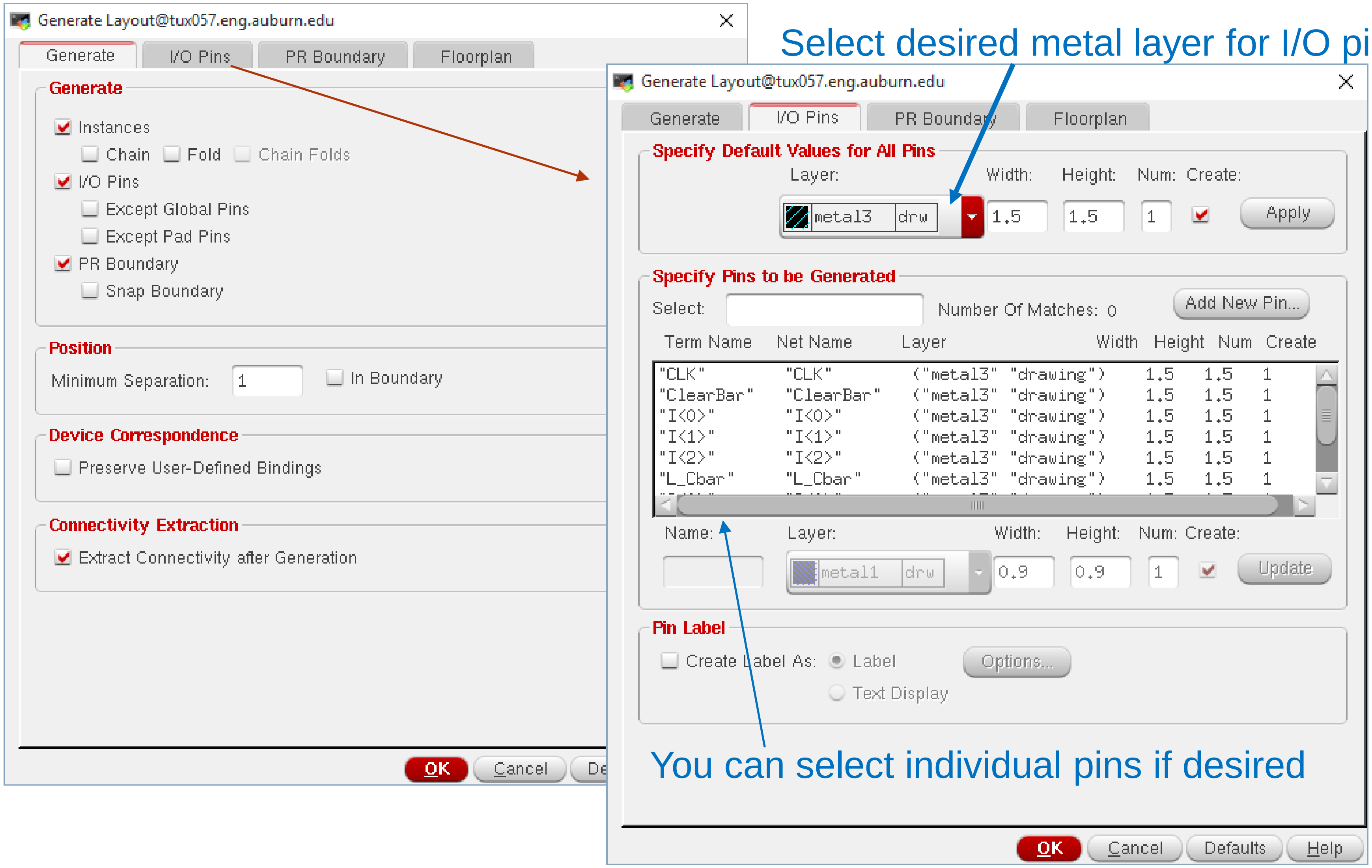
Open with: Layout GXL
Always use this application for this type of file

Open for [✓ edit] read

Library path file: /home/nelson/nelsovp/cadence/Modulo6_UofU/top/cds.lib

From Layout Menu:
Connectivity > Layout GXL

Or click icon in bottom left corner:



Generate Layout@tux057.eng.auburn.edu

Generate
- [✓] Instances
  - [ ] Chain [ ] Fold [ ] Chain Folds
- [✓] I/O Pins
  - [ ] Except Global Pins
  - [ ] Except Pad Pins
- [✓] PR Boundary
  - [ ] Snap Boundary

Position
Minimum Separation: 1 [ ] In Boundary

Device Correspondence
[ ] Preserve User-Defined Bindings

Connectivity Extraction
[✓] Extract Connectivity after Generation

Select desired metal layer for I/O pins

Generate Layout@tux057.eng.auburn.edu

Specify Default Values for All Pins

Layer:	Width:	Height:	Num:	Create:
metal3 drw	1.5	1.5	1	✓

Specify Pins to be Generated
Select: Number Of Matches: 0

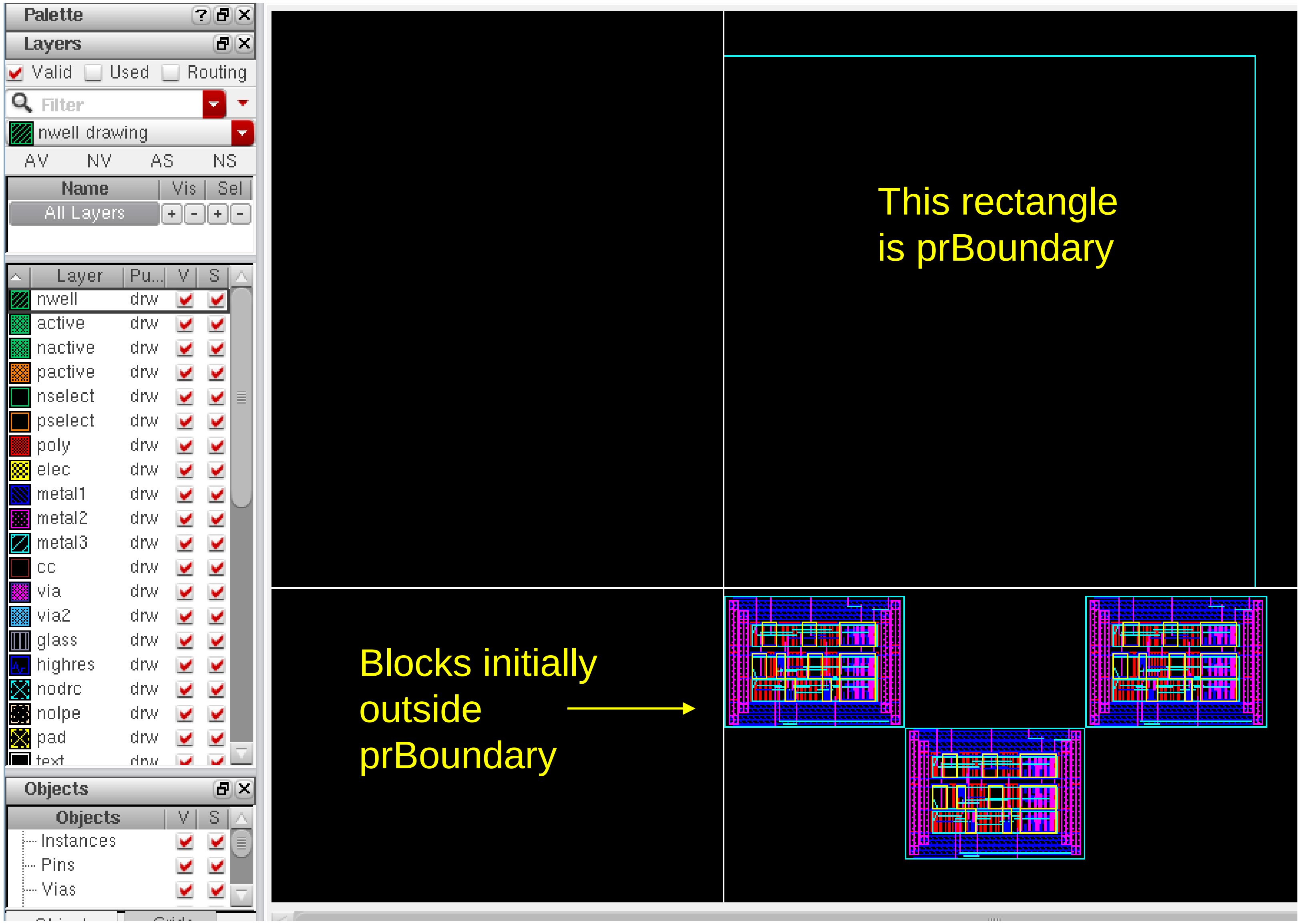
```
Term Name    Net Name     Layer                      Width  Height  Num  Create
"CLK"        "CLK"        ("metal3" "drawing")       1.5    1.5     1
"ClearBar"   "ClearBar"   ("metal3" "drawing")       1.5    1.5     1
"I<0>"       "I<0>"       ("metal3" "drawing")       1.5    1.5     1
"I<1>"       "I<1>"       ("metal3" "drawing")       1.5    1.5     1
"I<2>"       "I<2>"       ("metal3" "drawing")       1.5    1.5     1
"L_Cbar"     "L_Cbar"     ("metal3" "drawing")       1.5    1.5     1
```

Name:	Layer:	Width:	Height:	Num:	Create:
	metal1 drw	0.9	0.9	1	✓

Pin Label
[ ] Create Label As: (● Label) ○ Text Display

You can select individual pins if desired

Before module and I/O placement



☑ Valid ☐ Used ☐ Routing

nwell drawing

Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓
via	drw	✓	✓
via2	drw	✓	✓
glass	drw	✓	✓
highres	drw	✓	✓
nodrc	drw	✓	✓
nolpe	drw	✓	✓
pad	drw	✓	✓
text	drw	✓	✓

Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

This rectangle is prBoundary

Blocks initially outside prBoundary $\longrightarrow$

To view block details: Options > Display form - set display levels “Stop” to 30

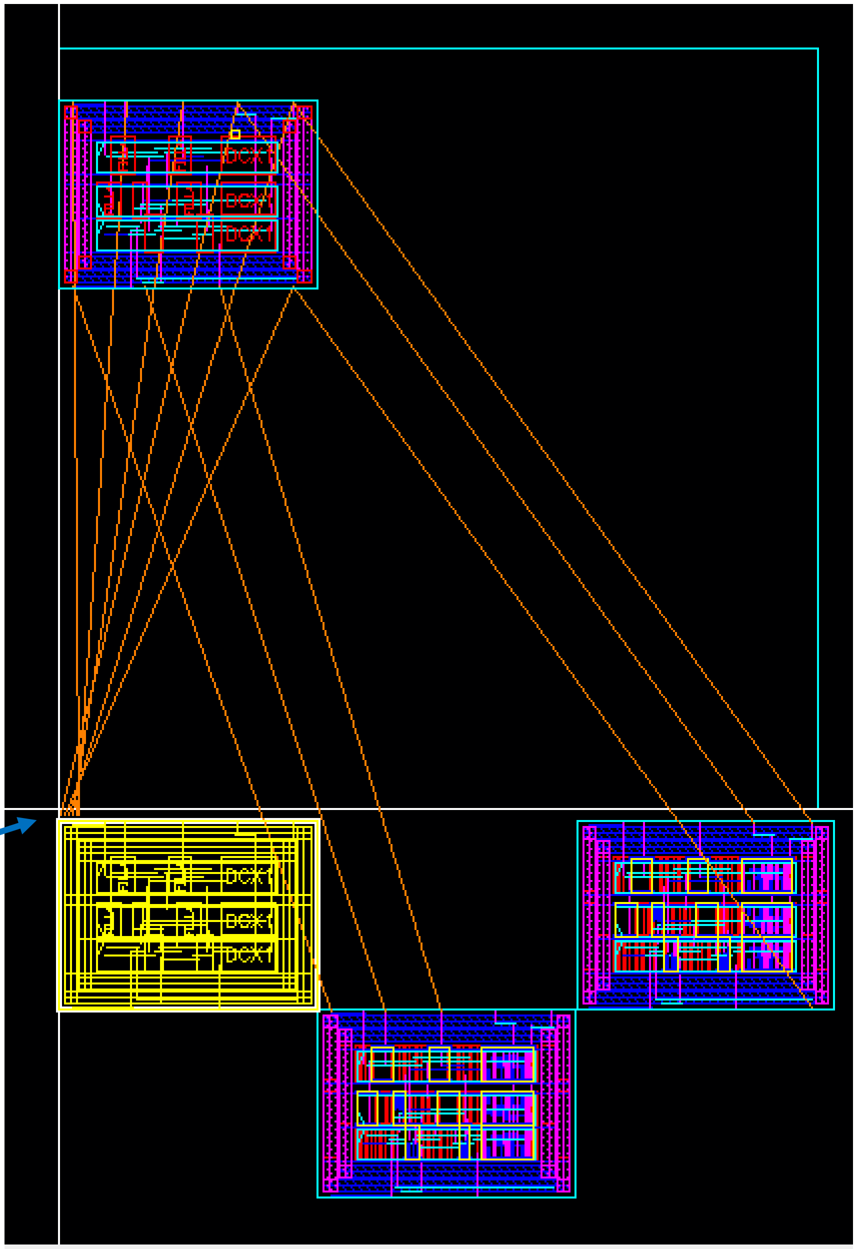
Drag blocks to desired floorplan locations

“Move” hotkey = m

Note the block connections.

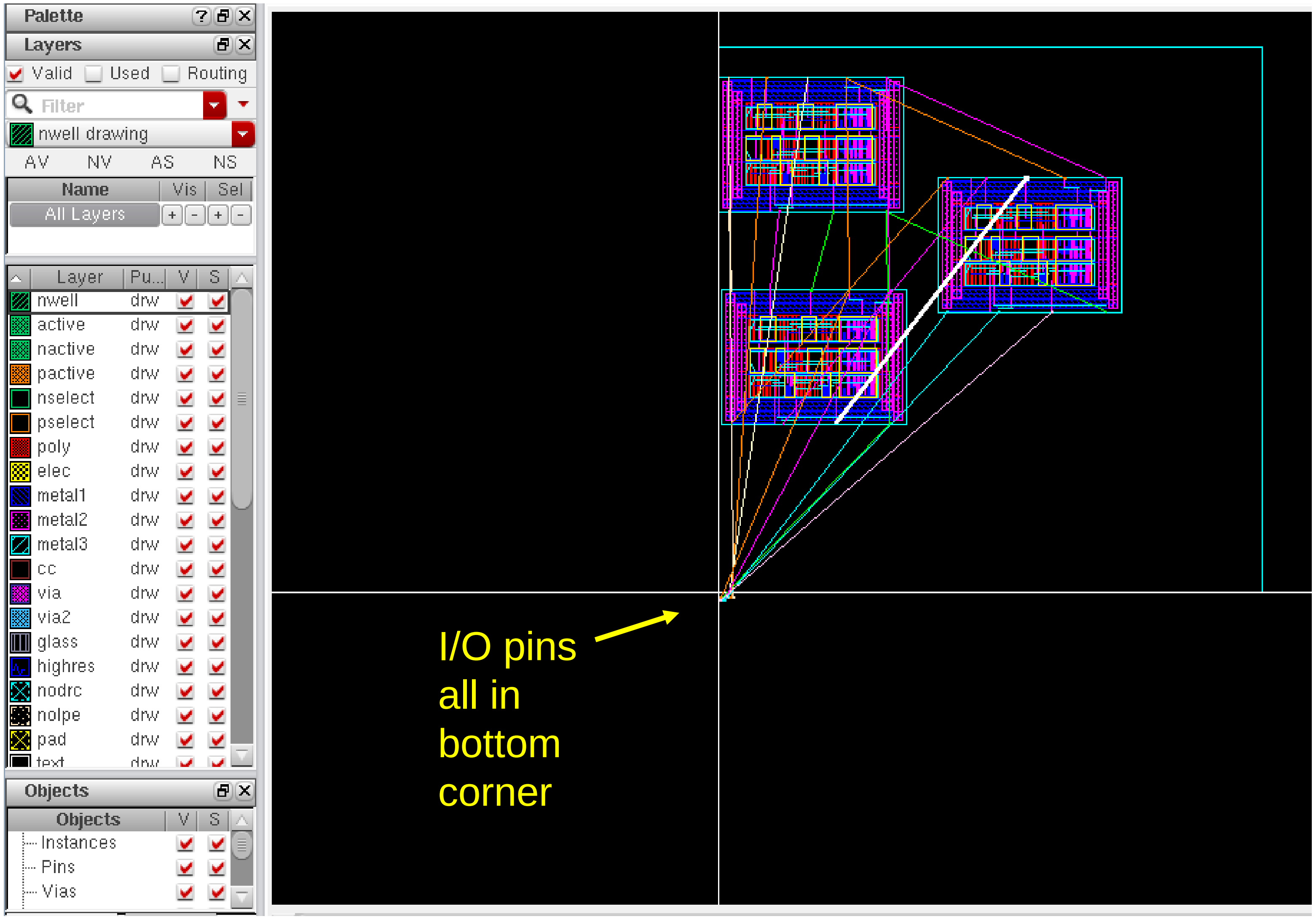
These will also be highlighted in the schematic window.

I/O pins all in bottom corner



After placing modules

To see the nets: *Connectivity > Analyze*
Connectivity > Nets > Show/Hide All Incomplete Nets



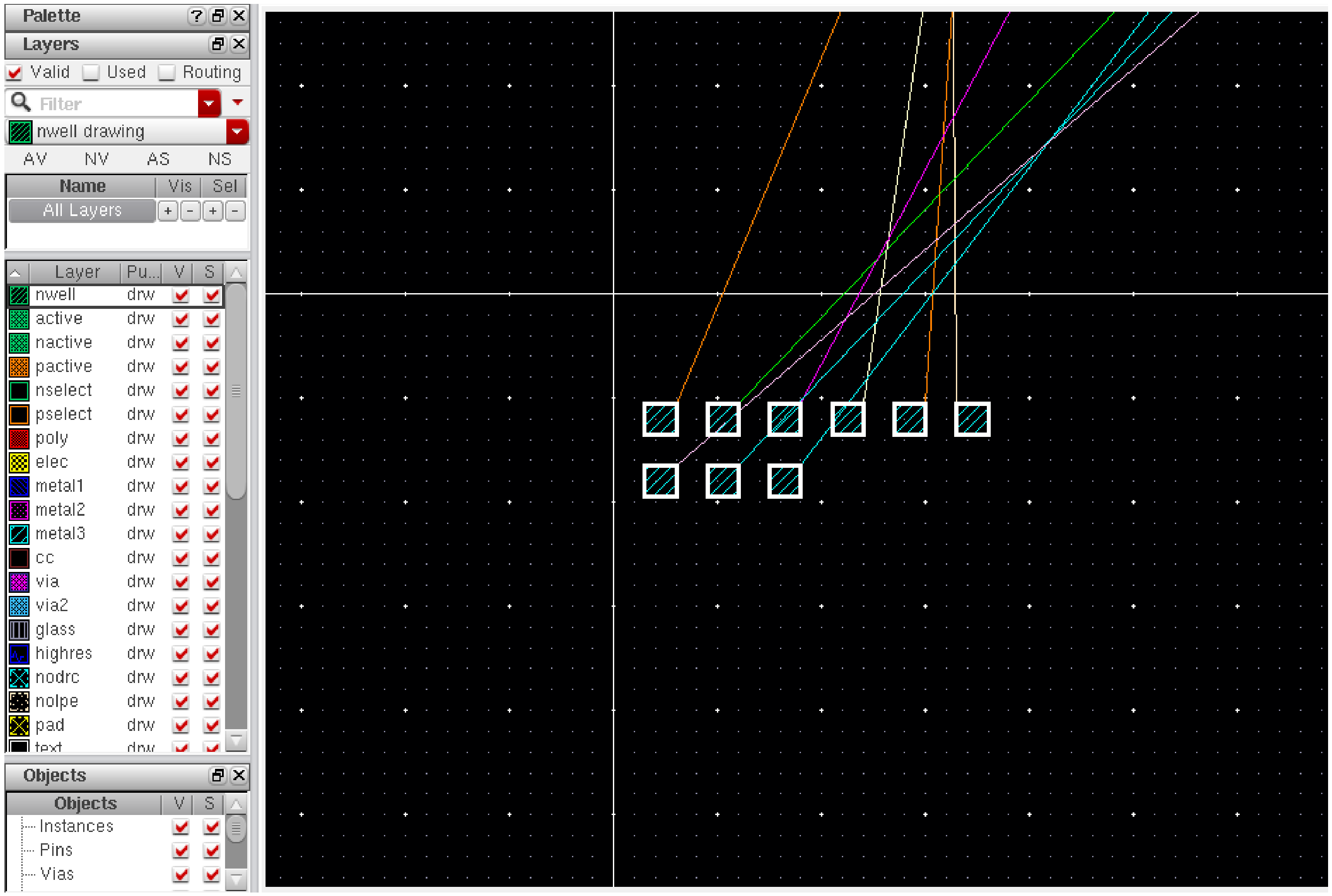
Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓
via	drw	✓	✓
via2	drw	✓	✓
glass	drw	✓	✓
highres	drw	✓	✓
nodrc	drw	✓	✓
nolpe	drw	✓	✓
pad	drw	✓	✓
text	drw	✓	✓

Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

I/O pins all in bottom corner

Zoom in on lower left corner to view I/O pins

- Select and drag manually to desired boundary edge
- Or auto-place the pins (next slide)



Autoroute pins:
Place > Pin Placement

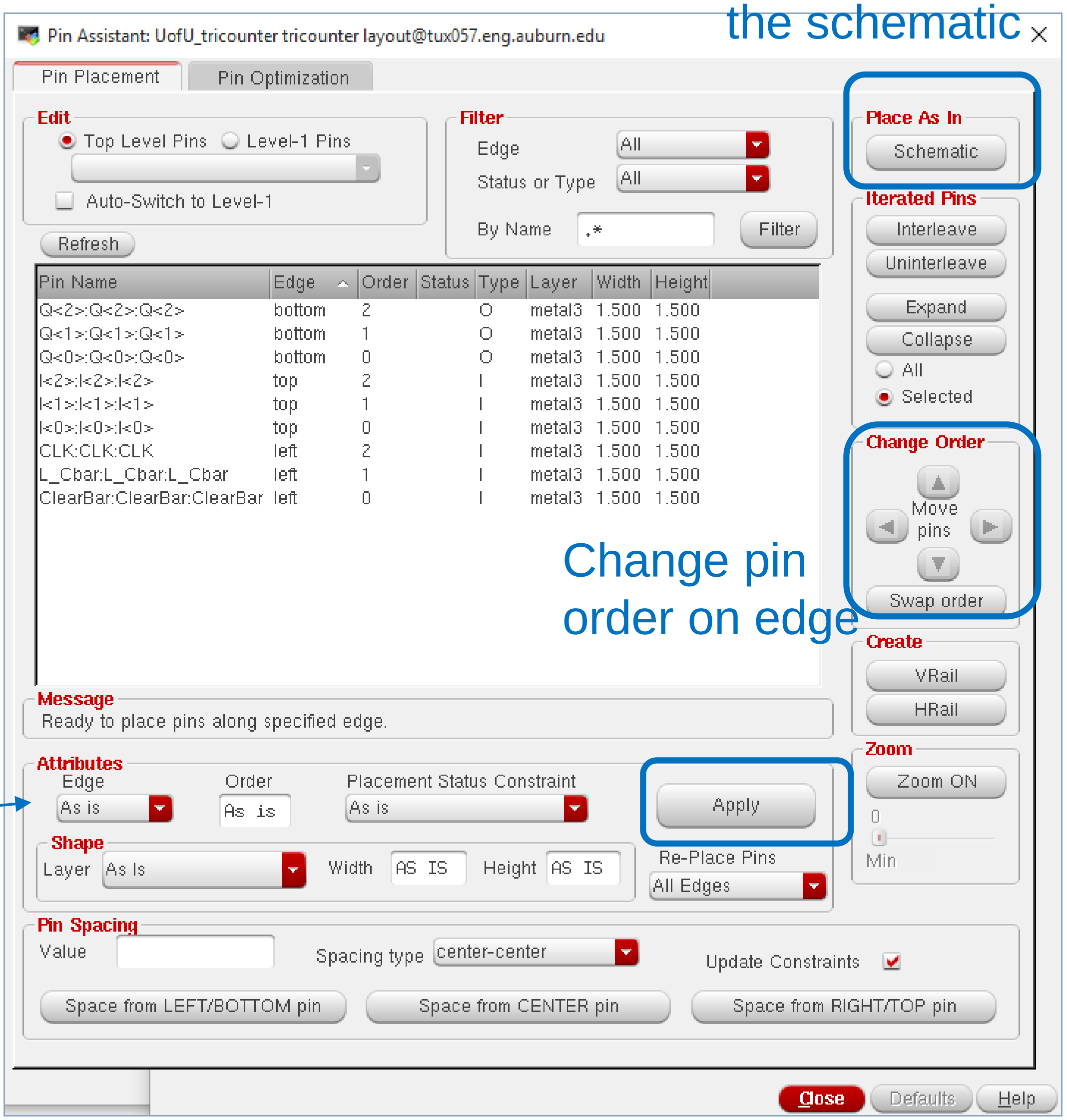
To place pins on specific edges:

Select pins to be placed →

Select Edge and Apply →

Can place as in the schematic

Change pin order on edge


Pin Assistant: UofU_tricounter tricounter layout@tux057.eng.auburn.edu

Pin Name	Edge	Order	Status	Type	Layer	Width	Height
Q<2>:Q<2>:Q<2>	bottom	2		O	metal3	1.500	1.500
Q<1>:Q<1>:Q<1>	bottom	1		O	metal3	1.500	1.500
Q<0>:Q<0>:Q<0>	bottom	0		O	metal3	1.500	1.500
I<2>:I<2>:I<2>	top	2		I	metal3	1.500	1.500
I<1>:I<1>:I<1>	top	1		I	metal3	1.500	1.500
I<0>:I<0>:I<0>	top	0		I	metal3	1.500	1.500
CLK:CLK:CLK	left	2		I	metal3	1.500	1.500
L_Cbar:L_Cbar:L_Cbar	left	1		I	metal3	1.500	1.500
ClearBar:ClearBar:ClearBar	left	0		I	metal3	1.500	1.500

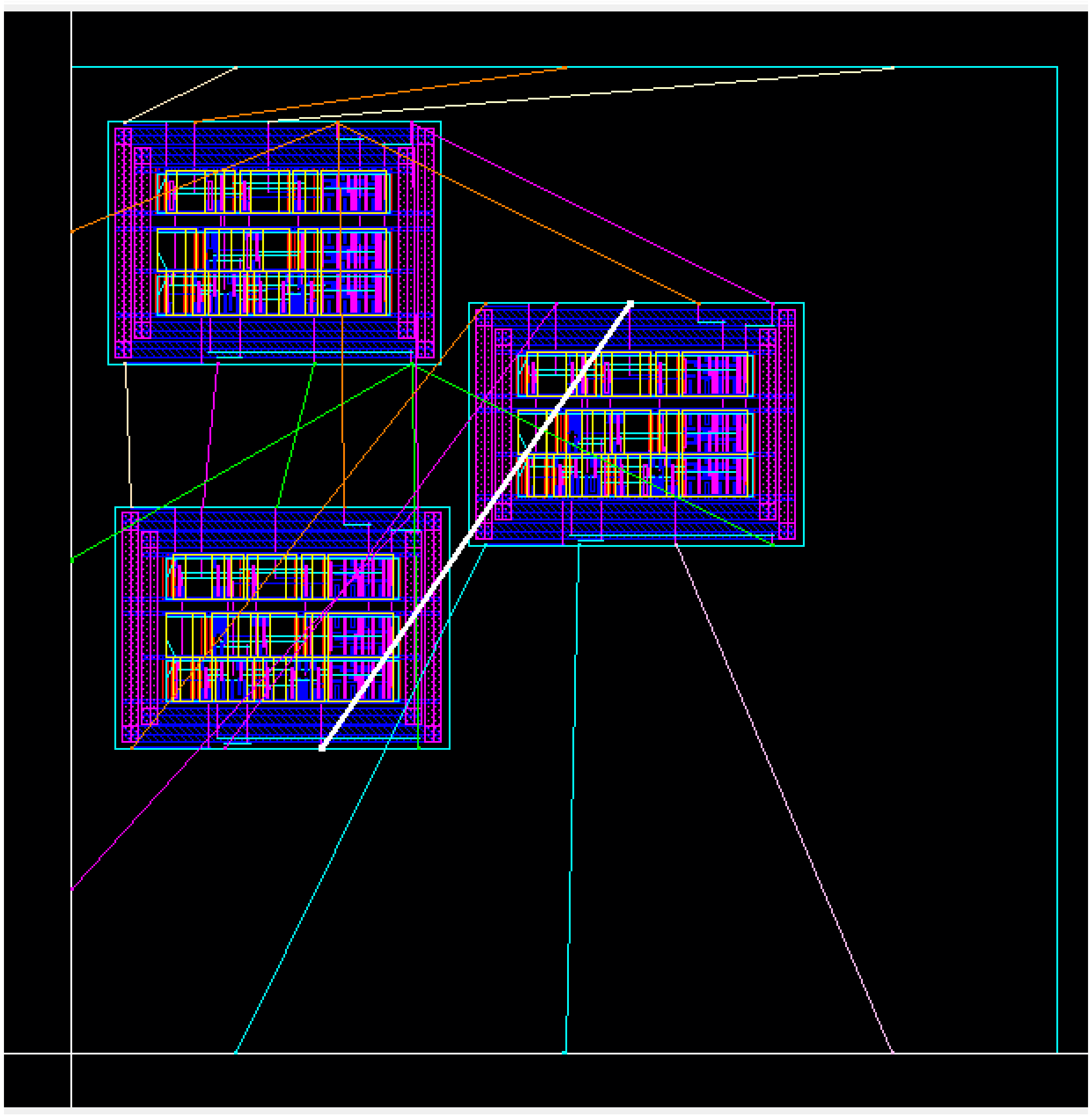
Message
Ready to place pins along specified edge.

Attributes
Edge: As is
Order: As is
Placement Status Constraint: As is
Apply
Shape
Layer: As Is
Width: AS IS
Height: AS IS
Re-Place Pins: All Edges

Pin Spacing
Value:
Spacing type: center-center
Update Constraints ✓
Space from LEFT/BOTTOM pin
Space from CENTER pin
Space from RIGHT/TOP pin

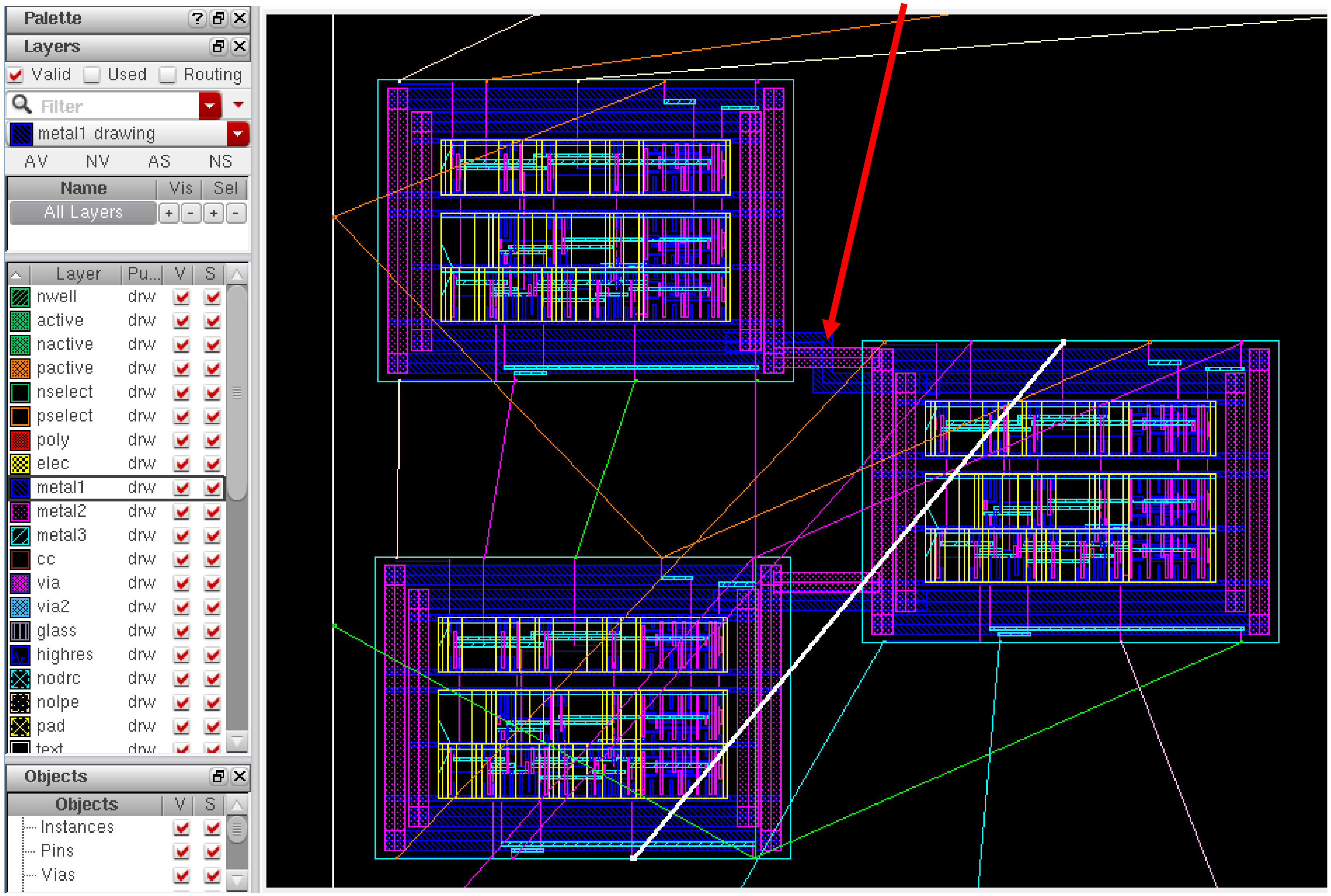
Layout updated automatically – continue changes until happy with arrangement

Final pin placement



Power routing between blocks

Draw “Shape” or “Path” to connect power and ground rails of blocks

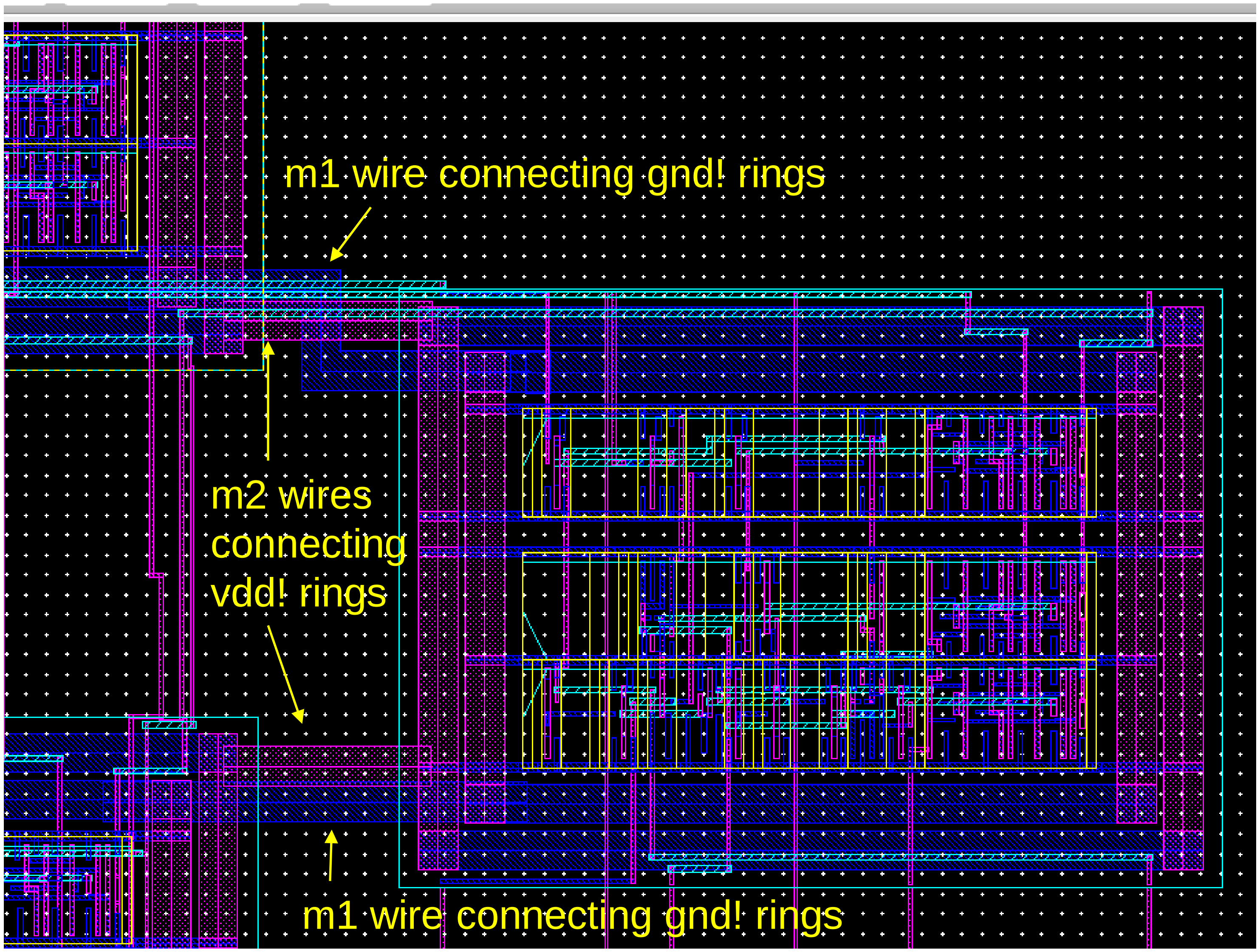


Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓
via	drw	✓	✓
via2	drw	✓	✓
glass	drw	✓	✓
highres	drw	✓	✓
nodrc	drw	✓	✓
nolpe	drw	✓	✓
pad	drw	✓	✓
text	drw	✓	✓

Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

Mine is not “pretty” since my blocks have pins on M2 close to M2 of power rings!

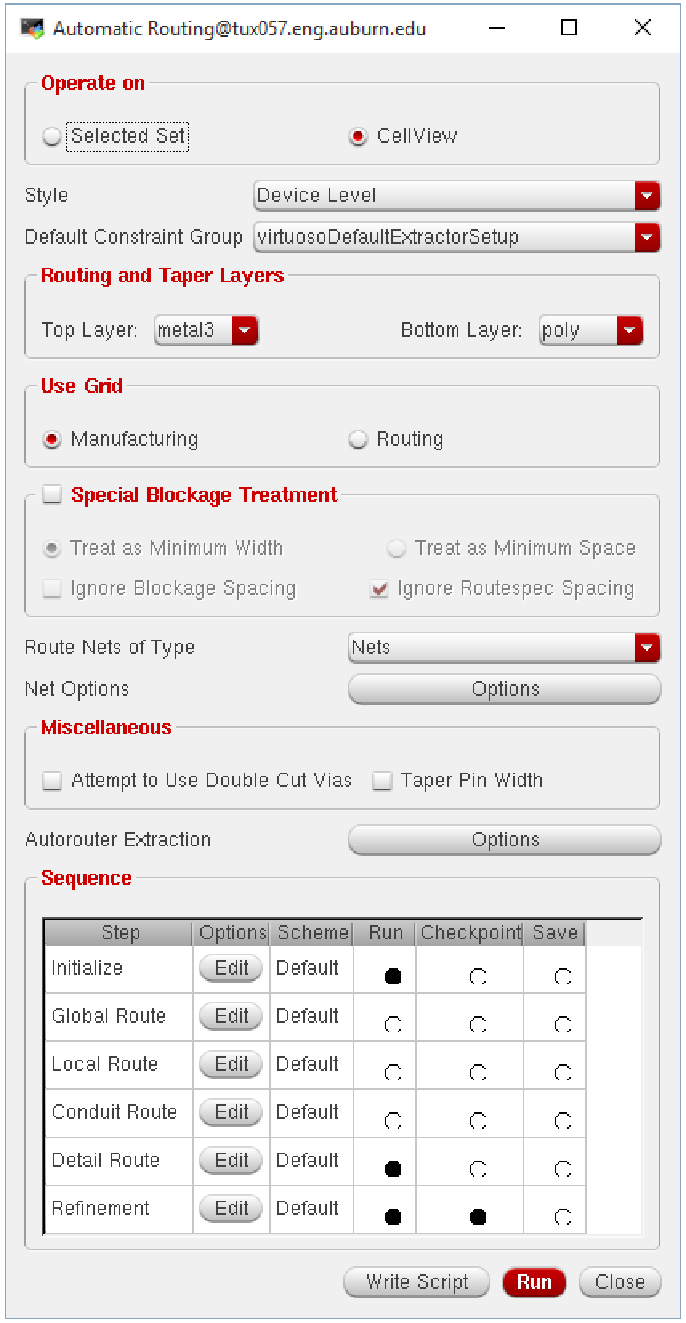
Example" wires connecting power rings (you may choose different wires/layers)


m1 wire connecting gnd! rings
m2 wires connecting vdd! rings
m1 wire connecting gnd! rings

Signal wire routing:
Use the Virtuoso Autorouter
(Virtuoso Space-Based Router)

Route > Automatic Routing

Default values recommended.


Automatic Routing@tux057.eng.auburn.edu

Operate on

○ Selected Set [✓ CellView]

Style: Device Level

Default Constraint Group: virtuosoDefaultExtractorSetup

Routing and Taper Layers

Top Layer: metal3 Bottom Layer: poly

Use Grid

[✓ Manufacturing] ○ Routing

☐ **Special Blockage Treatment**

[✓ Treat as Minimum Width] ○ Treat as Minimum Space

☐ Ignore Blockage Spacing ☑ Ignore Routespec Spacing

Route Nets of Type: Nets

Net Options: Options

Miscellaneous

☐ Attempt to Use Double Cut Vias ☐ Taper Pin Width

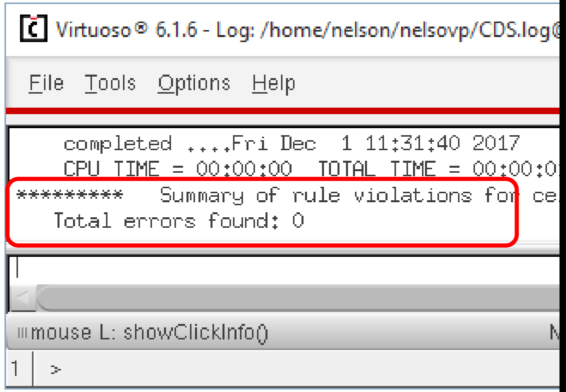
Autorouter Extraction: Options

Sequence

Step	Options	Scheme	Run	Checkpoint	Save
Initialize	Edit	Default	●	○	○
Global Route	Edit	Default	○	○	○
Local Route	Edit	Default	○	○	○
Conduit Route	Edit	Default	○	○	○
Detail Route	Edit	Default	●	○	○
Refinement	Edit	Default	●	●	○

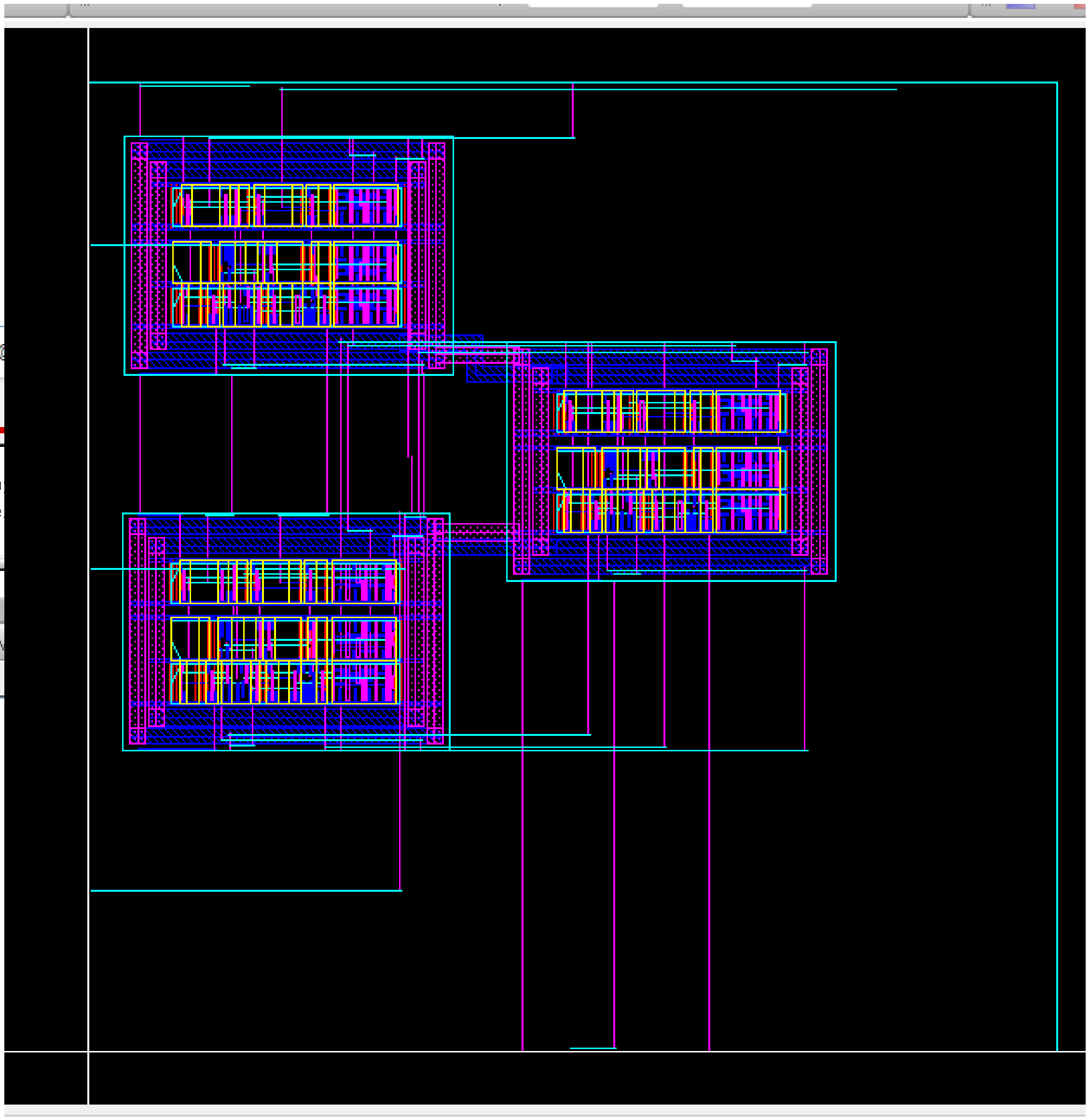
Fully-routed circuit block

Run DRC-Extract-LVS



Virtuoso® 6.1.6 - Log: /home/nelson/nelsovp/CDS.log

```
    completed ....Fri Dec  1 11:31:40 2017
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:0
**********   Summary of rule violations for ce
   Total errors found: 0
```

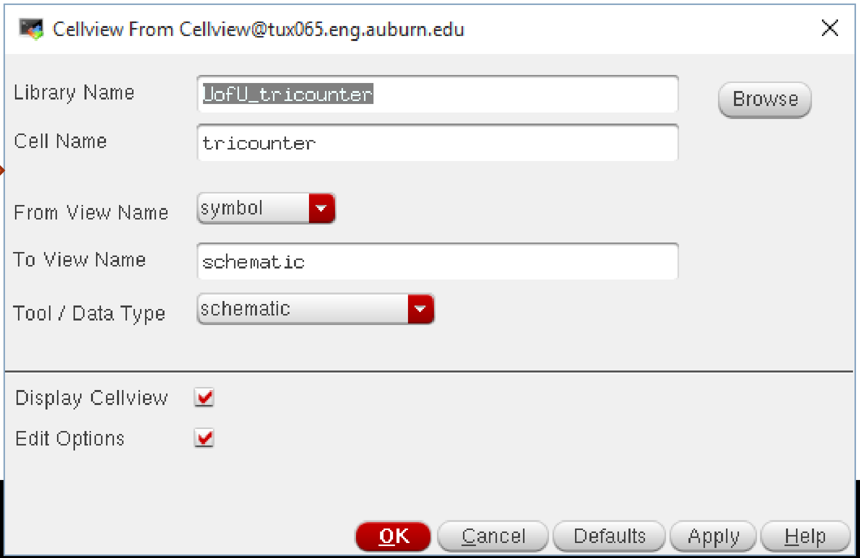


SAVE!!

Block symbol (to connect to I/O pads)

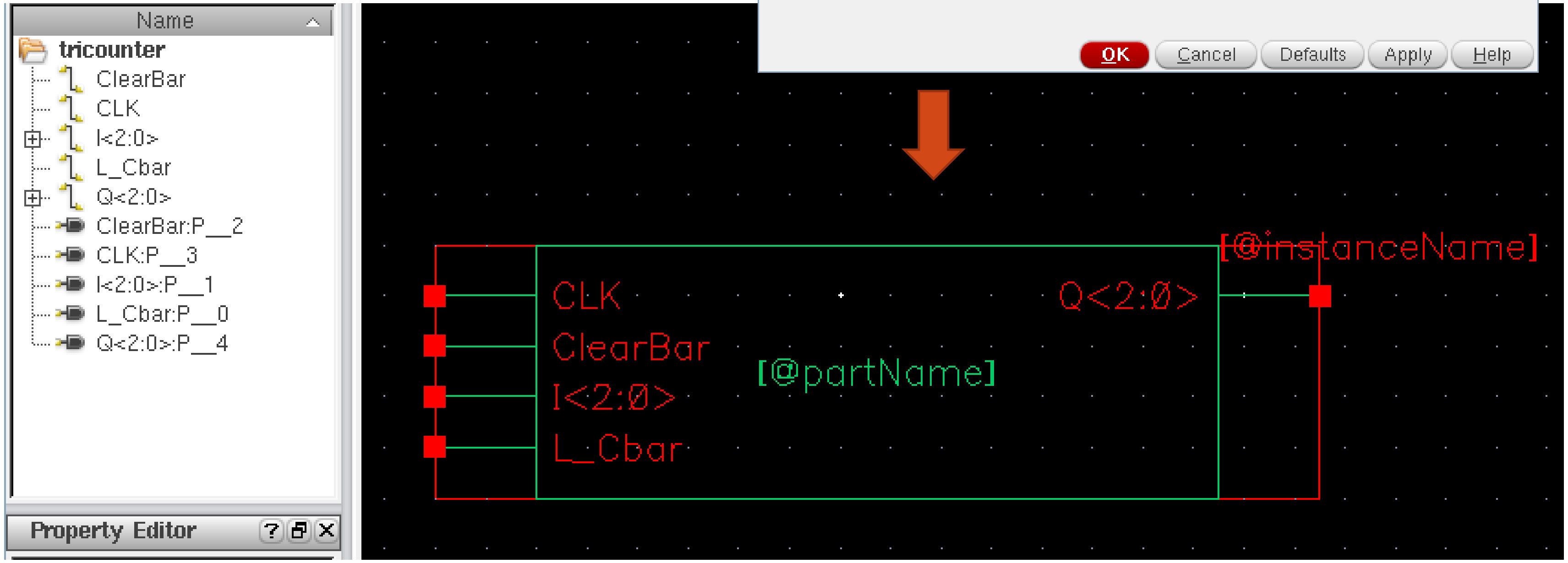
With Schematic Open:
Create > Cellview > From Cellview

Check and Save



Cellview From Cellview@tux065.eng.auburn.edu

Library Name	UofU_tricounter
Cell Name	tricounter
From View Name	symbol
To View Name	schematic
Tool / Data Type	schematic
Display Cellview	✓
Edit Options	✓



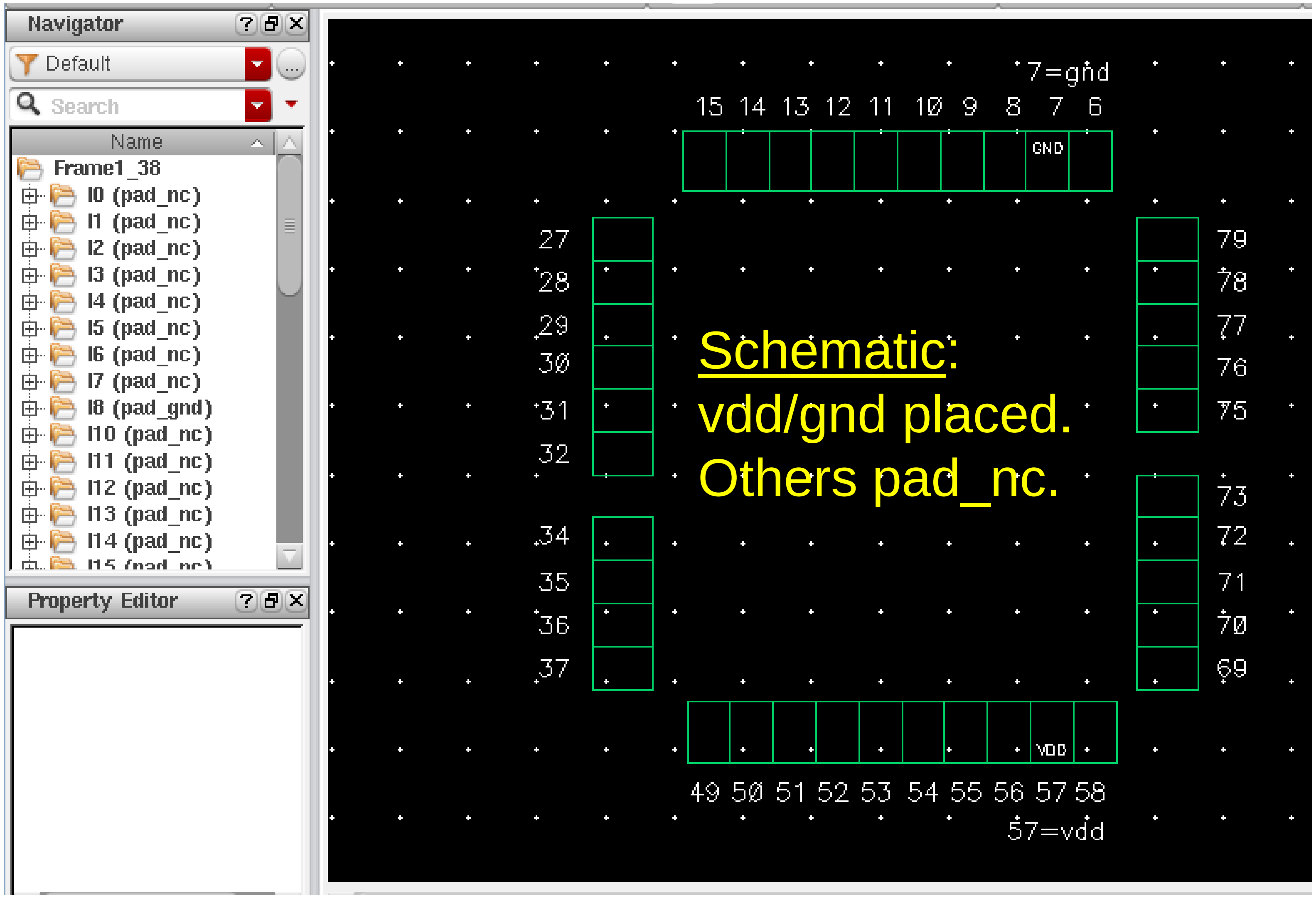
Name
tricounter
- ClearBar
- CLK
- I<2:0>
- L_Cbar
- Q<2:0>
- ClearBar:P__2
- CLK:P__3
- I<2:0>:P__1
- L_Cbar:P__0
- Q<2:0>:P__4

Prepare for full chip layout

- Make a new PadFrame library (so you can edit Frame1_38)
  - Attach to UofU_TechLib_ami06
  - Select cell Frame1_38 in library UofU_Pads
  - Copy it to your PadFrame library (Edit > Copy)
    - If you get an error message, click "Fix Errors" and then OK
- Edit your pad frame <u>schematic</u> to change **pad_nc** instances to **pad_in** or **pad_out** for your circuit I/O signals
  - Decide which pins you wish for circuit I/O signals
  - Create a symbol view from the edited schematic
- Create a schematic comprising circuit block and pad frame
- Edit your pad frame <u>layout</u> to match the schematic
  - Change pad properties from "pad_nc" to "pad_in" or "pad_out"
- Create chip layout from chip schematic

Pad frame schematic showing I/O pads

Use the Frame1_38 cell that you copied to your PadFrame library

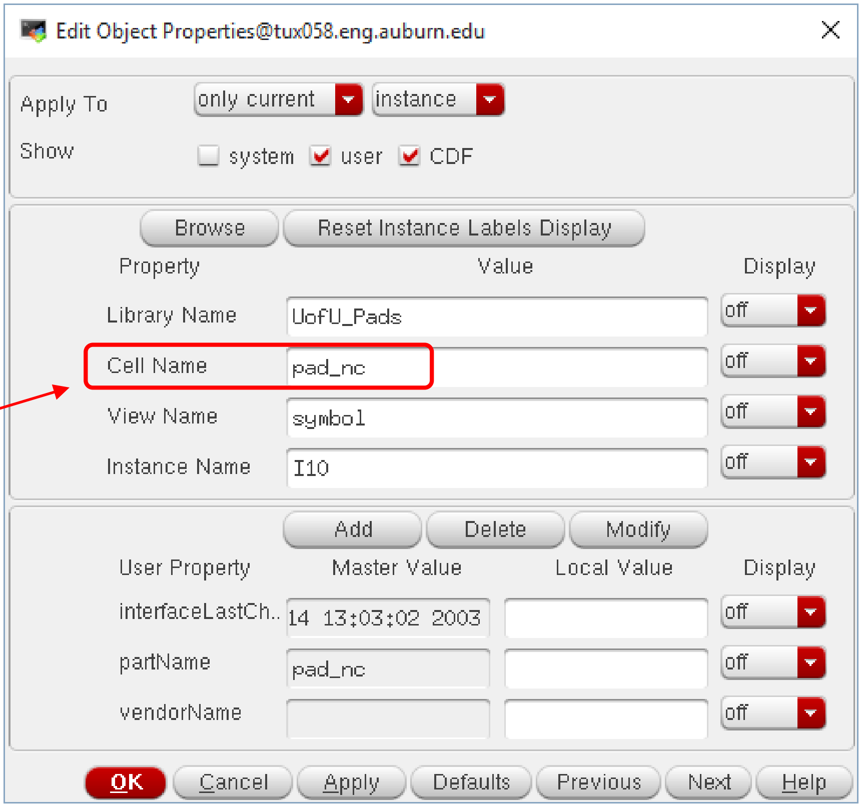


Frame1_38
- I0 (pad_nc)
- I1 (pad_nc)
- I2 (pad_nc)
- I3 (pad_nc)
- I4 (pad_nc)
- I5 (pad_nc)
- I6 (pad_nc)
- I7 (pad_nc)
- I8 (pad_gnd)
- I10 (pad_nc)
- I11 (pad_nc)
- I12 (pad_nc)
- I13 (pad_nc)
- I14 (pad_nc)
- I15 (pad_nc)

Schematic:
vdd/gnd placed.
Others pad_nc.

Modify pad frame schematic for your project

- Leave VDD and GND pads alone – unless you really want them elsewhere.
- Decide which pad to use for each I/O pin on your layout block.
- Change Cell Names of desired signal pads from pad_nc to pad_in or pad_out
  - Click on pad to select it
  - Open properties with hot key "q" or right mouse button

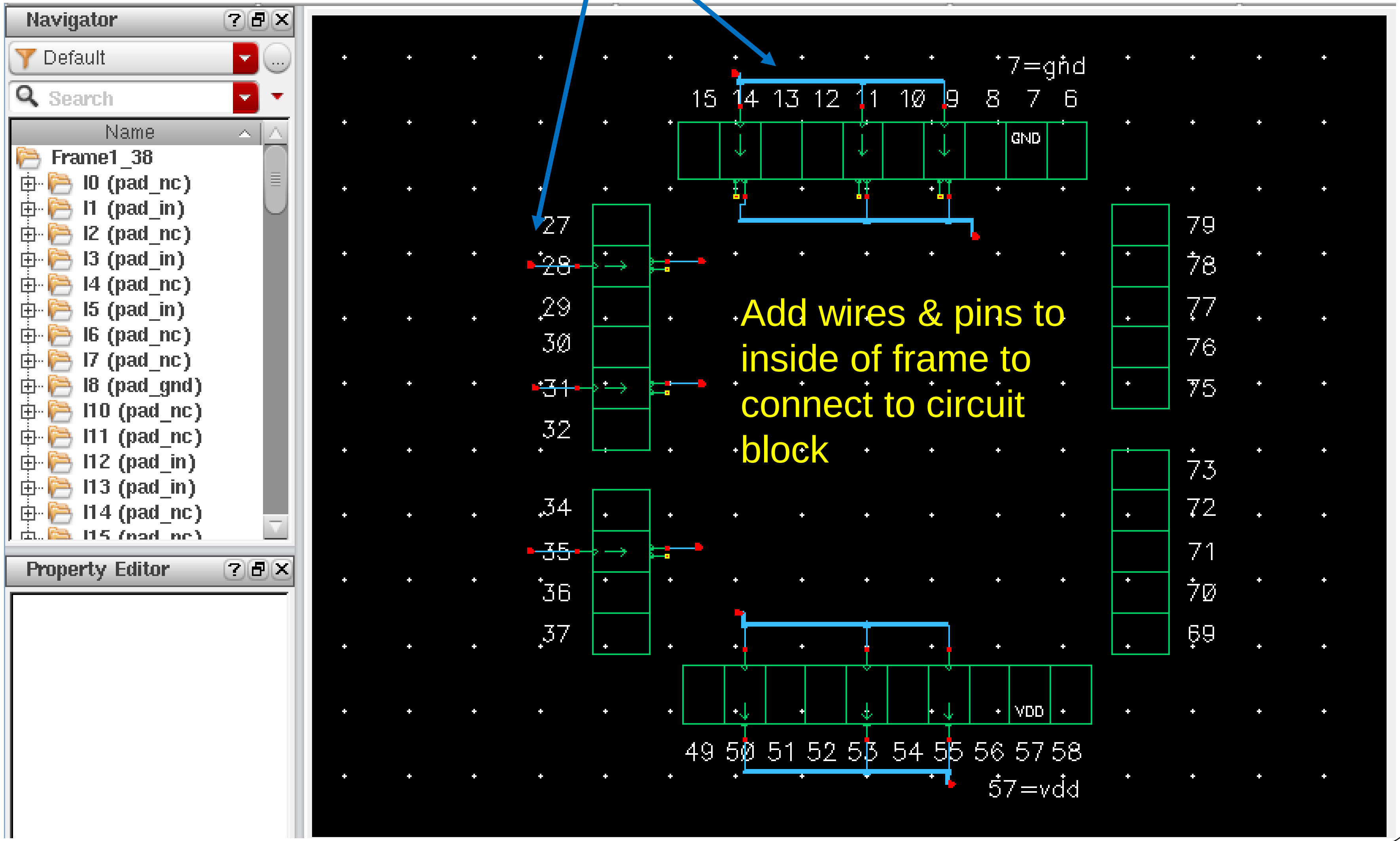

Edit Object Properties@tux058.eng.auburn.edu
Browse
Reset Instance Labels Display
Add
Delete
Modify
OK
Cancel
Apply
Defaults
Previous
Next
Help

Apply To: only current, instance
Show: [ ] system [✓] user [✓] CDF

Property	Value	Display
Library Name	UofU_Pads	off
Cell Name	pad_nc	off
View Name	symbol	off
Instance Name	I10	off

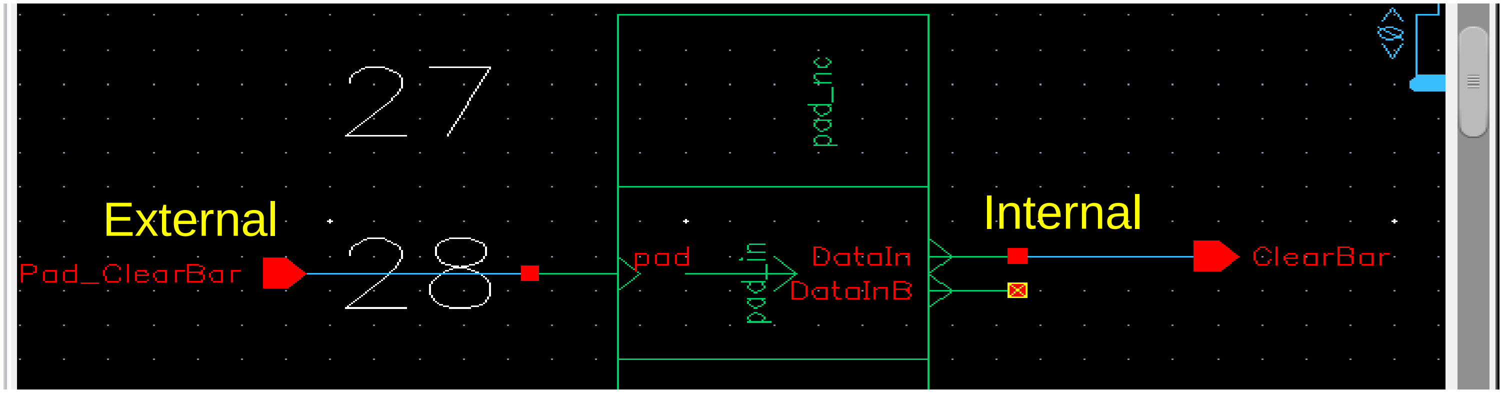
User Property	Master Value	Local Value	Display
interfaceLastCh..	14 13:03:02 2003		off
partName	pad_nc		off
vendorName			off

- Connect wires and pins on outside of frame, representing external connections



Example: pad_in (similar arrangement for pad_out)

- **DataIn** and **DataInB** connect to circuit
- **pad** represents wire-bonding connection
- Use related, but different, pin names (Ex. Pad_ClearBar and ClearBar)



Pad input pin:

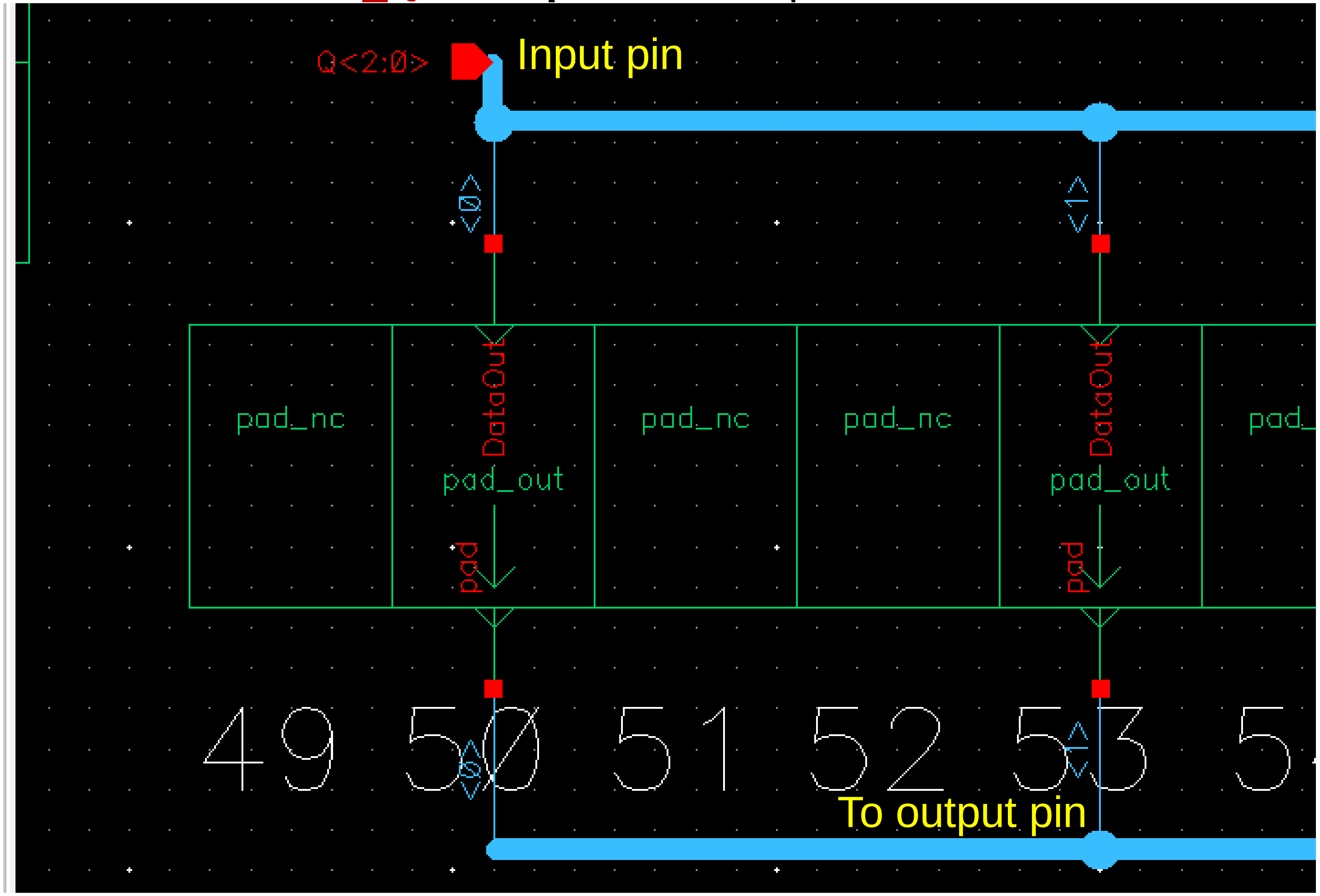
Pad_ClearBar input to Pad will connect to external input.

Pad output pin:

ClearBar output of Pad will connect to ClearBar input of the circuit.
It’s OK to leave one of these unconnected.

Q<2:0> bundle connects to **pad_out** inputs.
Add labels <0> <1> etc. to individual wires connected to the pins.

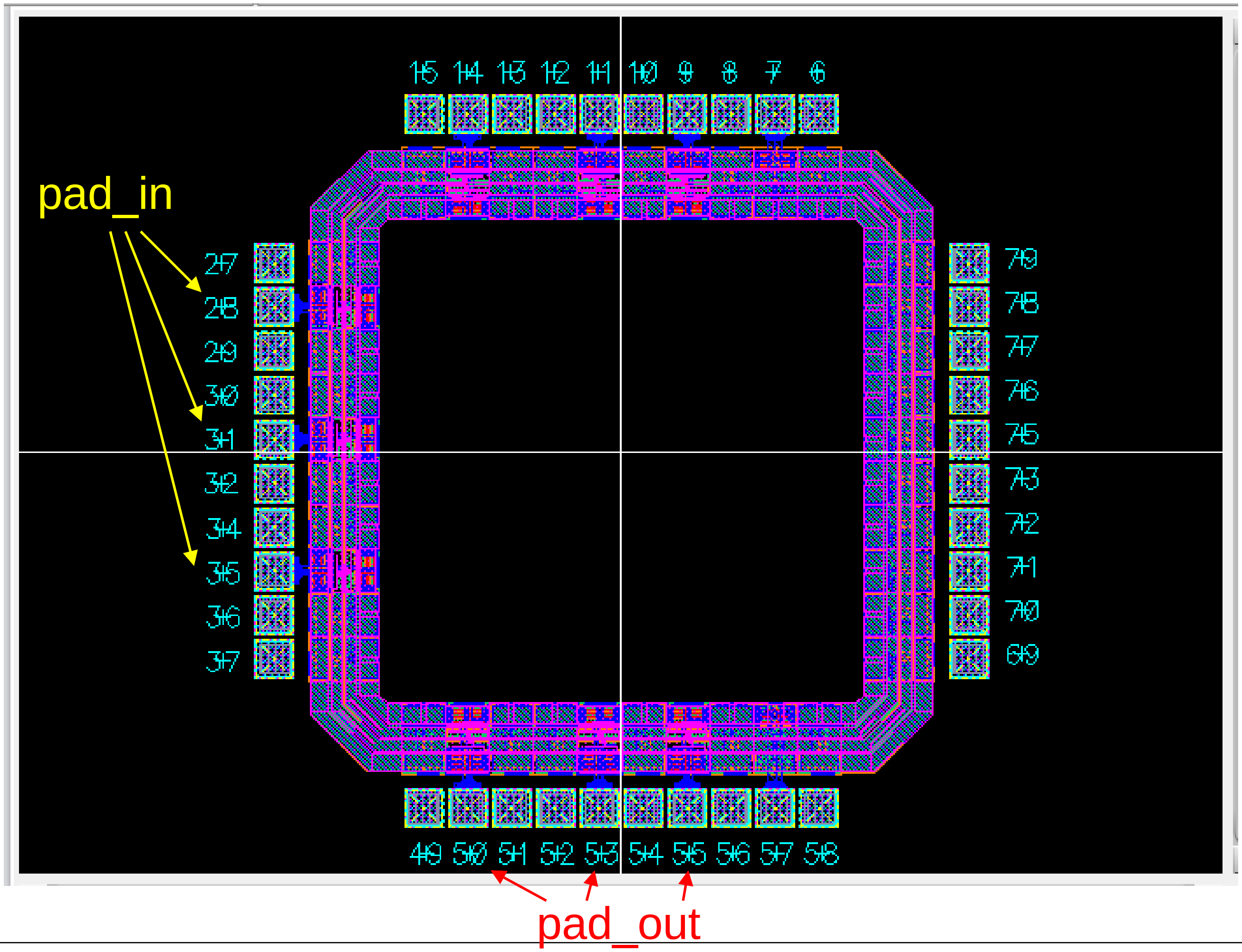
Likewise for Pad_Q<2:0> **pad_out** output bundle below.



Check and Save

Modify pad frame layout to match schematic

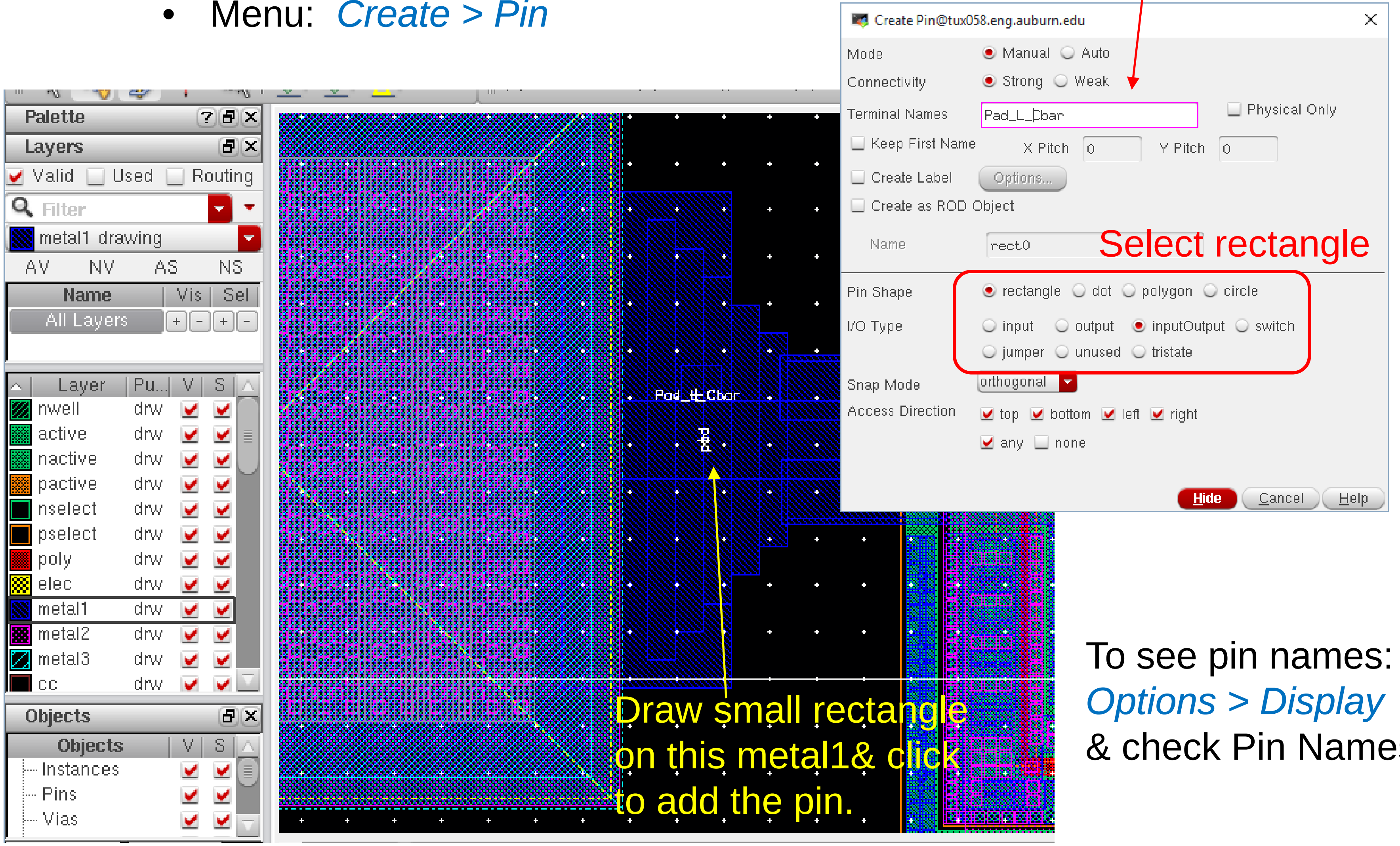
- VDD/GND pads already placed. Other pads are “pad_nc”.
- Select each desired signal pad, open properties, and change Cell from pad_nc to pad_in or pad_out.



Add “pin shapes” to each pad

- Select metal1 in the layer palette
- Zoom in to metal1 next to wire-bond pad
- Menu: *Create > Pin*

Enter Terminal Name



Create Pin@tux058.eng.auburn.edu

Mode [✓ Manual] Auto
Connectivity [✓ Strong] Weak
Terminal Names: Pad_L_Cbar   Physical Only
Keep First Name   X Pitch 0   Y Pitch 0
Create Label   Options...
Create as ROD Object
Name rect0

Select rectangle

Pin Shape [✓ rectangle] dot polygon circle
I/O Type input output [✓ inputOutput] switch jumper unused tristate
Snap Mode orthogonal
Access Direction ✓ top ✓ bottom ✓ left ✓ right ✓ any none

✓ Valid Used Routing
metal1 drawing

Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓

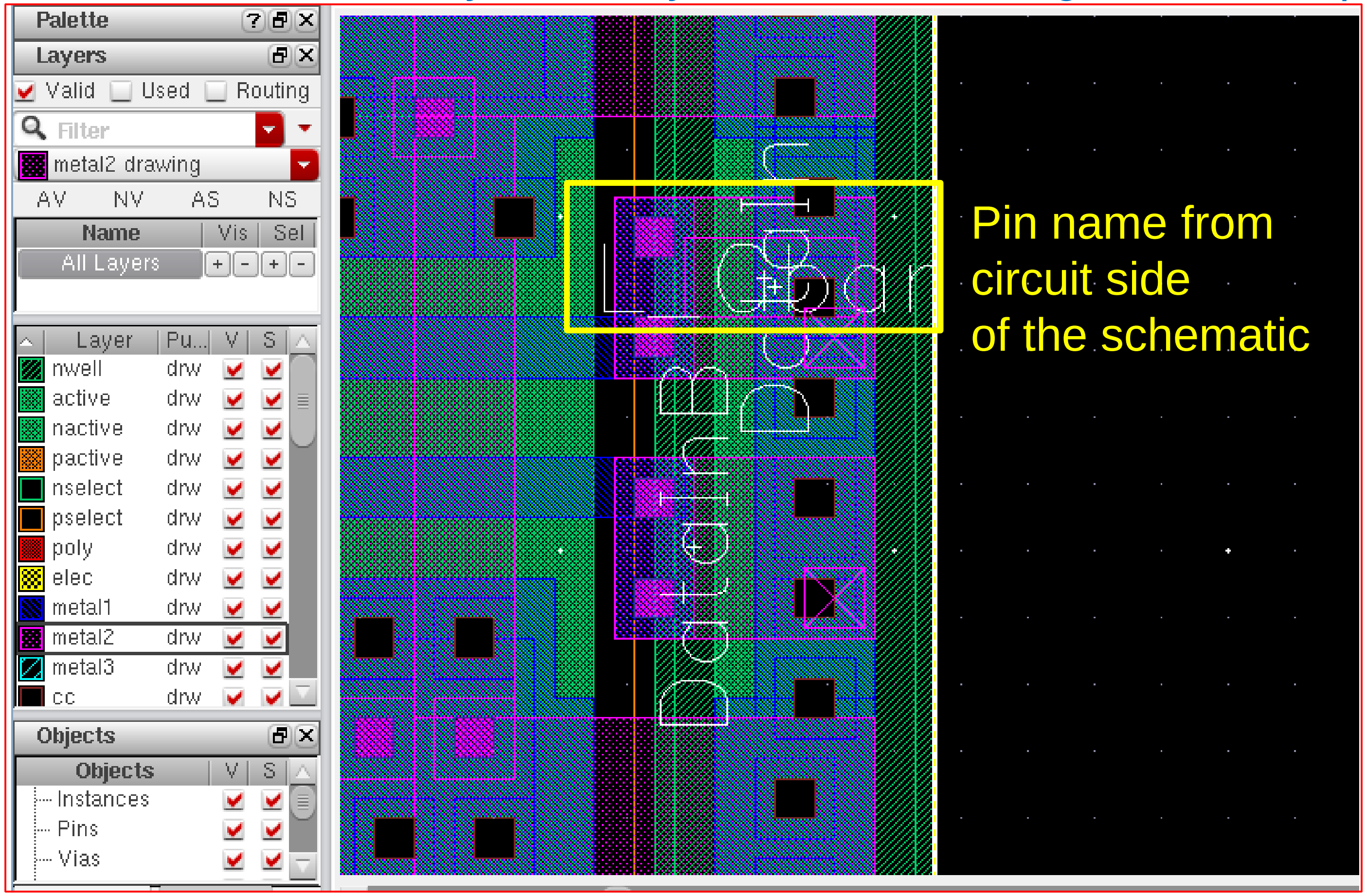
Objects	V	S
Instances	✓	✓
Pins	✓	✓
Vias	✓	✓

Draw small rectangle on this metal1& click to add the pin.

To see pin names: *Options > Display* & check Pin Names

Also add pin shape on metal 2 for connections to circuit block.

- Select metal2 in the layer palette
- Zoom in to metal2 pin on inside of pad frame: DataIn or DataInB or DataOut
- Menu: *Create > Pin (as on previous slide)*
  - Make sure you draw your metal2 rectangle within the pin area



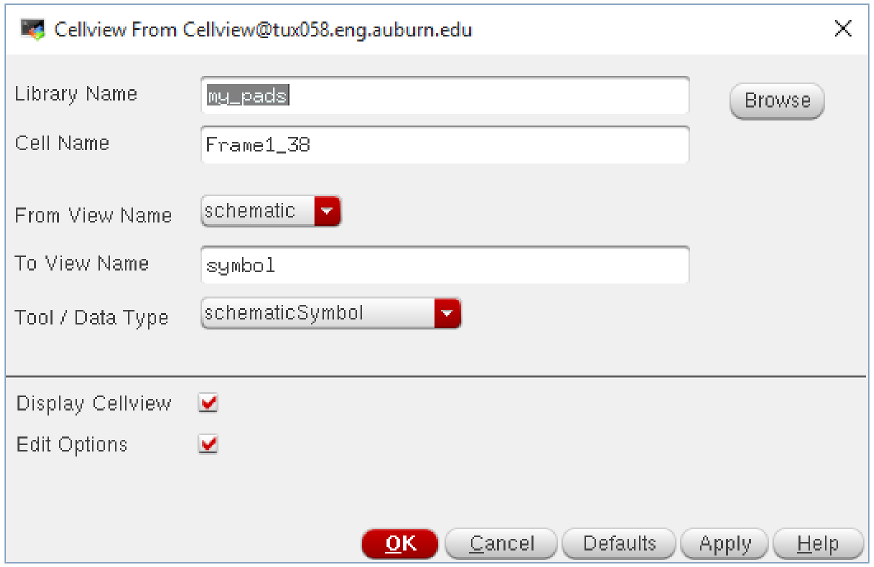
Layer	Pu...	V	S
nwell	drw	✓	✓
active	drw	✓	✓
nactive	drw	✓	✓
pactive	drw	✓	✓
nselect	drw	✓	✓
pselect	drw	✓	✓
poly	drw	✓	✓
elec	drw	✓	✓
metal1	drw	✓	✓
metal2	drw	✓	✓
metal3	drw	✓	✓
cc	drw	✓	✓

DRC and Save

Create a symbol view of the pad frame

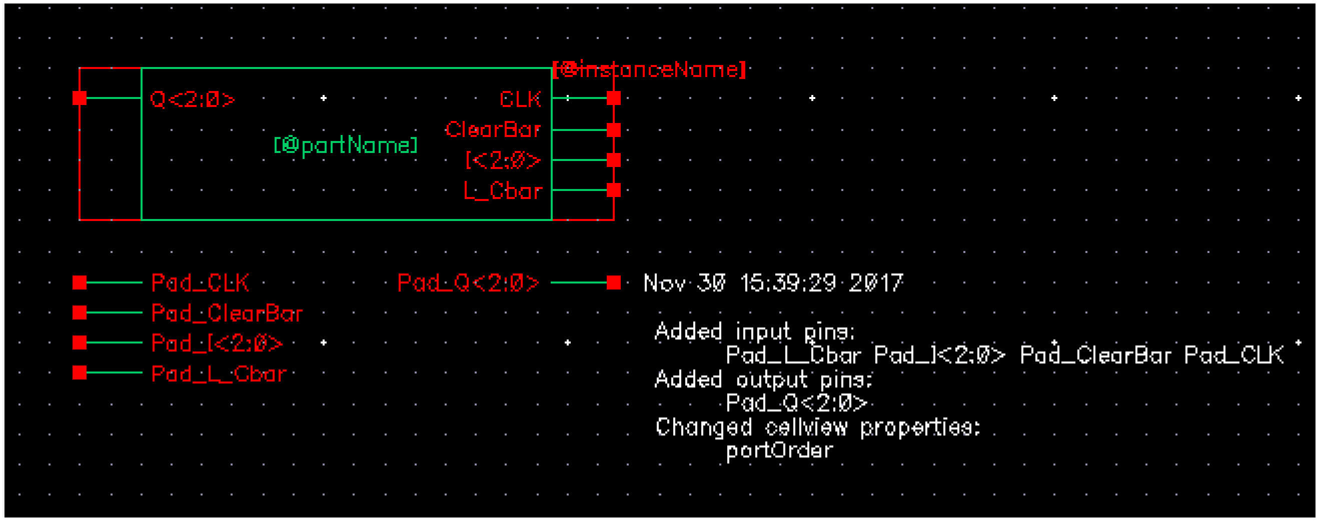
In the schematic window:

Create > Cell View > From Cellview



Cellview From Cellview@tux058.eng.auburn.edu

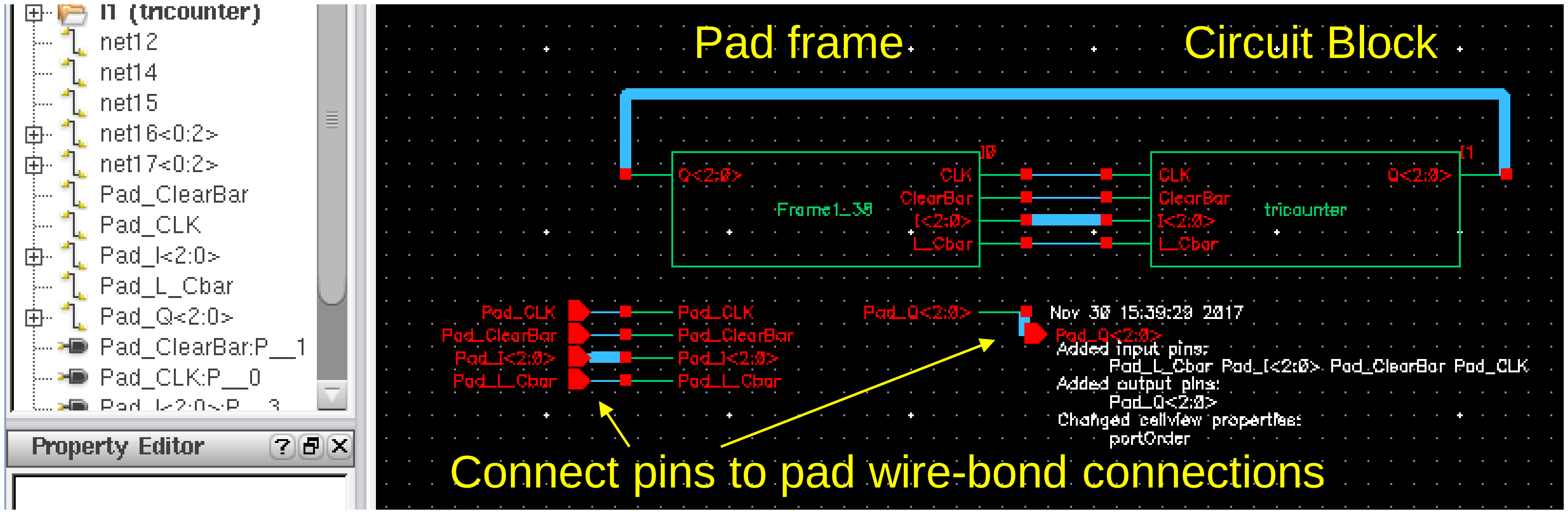
Library Name	my_pads
Cell Name	Frame1_38
From View Name	schematic
To View Name	symbol
Tool / Data Type	schematicSymbol
Display Cellview	✓
Edit Options	✓



```
Nov 30 15:39:29 2017

 Added input pins:
        Pad_L_Cbar Pad_I<2:0> Pad_ClearBar Pad_CLK
 Added output pins:
        Pad_Q<2:0>
 Changed cellview properties:
        portOrder
```

Create a new schematic connecting circuit block to pad frame



```
Nov 30 15:39:28 2017
Added input pins:
        Pad_L_Cbar Pad_I<2:0> Pad_ClearBar Pad_CLK
Added output pins:
        Pad_Q<2:0>
Changed cellview properties:
        portOrder
```

- Check and Save
- Create layout from schematic: Launch > Layout GXL
  Similar to creating block layout from its schematic, except for I/O pins. (see next slide)

Create chip layout from the chip schematic

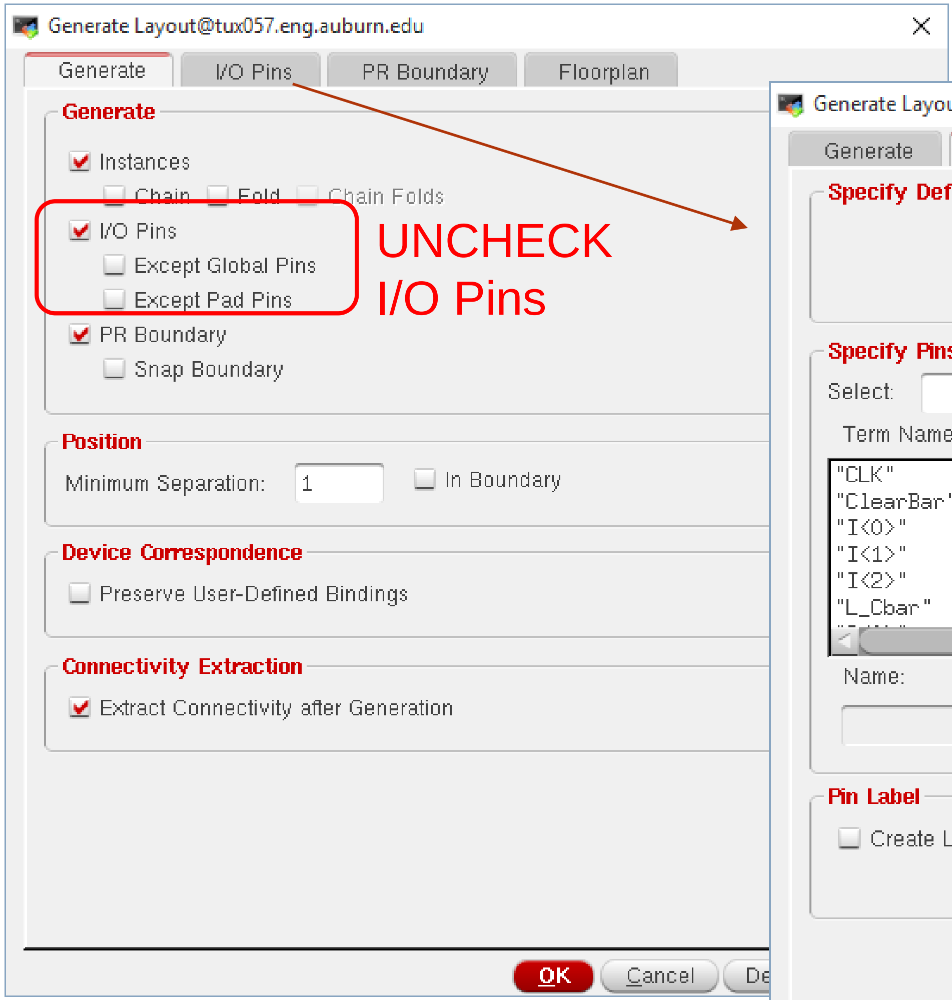
- Launch > Layout GXL from the schematic window

From Layout Menu:
Connectivity > Layout GXL

Or click icon in bottom left corner:

Select all pad pins, UNcheck "Create", & Apply

UNCHECK I/O Pins


Generate Layout@tux057.eng.auburn.edu

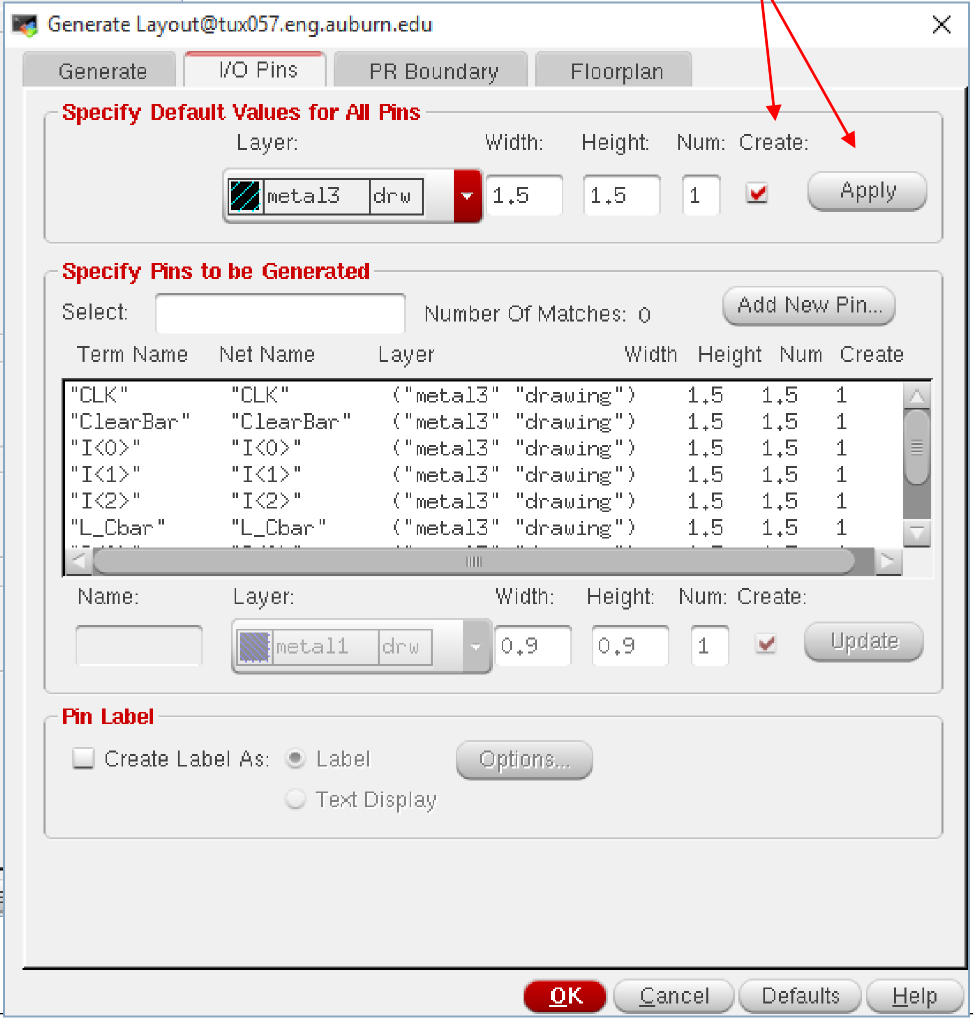
Tabs: Generate | I/O Pins | PR Boundary | Floorplan

Generate
- [✓] Instances
  - [ ] Chain [ ] Fold [ ] Chain Folds
- [✓] I/O Pins
  - [ ] Except Global Pins
  - [ ] Except Pad Pins
- [✓] PR Boundary
  - [ ] Snap Boundary

Position
Minimum Separation: 1 [ ] In Boundary

Device Correspondence
[ ] Preserve User-Defined Bindings

Connectivity Extraction
[✓] Extract Connectivity after Generation


Generate Layout@tux057.eng.auburn.edu

Tabs: Generate | I/O Pins | PR Boundary | Floorplan

Specify Default Values for All Pins

Layer:	Width:	Height:	Num:	Create:
metal3 drw	1.5	1.5	1	✓

Specify Pins to be Generated
Select: Number Of Matches: 0 Add New Pin...

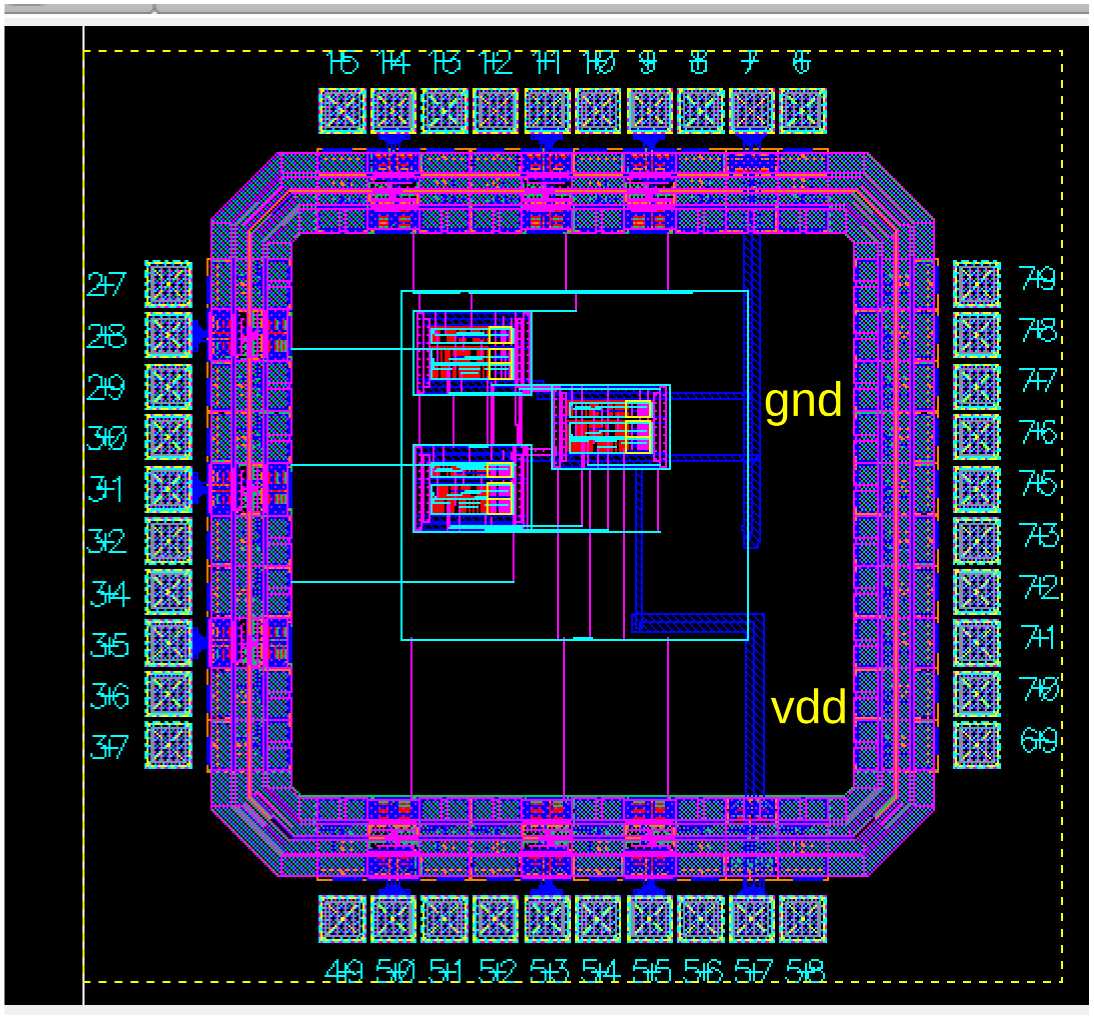
Term Name	Net Name	Layer	Width	Height	Num	Create
"CLK"	"CLK"	("metal3" "drawing")	1.5	1.5	1	
"ClearBar"	"ClearBar"	("metal3" "drawing")	1.5	1.5	1	
"I<0>"	"I<0>"	("metal3" "drawing")	1.5	1.5	1	
"I<1>"	"I<1>"	("metal3" "drawing")	1.5	1.5	1	
"I<2>"	"I<2>"	("metal3" "drawing")	1.5	1.5	1	
"L_Cbar"	"L_Cbar"	("metal3" "drawing")	1.5	1.5	1	

Name:	Layer:	Width:	Height:	Num:	Create:
	metal1 drw	0.9	0.9	1	✓

Pin Label
[ ] Create Label As: (● Label) ○ Text Display

Complete the chip layout

- Move pad frame into prBoundary
- Move and position circuit block within the pad frame cavity



- Draw VDD/GND wires (metal1) from pads to pad rings of blocks (make width about 3x that of pad ring wires)
- Autoroute signal wires
- DRC/LVS
- Save

Placement of frame and core

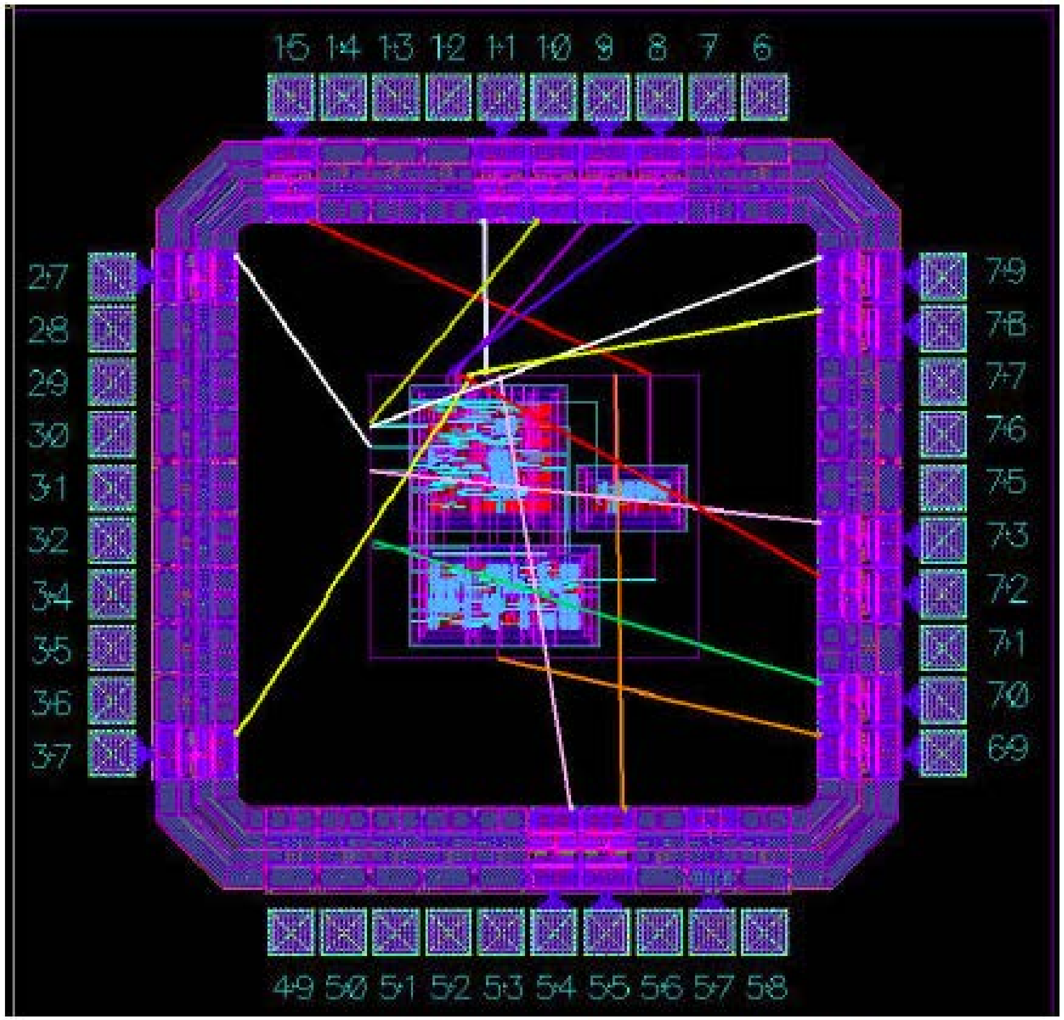


Figure 12.19: Frame and core placed in *Virtuoso-XL*

From
E. Brunvand
Book

Power/ground routed manually

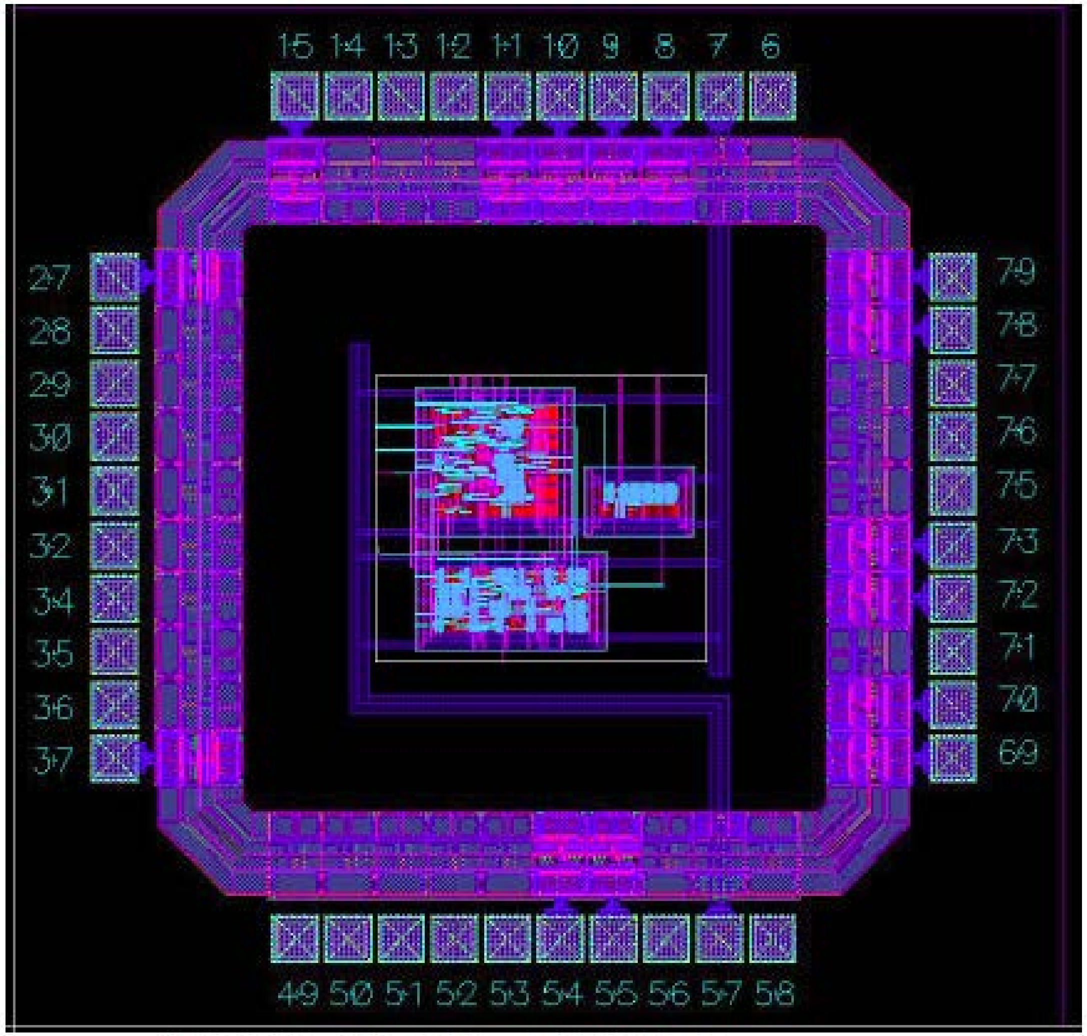
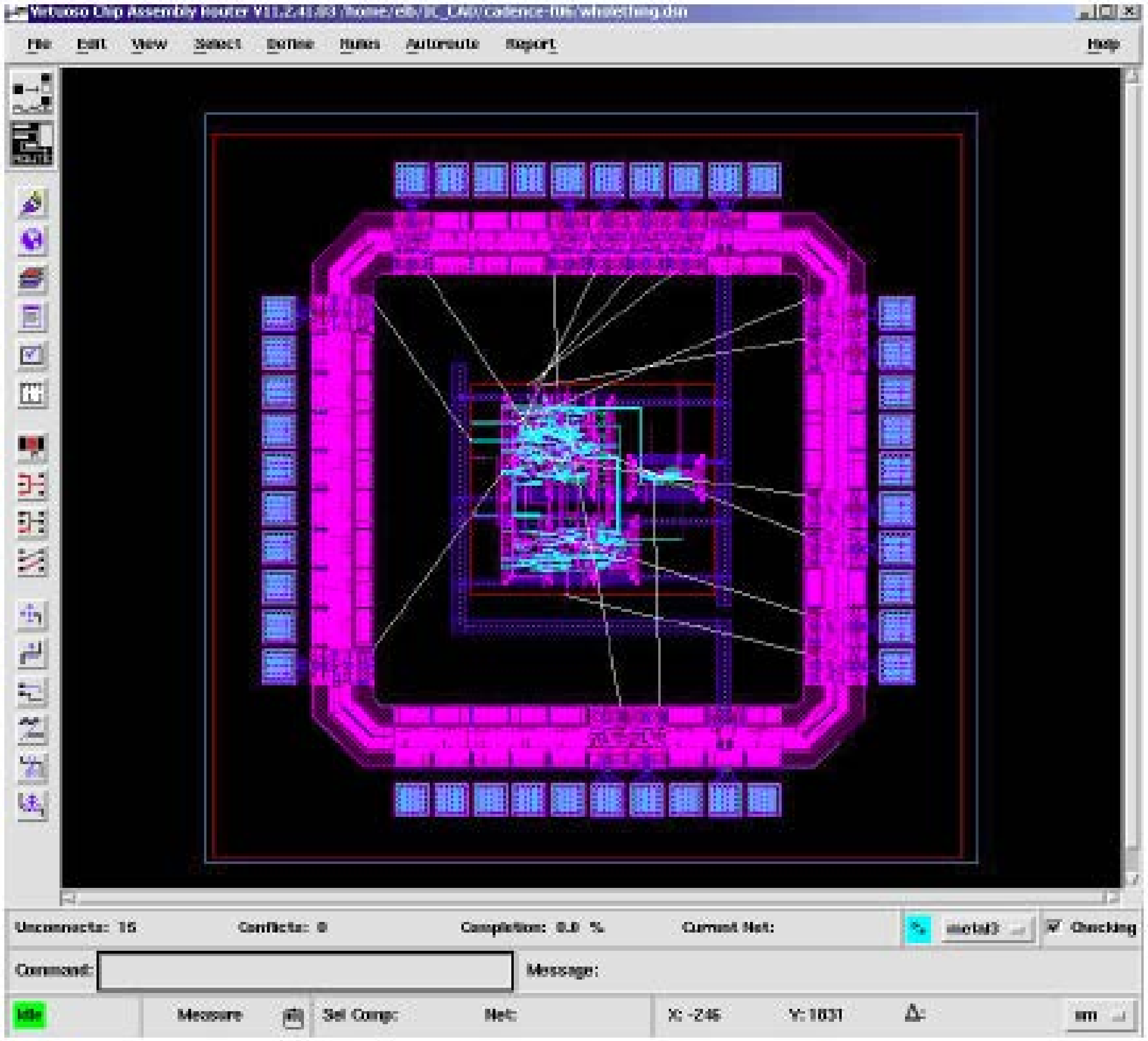


Figure 12.20: Frame and core placed in *Virtuoso-XL* with **vdd** and **gnd** routing completed

From
E. Brunvand
Book

Before signal routing


Virtuoso Chip Assembly Router V11.2.41.83 /home/elb/IC_CAD/cadence-f06/wholething.dsn
File
Edit
View
Select
Define
Rules
Autoroute
Report
Help

Unconnects: 15 Conflicts: 0 Completion: 0.0 % Current Net: metal3 ☑ Checking

Command: Message:

Idle Measure Sel Comp: Net: X: -246 Y: 1831 Δ: um

Figure 12.21: Frame and core before routing in *ccar*

From
E. Brunvand
Book

After signal routing

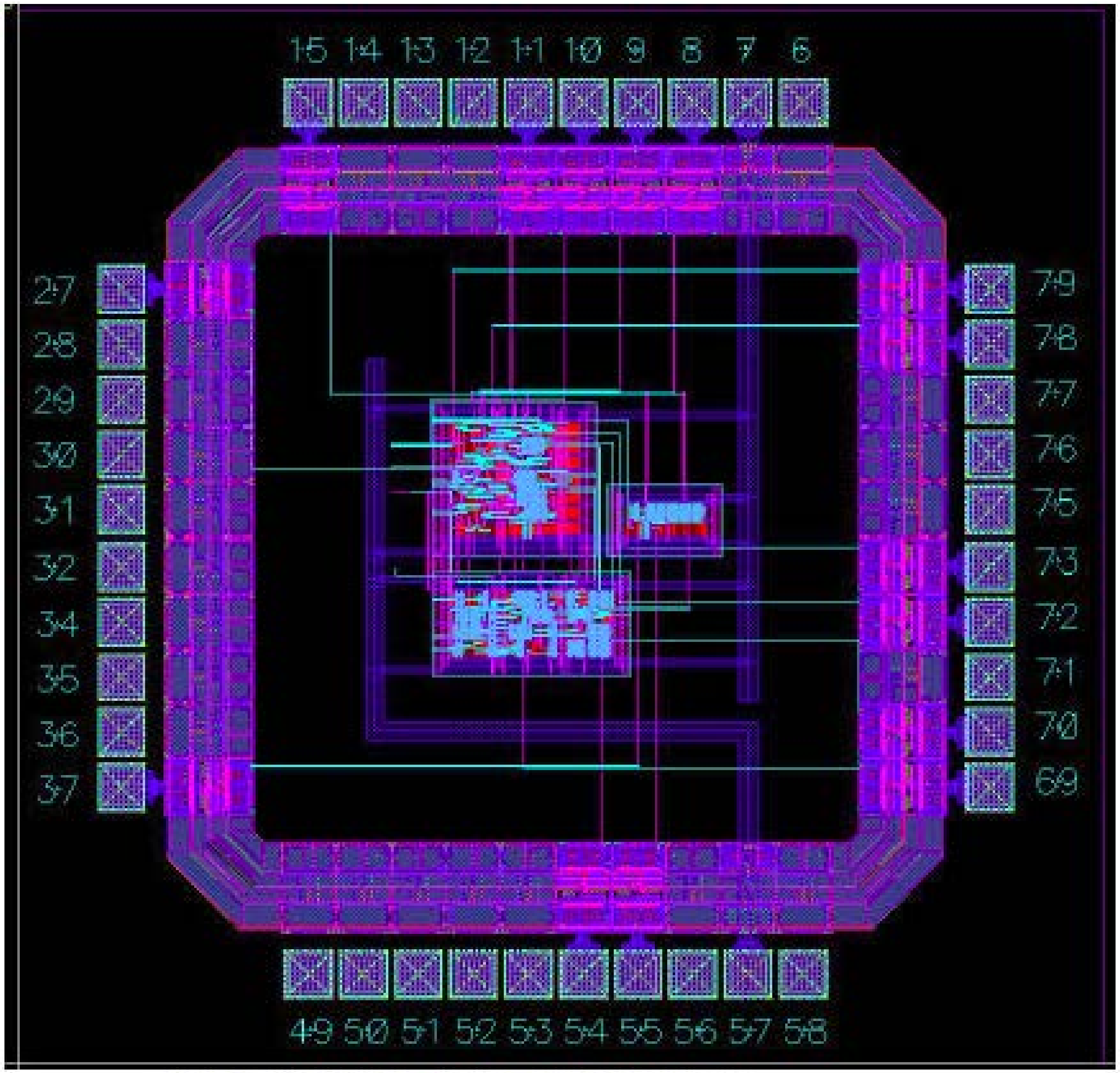


Figure 12.22: Frame and core after routing in *Virtuoso*

From
E. Brunvand
Book