ELEC 5250/6250 – Homework Project 2

In Project 1, you manually designed a gate-level structural model of a modulo-6 counter. Now we want to (1) verify its correctness through simulation, (2) develop a behavioral model of the counter, which is where we would normally begin the design process, and (3) compare your hand-designed gate-level circuit with one that you will synthesize later from the behavioral model using the Synopsys Design Compiler. So, in this project you are to write **two Verilog models**.

Model 1

Design a **dataflow** model of your modulo-6 counter from Project 1. This model should have a single Verilog module, with no instantiations of lower-level modules. You may model the functionality of the counter using the logic equations that you derived in Project 1, or you may use Verilog primitive gates to represent the circuit that you derived in Project 1. Since Verilog primitive gates do not include flip flops, you will need a procedural block (always block) to model those.

Model 2

Design a **behavioral** model of the modulo-6 counter you designed in Project 1. The model should have a single Verilog module, and should not instantiate any lower-level modules. Since this is a behavioral model, it should not contain logic equations or primitive gates, since these would normally be produced during synthesis. The inputs/outputs and the function are to be identical to those of Model 1 and the hand-designed circuit.

Homework Deliverables

Submit printouts of the two Verilog models and a copy of your hand-designed circuit from Project 1. We will simulate the two models in the next assignment.

Use comments throughout your design to help the instructor understand your models.