VLSI Design and Test Seminar

"Specification Test Minimization for Given Defect Level"

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An accepted industry practice for testing of analog and RF circuits is to use specification-based tests. These tests are capable of providing a very low defect level but tend to be long and costly. In this work, we focus on minimizing the specification-based tests without exceeding any specified defect level. We use Monte Carlo simulation to determine the probabilities with which a test covers specifications it was not originally intended to cover. These probabilities and the given defect level then define an integer linear programming (ILP) model for eliminating unnecessary tests. Two examples provide evidence of successful implementation of the proposed methodology. First, a hypothetical case of ten specifications illustrates that depending upon the defect level requirement, up to half of the tests may be eliminated. Monte Carlo simulation using spice for probabilistic characterization of tests versus specifications of a commercially available operational amplifier circuit is then presented. This talk is based on a forthcoming paper, S. Sindia and V. D. Agrawal, “Specification Test Minimization for Given Defect Level,” 15th IEEE Latin American Test Workshop, Fortaleza, Brazil, March 12-14, 2014.