Fault Injection for FPGA Testing on the ADVANTEST T2000

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Abstract:

The basic scope of this project is the insertion and testability of synthesized faults into a programmed FPGA. The Advantest T2000 tester uses its own proprietary software for the execution and analysis of test programs. The objective of the project is to provide a simulation of faults or errors on the field programmable gate array (FPGA) that are analogous to the random defects that can occur on a chip from the micro fabrication process. Utilizing the functions of the ISE Design tools, Object Oriented programming and the Advantest T2000 Tester, designs can be re-configured to emulate and then simulate faults. A single defect could ruin the functionality of a chip and designing for testability ensures that a designer can detect the defaults that are present in any circuit. Any designer has to be sure that their device, when fabricated, is fault free before it is shipped to the consumer.