Better Than Worst Case Timing Design With Latch Buffers On Short Paths

Ravi Kanth Uppu, Ravi Tej Uppu & Adit D. Singh
Auburn University

Professor Ilia Polian
University of Passau, Germany

Abstract—Better-than-worst-case timing designs such as Razor introduce shadow flip-flops triggered by a delayed clock in parallel to the functional flip-flops for timing error detection through duplication and comparison. This arrangement suffers from the "short path" problem, whereby the activation of paths shorter than this timing skew can cause false errors to be flagged. The traditional solution is to add buffers to the short paths that are less than the clock skew between the duplicated error detection flip-flops. However, this approach adds considerable area and power overhead, particularly in the presence of significant process variations. This paper studies the use of latches to introduce extra delay on short paths. Holding short paths stable for the first phase of the clock allows the design to achieve a skew of half a clock period between the functional and shadow flip-flops without short path errors. We present a method that characterizes all the path groups and places latches in appropriate path segments of the circuit to ensure that all short paths driving duplicated flip flops are delayed by half a clock cycle. Unit delay simulations for benchmark designs with and without process variations are presented. Average performance improvement (API) and best case performance improvement (BPI) for designs are presented with an overall average performance improvement of about 15% and best case performance improvement of 32% at a cost of acceptable area overhead.