ELEC 5250_6250 Project #6
Due: Tuesday, October 15, 2018, 11:00 am

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.
ELEC 6250 Students: Do this assignment with the divider circuit.

Submit the report for this project as a file attached to an email message.

In this exercise, timing characteristics of a post-synthesis netlist will be studied and verified in *Synopsys Design Compiler (DC)* and *Modelsim*. The following parameters are to be determined and verified, as if you were preparing a datasheet for your circuit.

1. The minimum clock period/maximum clock frequency for reliable operation. This should be determined from the longest reported delay path from a clock transition to all flip flop inputs stable, added to flip flop setup time. (If you set a clock period constraint, this should be the path with the worst "slack".)
2. The worst case setup time for the circuit inputs (the external inputs to the counter or divider). This should be the worst case (longest) propagation delay from a circuit input pin to the flip-flop D inputs, including flip flop setup time.
3. The worst case delay from a clock transition to a circuit output pin (one of the external outputs of the counter or divider), i.e. the output arrival time.

Perform the following steps:

A. Determine the three parameters described above from a *DC* static timing analysis (delay) report.

B. Verify items 1, 2 and 3 above by simulating the synthesized netlist with its standard delay format (SDF) file in *Modelsim*, and measuring the parameters of interest in the simulation list window.
   a. **Use a list window (not a wave window) and highlight the significant delays on the printed listing.**
   b. **"Edit" the listing to save paper, printing only the lines of the list window that show the events and time parameters of interest.**
   c. Note that this requires determining the end points of the three worst case paths identified above, displaying these signals in the simulation list window, and executing an appropriate test sequence to exercise these paths.
   d. You may use either a testbench or a macro file to drive the simulation.

C. Report the parameters from items 1-2-3 in a table, listing the values predicted by *DC* in one column, and the values observed in the simulation list window in a second column.

D. Re-verify item 1 by **purposely creating violations** of at least one flip flop setup time. Violations should be reported in a message window. Print the lines from the simulation list window showing these violations, plus the generated messages. (Don't print the entire simulation list window.)