

# ELEC 5250/6250 Homework Project 1 (Digital logic prerequisite review.)

**Due: Friday, 8/24/2018**

## PART 1

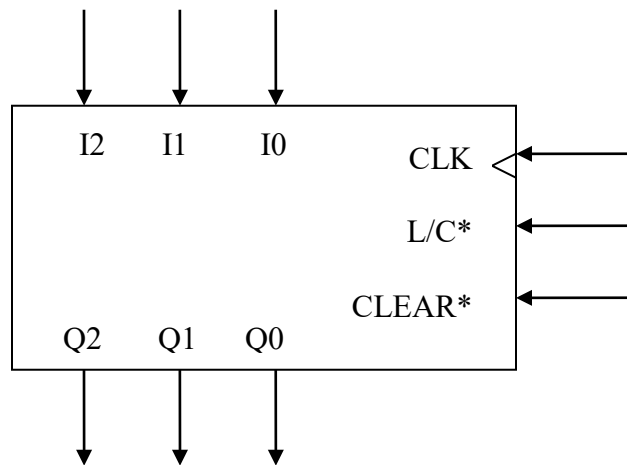
Design a *digital modulo-6 counter* with the following characteristics:

- Three output bits: Q2,Q1,Q0
- Synchronous count: count up on the rising edge of a clock (CLK)
- Synchronous load: load external inputs (I2,I1,I0) as the new counter state on the rising edge of CLK
- Asynchronous clear: active-low CLEAR\* signal forces the counter state to 000

The input/output signals are as follows:

CLK : active-high clock input  
CLEAR\* : active-low clear input  
L/C\* : high to select load, low to select count  
I2,I1,I0 : parallel data inputs  
Q2,Q1,Q0 : parallel data outputs

Your design must use D flip flops and simple logic gates, with the circuit minimized as much as possible. Submit your final schematic diagram and your design work.



## PART 2

Describe how you would test your counter design.

- What input values will you apply in each clock cycle of the test, and what output values would you expect?

- Indicated the reason for selecting each input pattern (what aspect of the counter design is to be tested?)