ELEC 5200/6200 (Fall 2013)

Homework 4 Problems (Pipelined design)
Assigned 10/11/13, due Wednesday, 10/16/13

Problem 1: Suppose for a computer, T_m is the time required for reading or writing the memory, T_f is the time for reading or writing the register file, T_a is the critical path delay of ALU or adder circuit and T_r is the clock to Q delay of all registers. Derive lower bounds on the cycle times for single-cycle, multicycle and pipeline MIPS datapaths.

Problem 2: Assume that each pipeline register and the program counter have a delay of 20ps. Times taken by other major hardware units in a MIPS processor are:

Memory read or write	100ps
Register file read and write	50ps
ALU	130ps
Add unit	100ps

All other hardware, including the control and multiplexers, has negligible delays. Then,

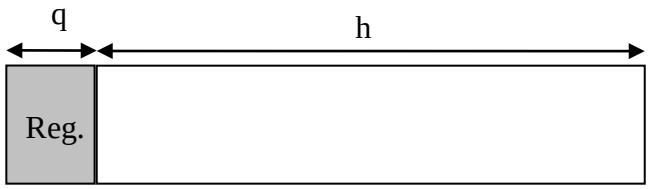
a. What is the maximum clock frequency for a five-stage MIPS pipeline datapath?

b. Neglecting any hazards and resulting stalls, what are the pipeline latency and the cycles per instruction (CPI) for a long instruction sequence?

c. Compare this datapath with a single cycle datapath:

Datapath	Clock cycle time	Clock frequency	CPI	Time per instruction	Million instructions per second (mips)
Single-cycle					
Pipeline					

Problem 3: Consider a single-cycle datapath as a one-stage pipeline. It consists of combinational and asynchronous circuitry and a single clocked register, the program counter. Its total cycle time consists of an interval q required by the register and an interval h used by the rest of the circuitry:



(a) Assume that the hardware delay h can be partitioned into n equal stages separated by clocked registers each having delay q, the first stage register being the program counter. Neglecting the latency and any hazard penalties, compute the execution time of an instruction by this n-stage pipeline.

(b) Show that the performance limit for the pipeline when we neglect the latency and hazards is determined by the register delay q. Find an upper bound for the clock frequency of this pipeline datapath.

(c) For an n-stage pipeline, suppose the average hazard penalty is $\alpha(n - 1)$ cycles per instruction, where $0 < \alpha < 1.0$ and $n \geq 1$. Find the optimum number of pipeline stages.

(d) For a hardware design it is estimated that $h = 9 \times q$ and for the ISA, $\alpha \approx 0.2$, what is the optimum number of stages for this pipeline and what is the corresponding speed up over a single-cycle datapath?

(e) For q = 50ps, tabulate clock cycle time, clock rate, average CPI and performance in million instructions per second for single-cycle datapath and the pipeline datapath with optimum number of stages found in (d).

Problem 4:

(a) Does a five stage MIPS pipeline execution of the following sequence of instructions generate a hazard? If yes, what type of hazard is it?

```
sub   $s0, $t0, $t1
sub   $t2, $s0, $t3
```

(b) If the instruction stream in (a) generates a hazard, could it be handled without a pipeline stall? Illustrate the handling of hazard by a sketch of pipeline stages.

Problem 5: Consider the following MIPS instruction sequence being executed on a five-stage pipeline:

```
sw    $6, 0($7)          # Mem[$7] = $6
lw    $8, 0($7)          # $8 = Mem[$7]
add   $9, $8, $2         # $9 = $8 + $2
```

(a) Will there be a hazard generated? If yes, what kind?
(b) If a hazard is generated how will the hardware handle it? Will there be a performance penalty?
(c) How can an intelligent compiler improve the code?