

Run-Time Content Editable Memory using MegaWizard Plug-In Manager

Note: Before you start with this tutorial it is important to go through tutorial 'Altera Quartus II and DE2 manual' available on course website.

1. To start creating the memory module, go to Tools -> MegaWizard Plug-In Manager. And click on "Create a new custom megafunction variation" as shown in Fig 1. Then click Next.

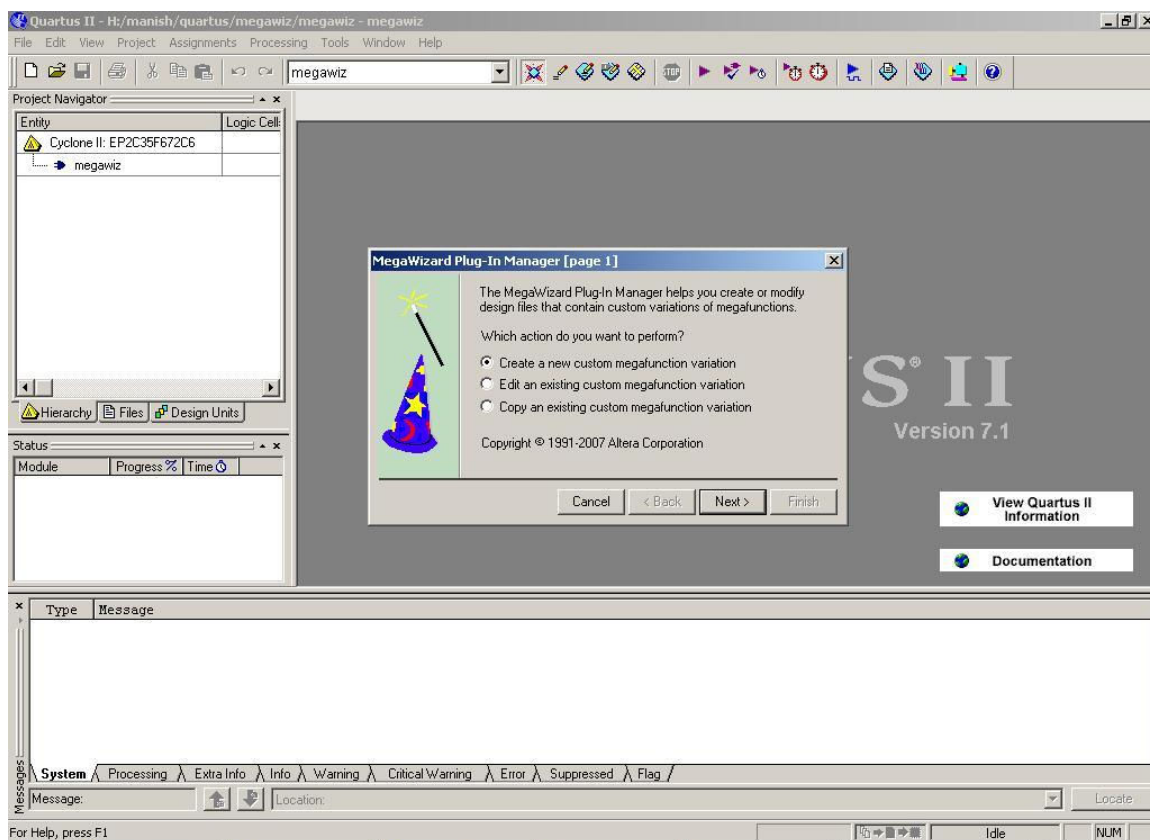


Fig. 1

- On the 2nd page select the device family “Cyclone II”. On the left hand side under the name memory compilers choose RAM: 1-PORT module as shown in the Fig 2. Type of output file that needs to be selected is VHDL. And finally name your output file. Then click Next.

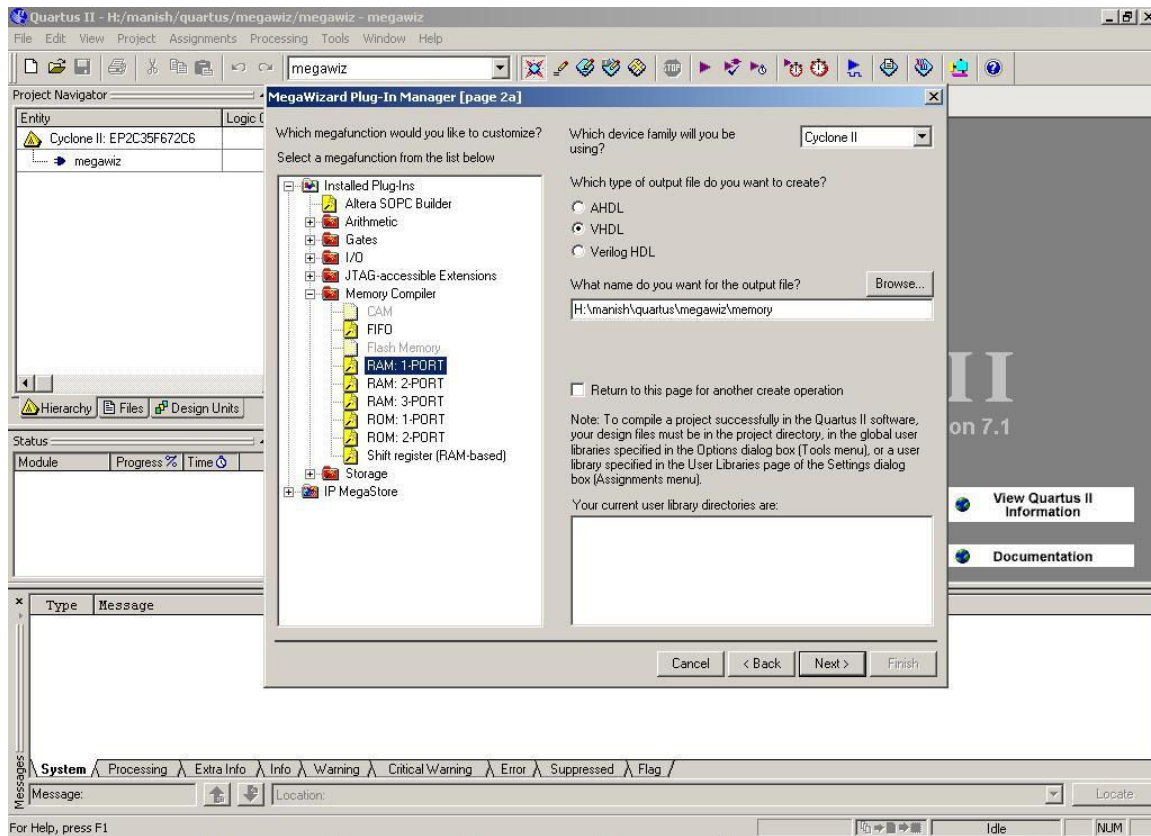


Fig. 2

- On page 3, 'q' output bus should be made 16 bits wide and the number of words can be selected as 8192 as shown in the Fig. 3. The number of words you are going to require depend on the length of your program. Though a 16 bit address line can access $2^{16} = 64K$ locations, we don't need this much memory. Then click "Next".

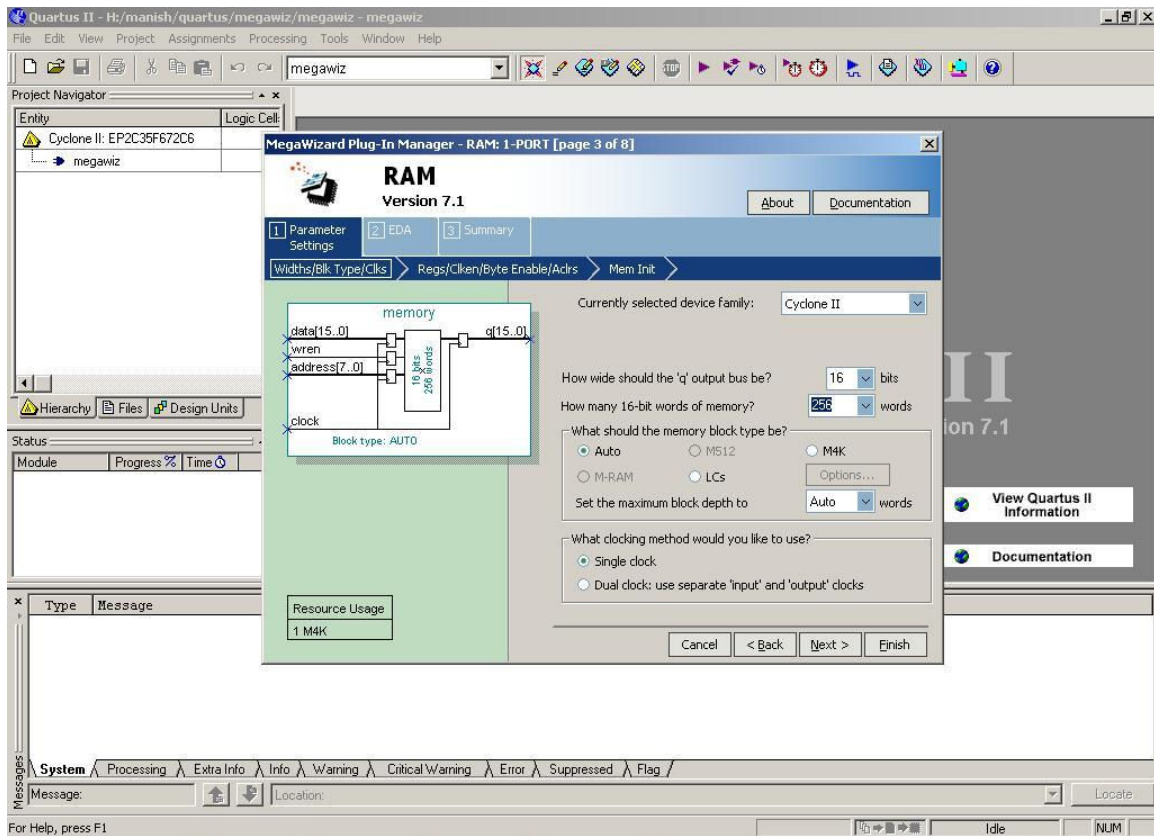


Fig. 3

4. Page 4 will appear as shown in Fig 4 . Uncheck 'q' output port . Click Next.

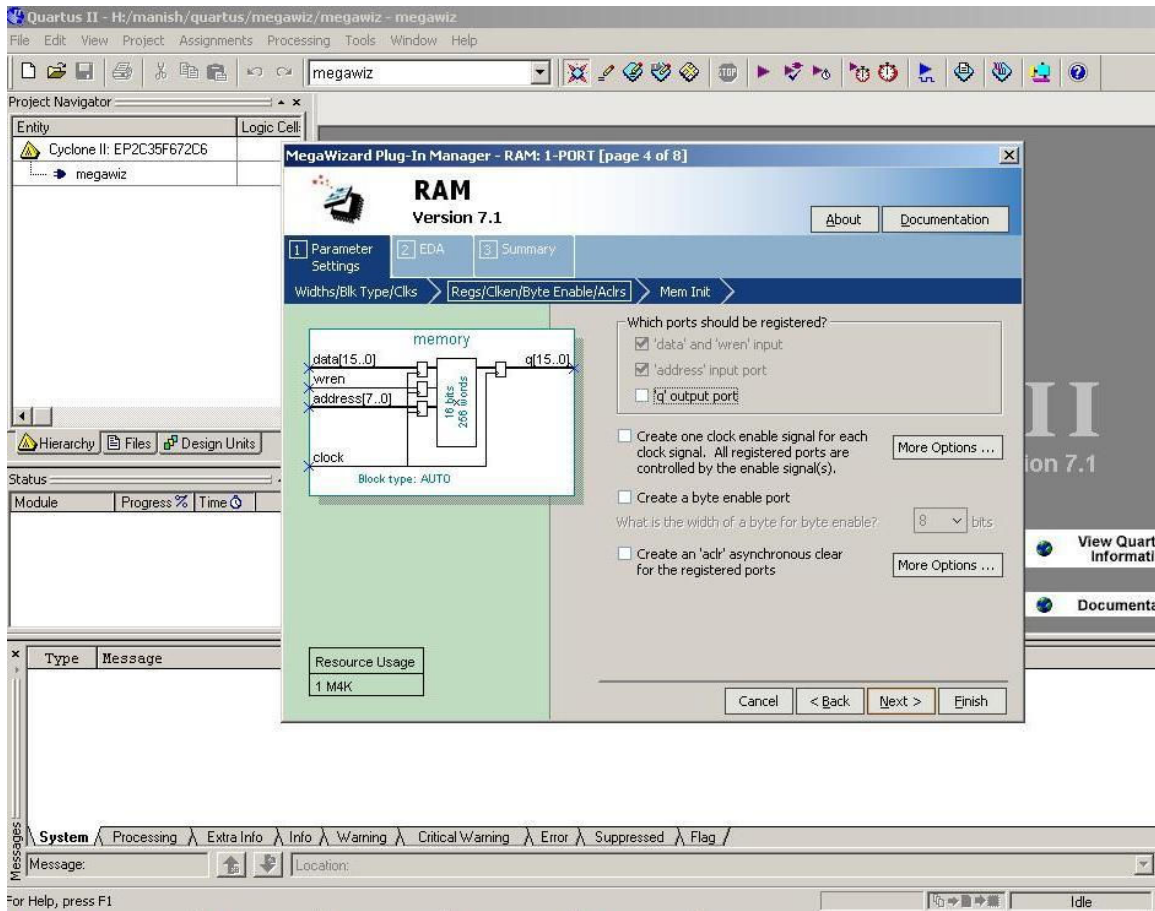


Fig. 4

- To place processor instructions into the memory, you need to specify *initial values* that should be stored in the memory once your circuit has been programmed into the FPGA chip. This can be done by telling the wizard to initialize the memory using the contents of a *memory initialization file (MIF)*. I have specified a file named *RAM_init.mif*, which then has to be saved in the directory that contains the Quartus II project. MIF format is available on course website. Write your MIF File as shown in that format. And click on “Yes, use this file for memory content data” and add your RAM_init.mif file as shown in Fig. 5. Then click Next.

To make the memory contents run-time editable, you need to check box against “Allow in system memory content editor to capture and update content independently of the system clock”. The Instance ID is any 4 digit number like 1234.

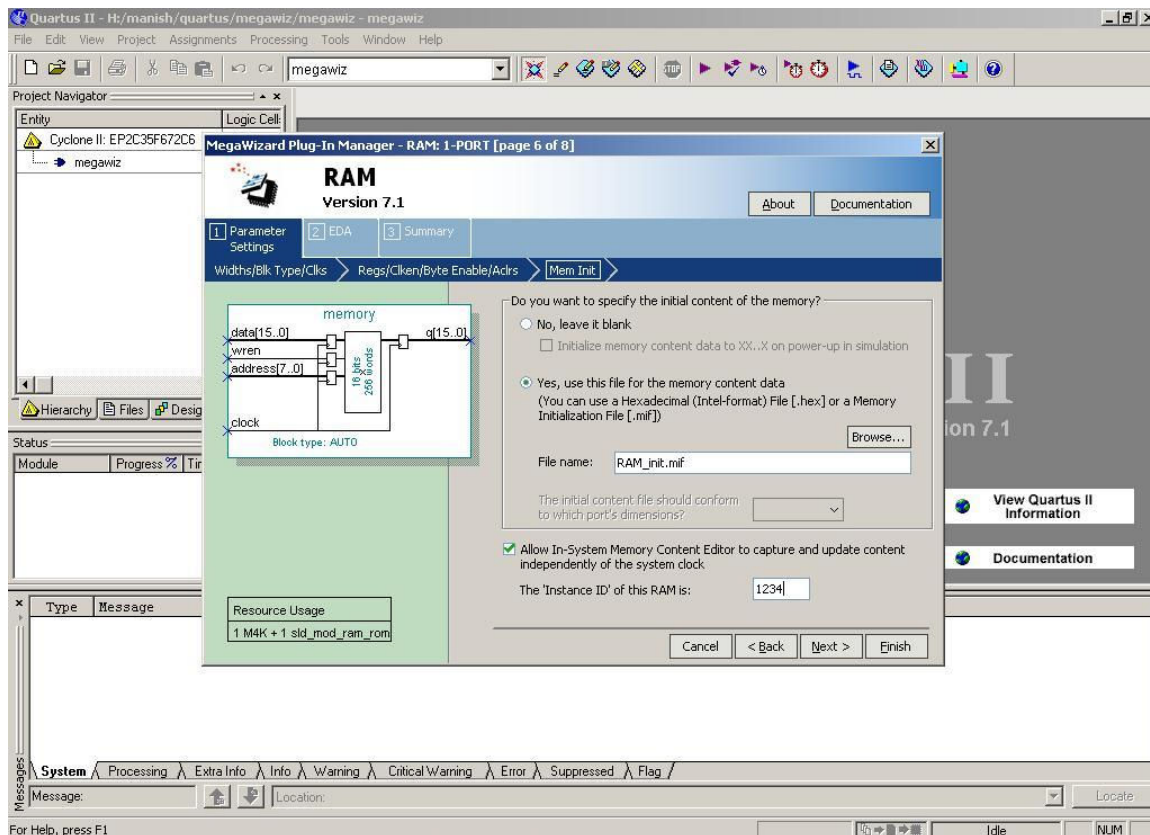


Fig. 5

6. Finally your .vhd file for RAM module will be created in your working directory. Select Next on page 7. (Fig. 6)

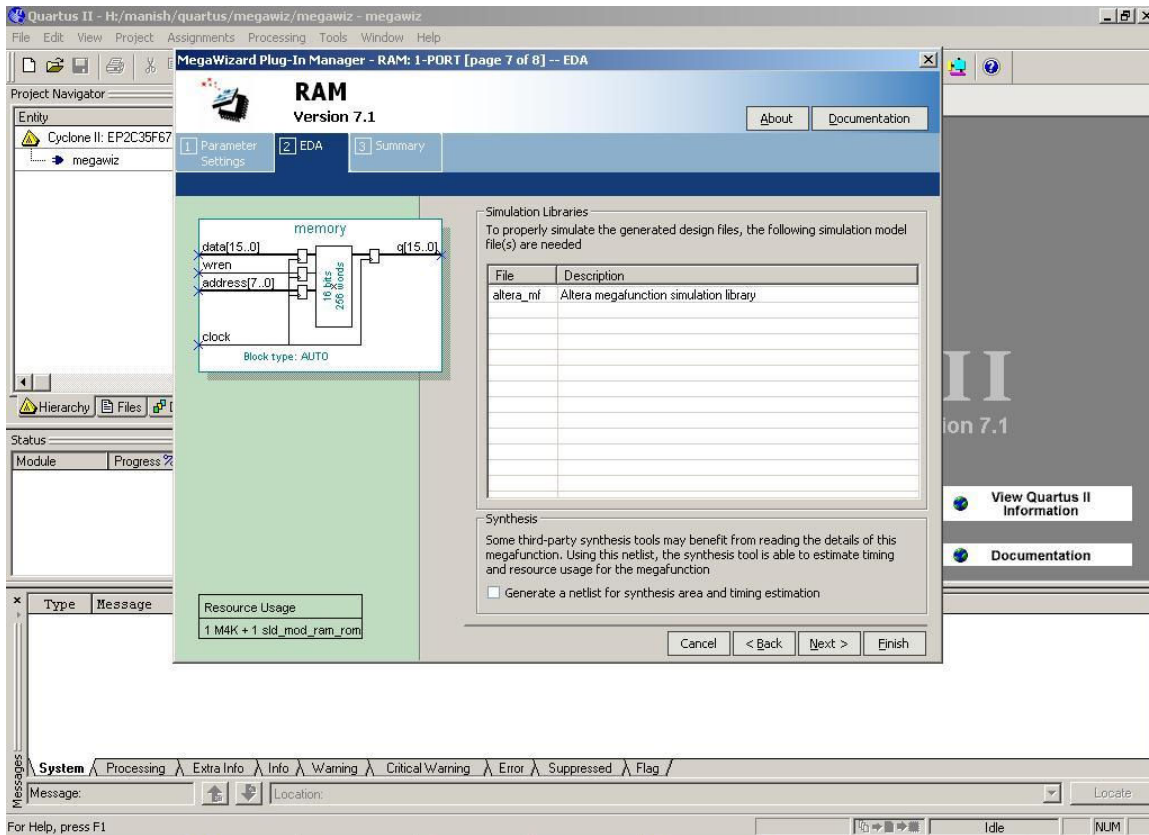


Fig. 6

7. Fig. 7 is a summary of all the files that will be created. Click Next.

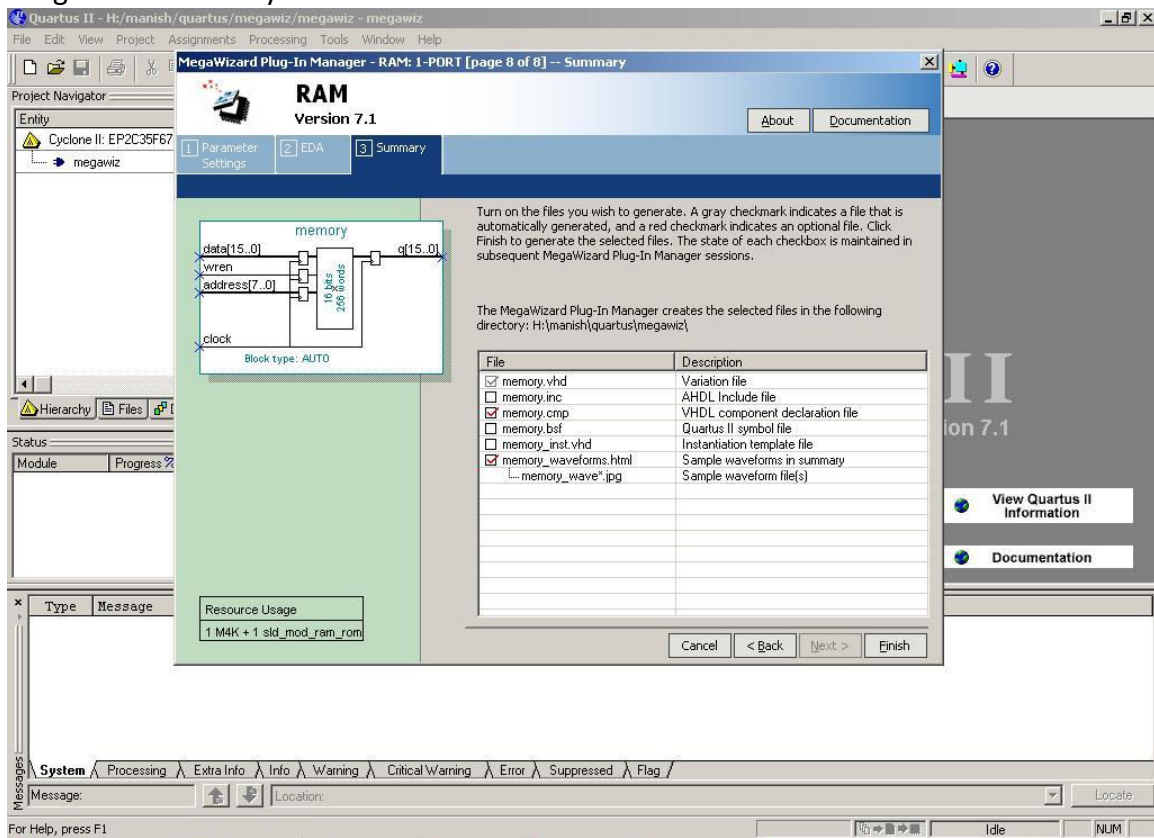


Fig. 7

8. Before you can use the In-System Memory Content Editor tool, one additional setting has to be made. In the Quartus II software select Assignments > Settings to open the window in Fig. 8, and then open the item called Default Parameters under Analysis and Synthesis Settings. As shown in the figure, type the parameter name CYCLONEII_SAFE_WRITE and assign the value RESTRUCTURE. This parameter allows the Quartus II synthesis tools to modify the single-port RAM as needed to allow reading and writing of the memory by the In-System Memory Content Editor tool. Click OK to exit from the Settings window.

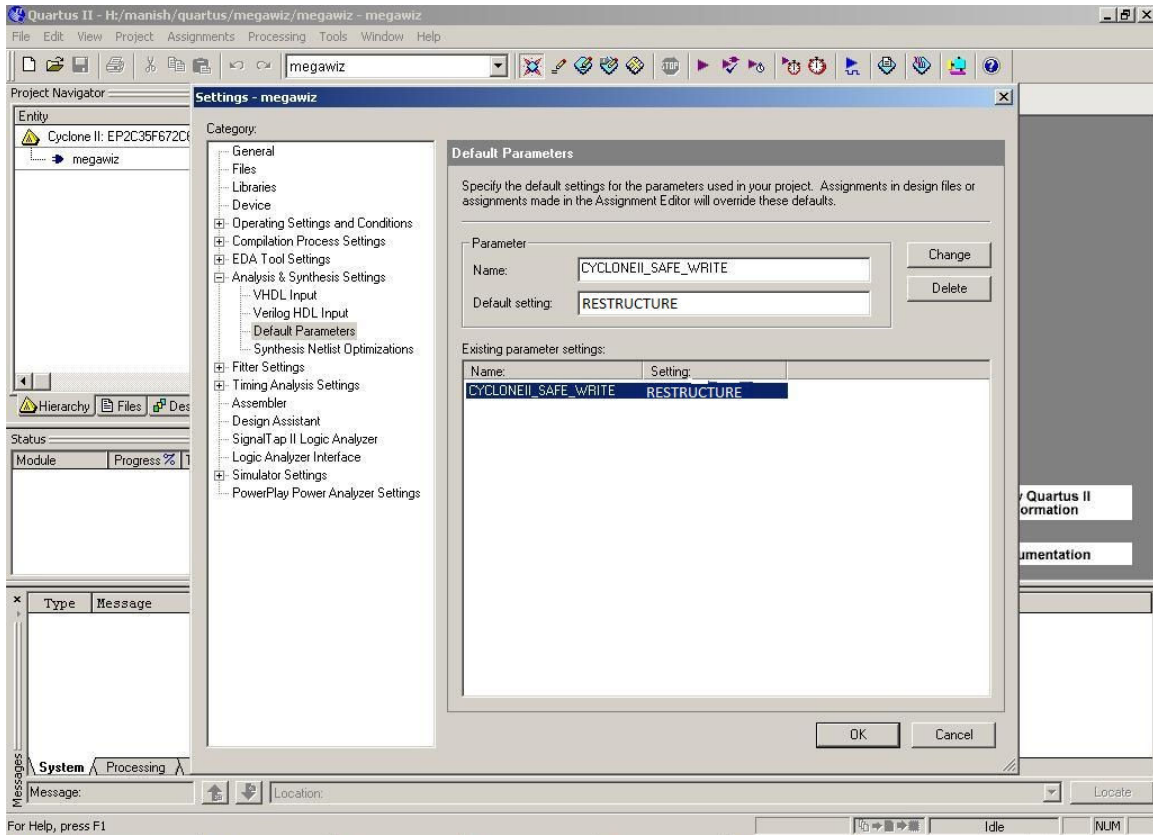


Fig. 8

9. Now use this memory in your design by port mapping. Compile your code and download the circuit onto the DE2 board as instructed in the tutorial 'Altera Quartus II and DE2 manual' available on course website.

10. After downloading the design in FPGA, Select Tools > In-System Memory Content Editor, which opens the window in Fig. 9. To specify the connection to your DE2 board click on the Setup button on the right side of the screen. In the window in Figure 9 select the USB-Blaster hardware, and then close the Hardware Setup dialog.

Note: While doing steps 10 and 11 the FPGA board should be powered up and should be in RUN mode.

- a. You can observe that the device ID specified appears in the instance manager.
- b. The status is ready to acquire and we can see the '??' indicating that the memory has not been read yet.

Select the memory in Instance manager and click the read data from system memory button (one with a red box) as shown in Fig. 10. Now you can see the contents in the memory.

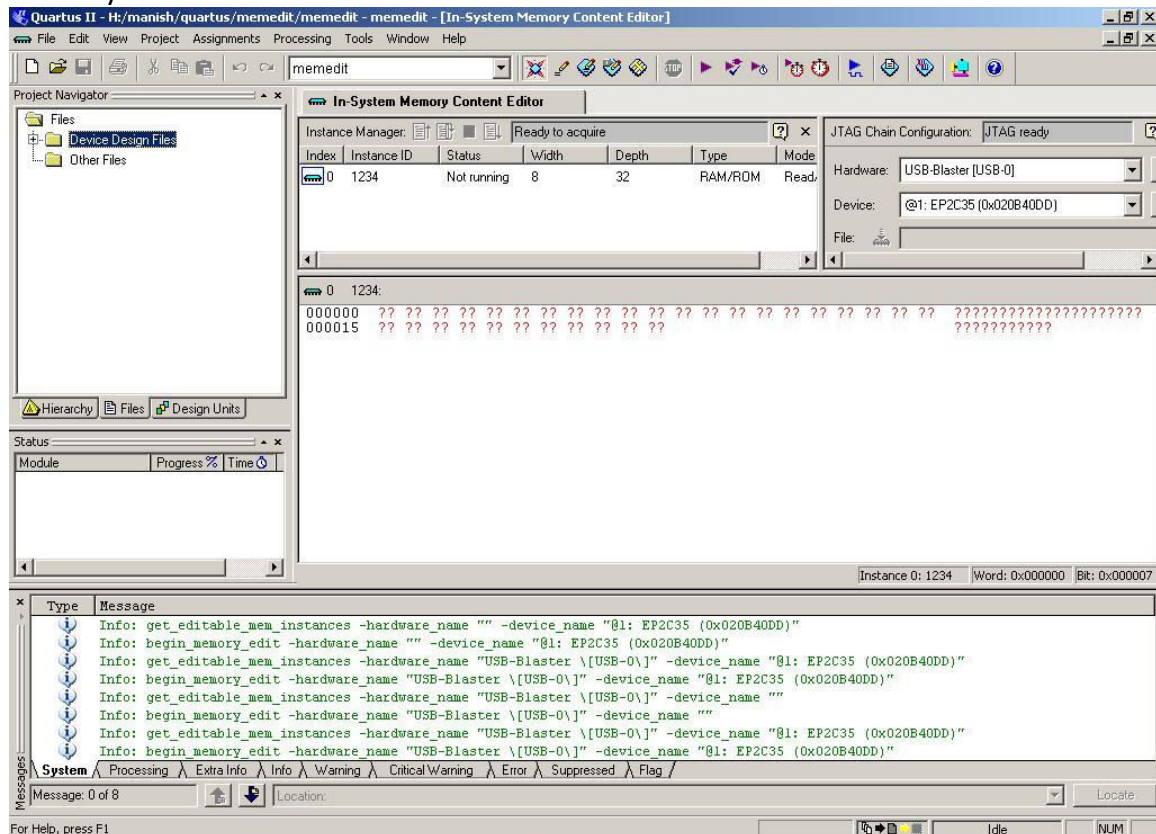


Fig. 9

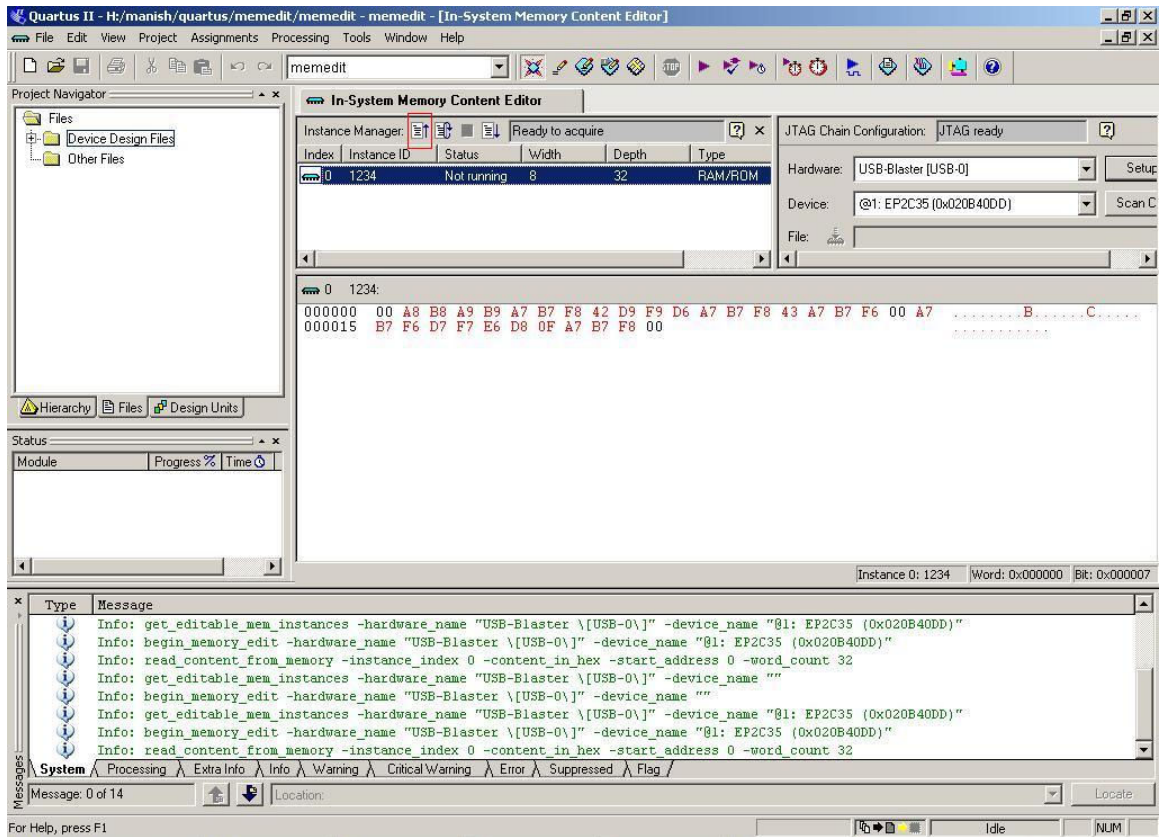


Fig. 10

11. The contents can be modified by directly overwriting them as shown in Fig. 11 at location 000000 we have changed the contents from 00 to 12. This is just a change made in the editor. To actually write the new value in the memory you can click the 'Write' button as highlighted in Fig. 11 with a red box.

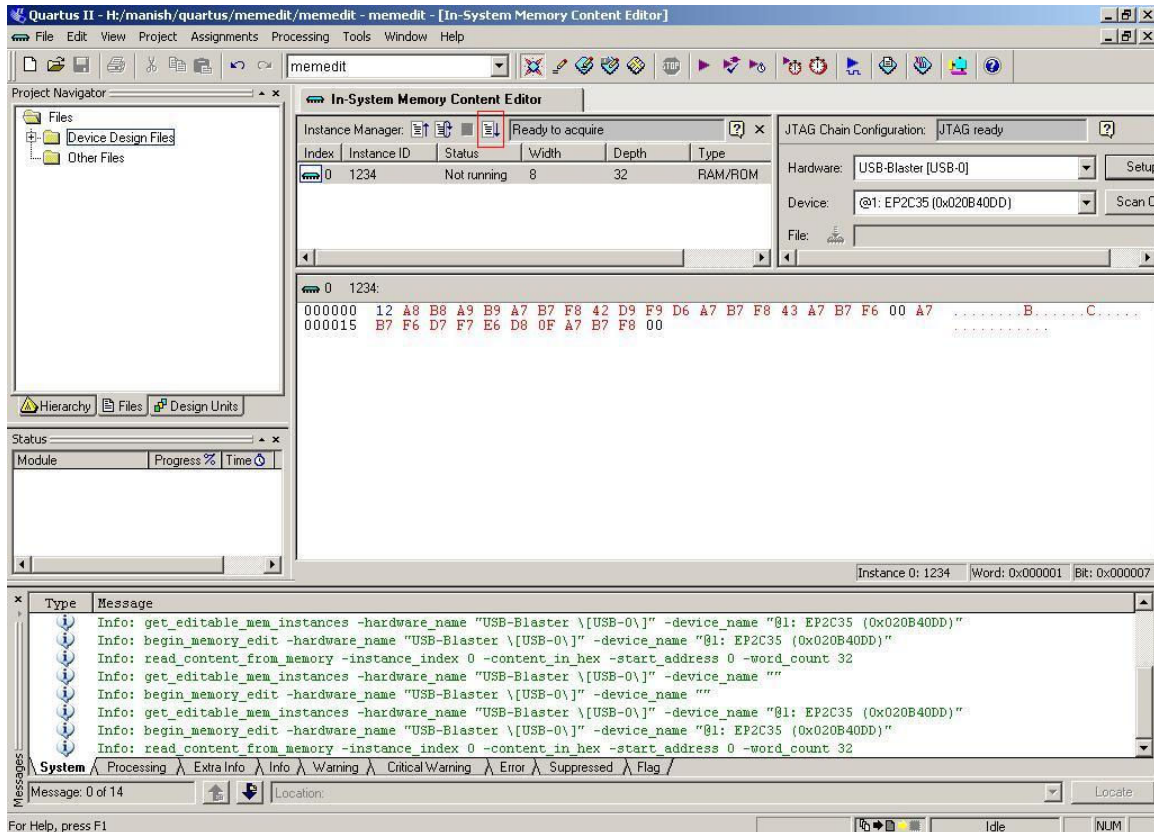


Fig. 11

12. After changing the contents you don't have to recompile your entire design in the FPGA. Just reset your circuit and now the design will operate on the changed memory contents. This run time memory content editor can be used to change one or two operands in your sample program or you can change the entire program as well.