# ELEC 5200/6200 VHDL PROJECT #2
**Due: Wednesday, September 18**

1. Design, test, simulate, and debug VHDL models of the following four components. These can be used as building blocks for your MIPS CPU. Where possible, perform operations on 32-bit vectors rather than individual bits to keep the models simple ("register level" rather than gate level).

   a. 32-bit parallel-load register, loaded on the *falling* edge of clock, CLK, when the enable input (EN) is ***high***.
   b. 32-bit parallel-load latch, loaded via ***active-high*** latch-enable signal LE.
   c. 32-bit 2-to-1 multiplexer with input selection line S.
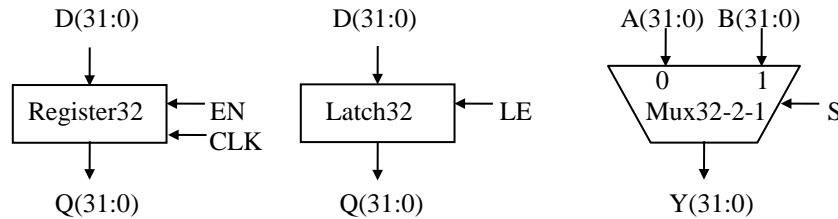


   d. 32-bit bus transceiver.
      - CPU side: IEEE std_logic_vector, with bits having values '0' or '1'
      - BUS side: IEEE std_logic values, with bits having values '0', '1' or 'Z'
      - The receiver outputs should default to '0' when its bus input is 'Z' (each individual bit).
      - The bus driver outputs should be 'Z' when disabled (Enable=0).
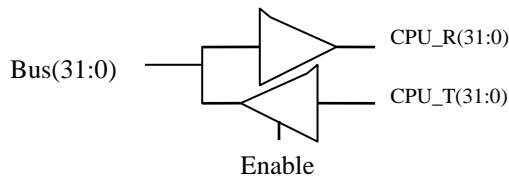


2. Create the following datapath, using the above components and your previously-designed adder/subtracter. The circled signals indicate external inputs and/or outputs for this datapath.
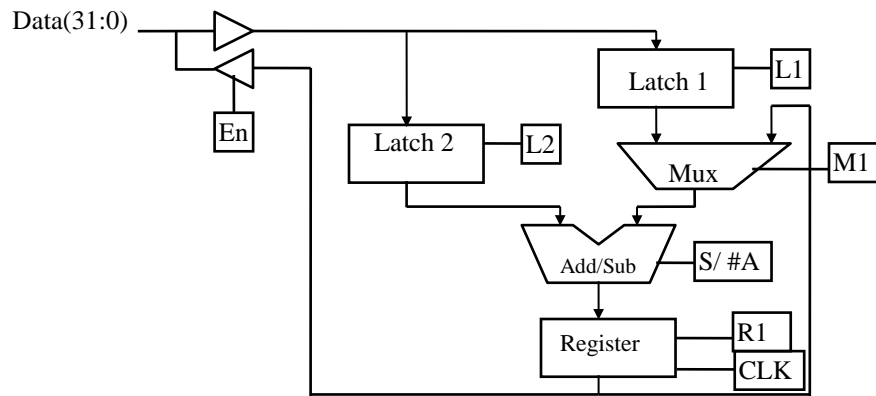


**Provide annotated simulations of the individual components and the datapath.**
**Test the datapath by doing the following:**
   1. Load different data values into latches 1 and 2.
   2. Load the sum of the values in latches 1 and 2 into the register and put this value onto the data bus.
   3. Load new data into latch 2.
   4. Subtract the data value in the register from the data value in latch 2 and put the result into the register and onto the data bus.

   Note that you will stimulate the control signals as if you were a "control unit" for this datapath.