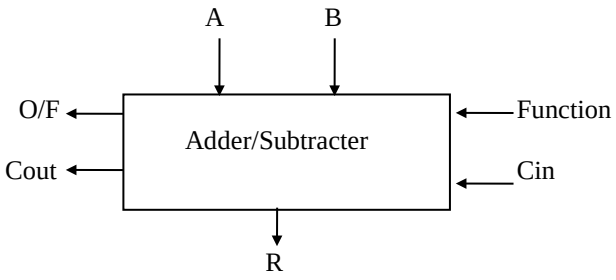
ELEC 5200/6200 VHDL PROJECT #1
Models Due: Wednesday, Sep. 4
Simulations Due: Monday, Sep. 9

Design and model in VHDL a 32-bit arithmetic circuit capable of adding and subtracting 32-bit data words, with or without carry, according to the function table given below. Operands A and B and result R are 32-bit values. "Function", F, is a two-bit code that selects the operation to be performed. Cin is an input from a previously saved "carry flag". Cout is the overall carry output. O/F indicates 2's complement overflow. Refer to Chapter 3 of Patterson/Hennessey and the ELEC 2200 text for discussions on binary arithmetic. Use the default delta delays on all statements that model hardware elements.

Operation	Function	F: Function Code
ADD	R = A+B	00
ADDC (add with carry)	R = A+B+Cin	01
SUB (subtract)	R = A+B	10
SUBB (subtract with borrow)	R = A-B-Cin	11



Design the VHDL model of the adder/subtracter hierarchically as three design units (three VHDL models/files):

1. 4-bit full adder: C_{out} & $S_{3-0} = A_{3-0} + B_{3-0} + C_{in}$
2. 32-bit full adder: Instantiate 4-bit full adders to generate Cout & R = A + B + Cin
3. 32-bit adder/subtracter: Instantiate a copy of the 32-bit adder and use a complementer on the B input, utilizing that and the adder carry input to perform addition and subtraction with the single adder.

Obtain a one-inch 3-ring binder, and insert the following **two items for each design unit**:

1. VHDL model (entity and architecture) – include a few comments in each model
2. ANNOTATED simulation results (LIST format only - no waveforms)
   - Use a highlighter pen to mark where "significant" test inputs are applied and where significant results are displayed.
   - Write a few words (by hand) in the margin next to each highlighted event to indicate what should be observed in the listing. For example, if showing that the adder correctly added 5+6, then highlight the two inputs 5 and 6, highlight the result (11) and write in the margin: 5+6=11.

Points will be deducted for missing or insufficient tests and/or for missing or insufficient annotation. Simulation results not annotated will be assumed incorrect!