CPU Design Project – Part 6 – Hardware Implementation and a Working Processor Demo

ELEC 6200 – Required ELEC 5200 – Optional/Extra Credit

Report Due Friday, 12/6/2013

- 1) Follow the <u>Altera Quartus II and DE2 Manual</u> (posted on course website) for designing and implementing your circuit on the FPGA.
- 2) Reset can be connected to any of the 4 Keys on DE2 Board. These Keys are normally at logic '1'. And pressing them will change the logic to '0'. So make the changes in your design as needed.
- 3) Clock can be connected to any of the two free-running clock frequencies available, 27MHz and 50MHZ. To connect to any of these clock inputs, the pin numbers are mentioned in the Pin Assignment MSExcel sheet. You can also debug your design by connecting the clock to one of the manual keys on the DE2 board, manually creating clock pulses instead of using free-running clock.
- 4) The "inr" input that selects the register number can be connected to any 4 switches on the board. And the "outvalue" that displays the contents of the register selected, can be connected to the LEDs or LCD on the board. For using 7 segment displays on the board you will require a HEX to 7 segment conversion model provided on the course website.
- 5) Run the test program and verify the results with your simulation in part 5.
- 6) You will have to show the implemented design on your DE2 Board. You will be conducting a demo as follows:
 - (a) Briefly describe what is implemented, what program you will run and what result is expected.
 - (b) Run the program pointing to the functions of the buttons you press. Let the viewer examine the result.
 - (c) Offer to make a change to some parameter to a viewer selected value and rerun the demo.
 - (d) Total duration of demo: FIVE MINUTES.
- 7) Part 5 report must be a one-page reply to three questions:
 - (a) What did you learn from this project?
 - (b) What would you do differently next time?
 - (c) What is your advice to someone who is going to work on a similar project?