

CPU Design Project: Part 4-Datapath Verification,
Report Due Wednesday, 10/6/2013

Combine all the components created in part 3 together into a new top-level component which will include both datapath and the control unit connected to each other (also include the instruction memory in your datapath if you have created it in part 3). This top-level component will be very similar to the final CPU you are going to create in part 5 except the memory.

The top-level component must be capable of working with at least a single memory outside the CPU. So it must have at least three 16-bit external “ports” to connect the component to the memory: a Read data bus (16-bit), A Write data bus (16-bit) and an address bus (10-bit). For those who have separate data and instruction memory in the datapath, if you have created an instruction memory in part 3, you will just need one more data memory. Otherwise, you will need two memories (both instruction and data memory) to use in logic simulation. The memory you need will be added in Part 5, which will be the RAM block in the Altera Megafunctions Library.

Verify this top-level component as described in the block diagram and register transfers in Part 2. Write a testbench to verify the correct execution of each instruction in your ISA (except the instructions which need data memory access, like “lw” and “sw”). **Show in the simulation where you verified each required register transfer for the CPU.** (If some register transfers are common to multiple instructions, you do not need to show them separately for every instruction – but it might be a good idea to do so anyway.) After that, write a short program using your instruction set (containing all kinds of instructions except “lw” and “sw”), hand compile the chosen test program into binary code and then use this code to verify if your datapath gives you the expected results.

Think about it, can you verify execution of “lw” and “sw” instruction in this part? If yes, how?

Notes:

1. The top-level design should contain only component instantiations, matching your block diagram (changes may be made to the diagram as necessary).
2. In the simulation, if you have included the instruction memory in your datapath, you can place instructions in the instruction memory to do simulation. **Otherwise**, you need to supply instruction(s) to the datapath manually in the testbench.
3. You are to submit the following in your notebook:
 - a) The VHDL code of the top level component.
 - b) Simulation results showing correct execution of each instruction and also the short test program. Clearly label the important information on the simulation results.
 - c) Both the assembly code and the binary code of the test program you used.