ELEC 4200 Lab#5

Hierarchical & Parameterized VHDL Modeling, Simulation & Synthesis

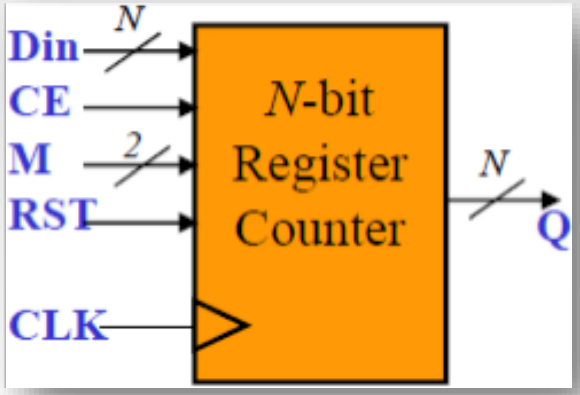
AUBURN

UNIVERSITY

SAMUEL GINN
COLLEGE OF ENGINEERING

Specifications (1)

- Write a parameterized VHDL model for a rising edge-triggered N-bit universal register/counter with the following specifications in order or precedence
  - Active high synchronous reset (RST)
  - Active high clock enable (CE)
  - Two mode control inputs (M1 & M0)
- Reference the function table below for modes of operation.
- Note: during shift register mode Qn-1 ← Dn-1



RST	CE	M1	M0	Q^+	Function
1	X	X	X	$Q_i^+ <= 0$	Reset
0	1	0	0	$Q^+ <= Q$	Hold
0	1	0	1	$Q_i^+ <= Q_{i+1}$	Shift
0	1	1	0	$Q^+ <= Q+1$	Count
0	1	1	1	$Q^+ <= Din$	Load

Pre-lab Assignment

- Write a PARAMETERIZED VHDL model for the register/counter using the specifications previously mentioned.
- Write a separate VHDL model for the digital one-shot from Lab 4
- Write a hierarchical VHDL model that calls and connects the register/counter model and the digital one-shot.
  - A VHDL model of a “debouncing” circuit is provided on the lab web page. This should be inserted before the digital one-shot.
  - The output of the digital one-shot drives the clock enable (CE)
- Determine the values of N you will use for simulation and design verification
- Determine the FPGA pin numbers you will use for LEDs, push buttons, and switches for both values of N
  - Make a table of these

Note: You should have FOUR total VHDL models
(Top-level, register-counter, one-shot, debounce)

Lab Exercise (1)

- Do the following for each value of N
  - Simulate and verify your register/counter VHDL model
  - Simulate and verify your hierarchical model that combines the register/counter and digital one shot
    - Be sure to take into account how signals propagate through the one-shot
  - Synthesize and implement your design for the Artix-7 FPGA on the Nexys4 board
    - Record the number of FFs, LUTs, and slices used
    - Put these in a table
  - Demonstrate your working circuit (all modes) to the GTA

- Be sure the GTA sees both values of N

Lab Exercise (2)

- Choose one of your N values and create one of the following circuits by hard coding M1 and M0
  - Counter (M1=1 and M0=0)
  - Shift Register (M1=0 and M0=1)
  - Parallel load register (M1=1 and M0=1)
- Record the number of FFs, LUTs ,and slices used
- Repeat the process for the other two modes
- Demonstrate to the GTA your working circuit with one value of N

Note: RST and CE must still function in each circuit

Note: There are a total of THREE circuits you must demonstrate

Report Guidelines

- Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:
  - All verified VHDL models
  - Annotated screenshots of your Aldec Active-HDL simulation results
    - » Be sure to describe your testing method
  - Design work (if applicable)
  - Table of synthesis results for each of the five circuits
    - » First N value, Second N value, Counter, Shift, Load
  - Answers to the following questions…

1. What values did you choose for N and why?

2. Compare the implementation results (resource usage) for the case in which the mode was hard-coded vs. the case for which the mode was left as selectable.