ELEC 4200 Lab#1
Combinational Design Using Logic Equations

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- References you may need:
  - **Nexys4-DDR_rm.pdf**
  - **Lab #0 Tutorial**

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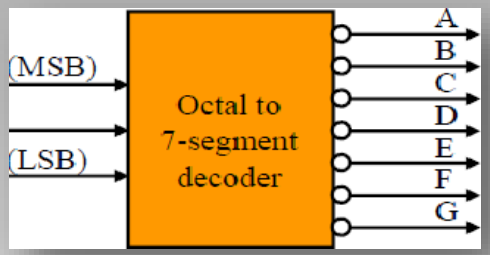
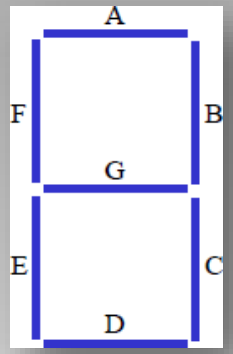
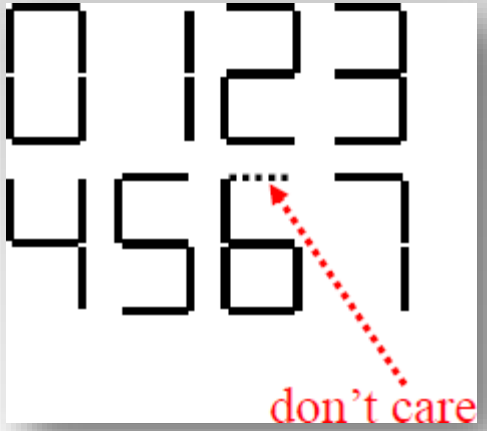
Overview

- Design an octal to 7-segment decoder with active-low outputs
  - Inputs D2-D0
  - Outputs A-G
- Generate:
  - Complete truth table
  - K-maps
  - Minimized SOP equations
  - Logic diagram





- Create a VHDL model from the SOP equations; use *Active-HDL* to simulate and verify the design, debugging as needed
  - *One model with individual input/output signals*
  - *One model with vector input/output signals*
- Use *Vivado* to synthesize, implement, download, and verify each model on the Nexys4 board



Pre-lab Assignment

1) Derive the truth table for the decoder

2) Use K-maps to obtain minimized SOP expressions
   - Share common product terms and gates where possible

3) Draw a logic diagram
   - Share common product terms and gates where possible
   - Label all inputs and outputs according to the system specifications

4) Read the following from the Nexys4-DDR reference manual
   - Chapter 1
   - Chapter 10

Lab Exercise

1) Create a VHDL model from the instructor-provided template, entering your SOP logic equations in the architecture
2) Simulate your circuit in *Active-HDL* for design verification
   - Simulate and verify all possible input combinations
   - Debug and fix problems if the output is incorrect
     - Check truth table against K-map population
     - Check K-map groups against logic equation product terms
3) In *Vivado*, synthesize and implement your design for the Artix-7 XC7A100T FPGA on the Nexys4 board.
   - Connect inputs (D2-D0) to switches
   - Connect outputs (A-G) to the 7-segment display
4) Download and verify your design
   - Verify for all possible input values
   - Debug and re-download as needed
5) Demonstrate your working circuit to the GTA
6) Repeat steps 1-5 using vectors for the inputs and outputs.

Report Guidelines

- Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:
  - Your VHDL model(s) – including appropriate comments
  - Annotated screenshot of your Active-HDL simulation results
    - Be sure to describe your testing method
  - Design work (truth-tables, k-maps, equations, etc)
  - Answers to the following questions…

1. Just by looking, would it have been easier to implement the circuit using POS equations for all outputs? What about just some outputs?
2. Based on your understanding of FPGA's, how would the SOP and POS implementations of the above circuit differ when implemented on an FPGA?