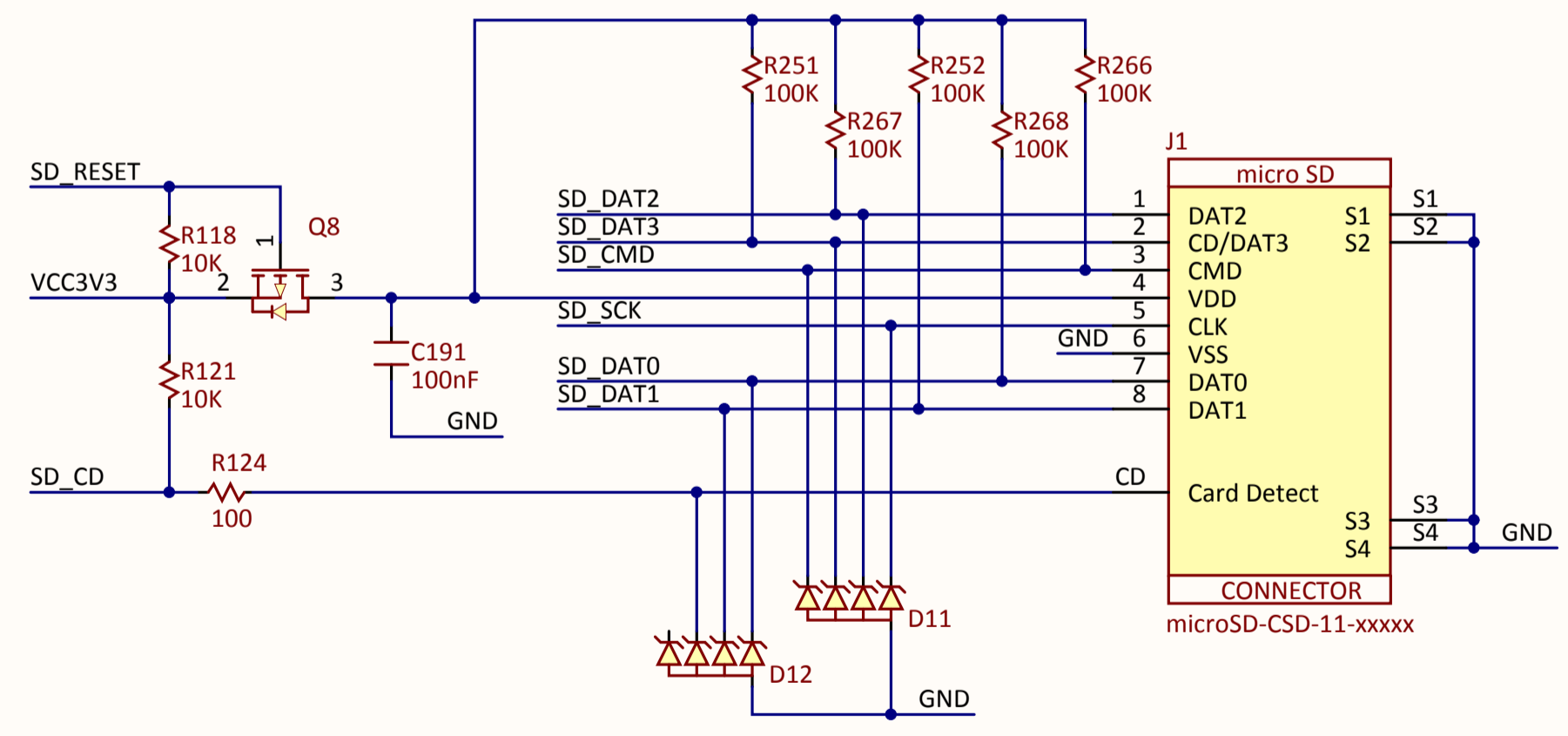
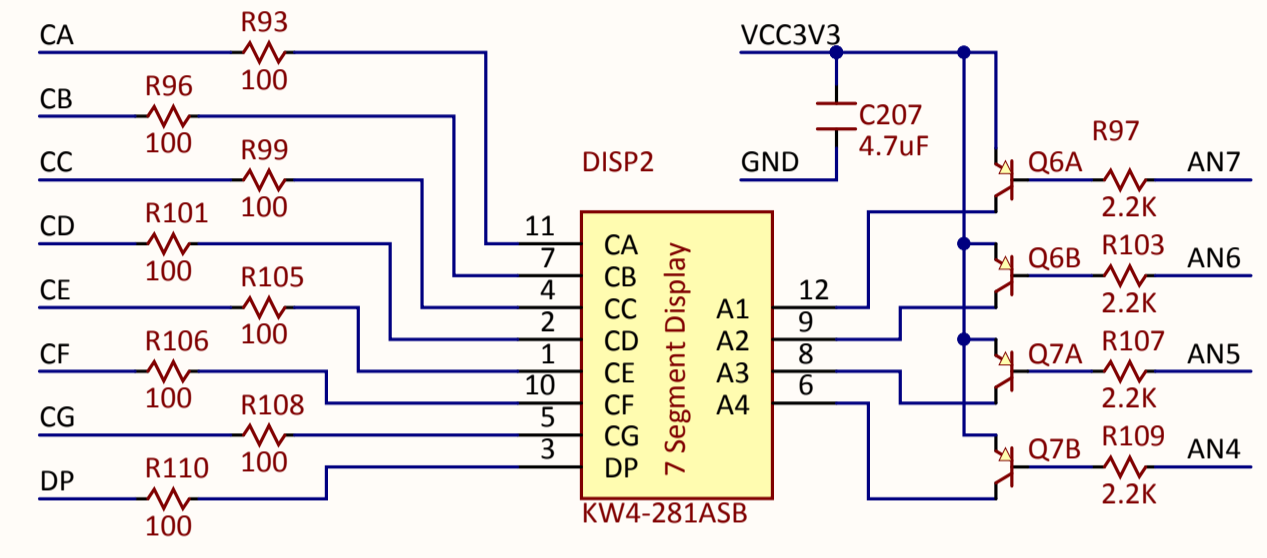
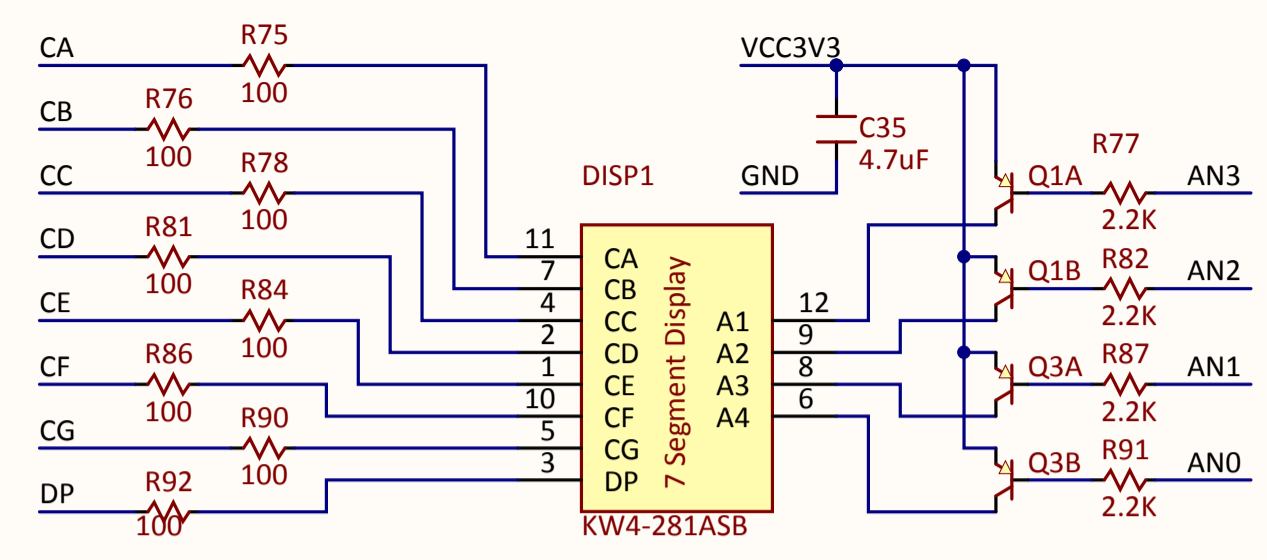
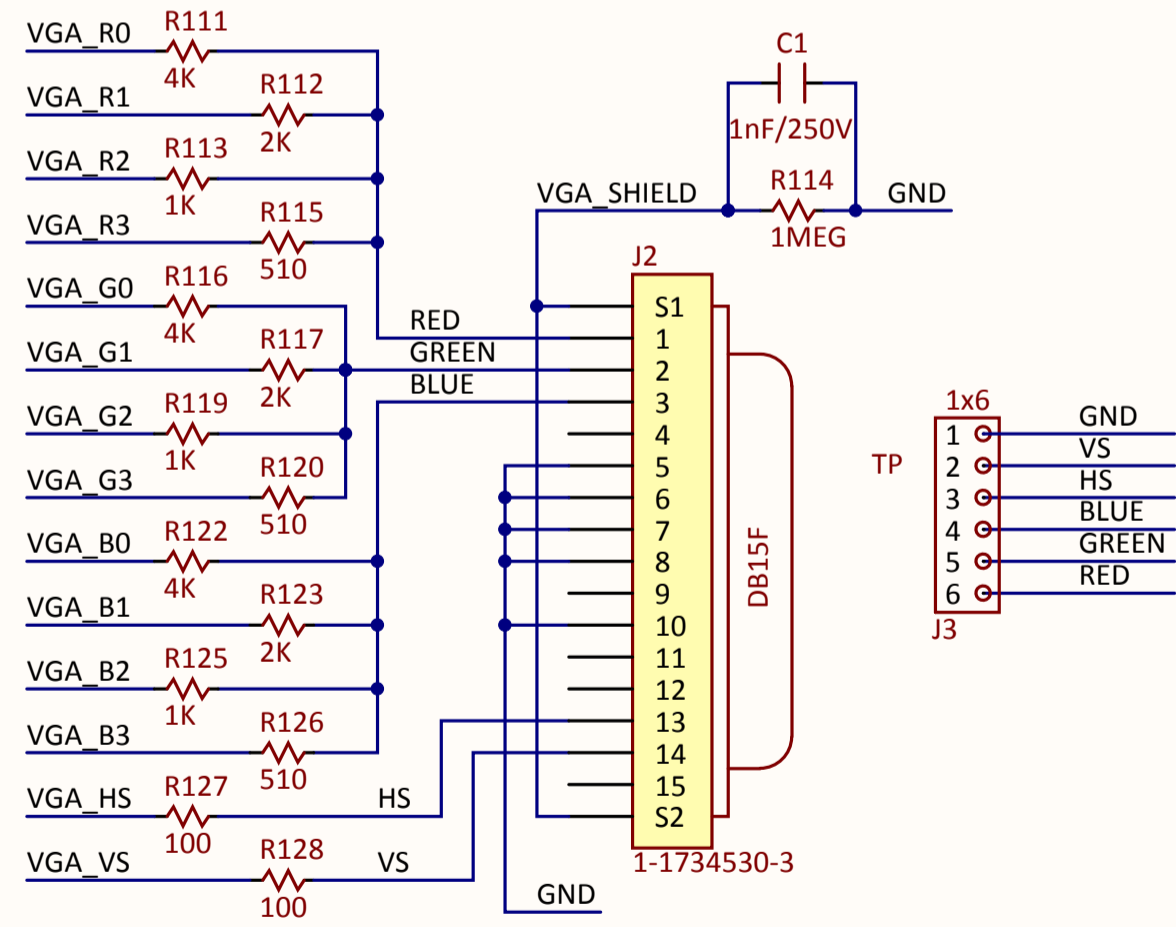
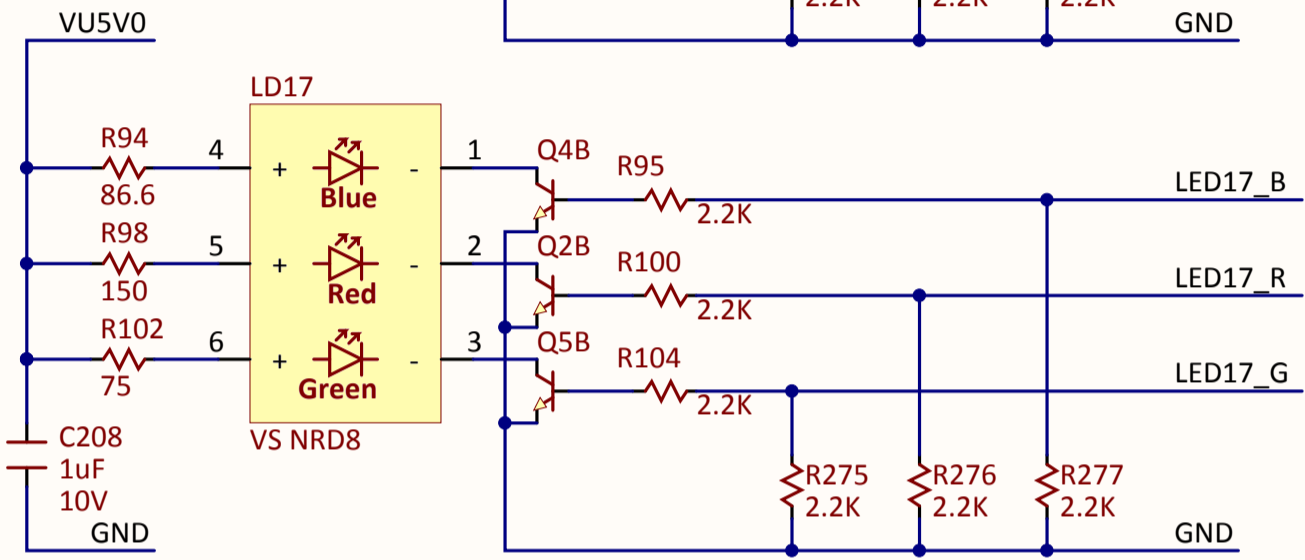
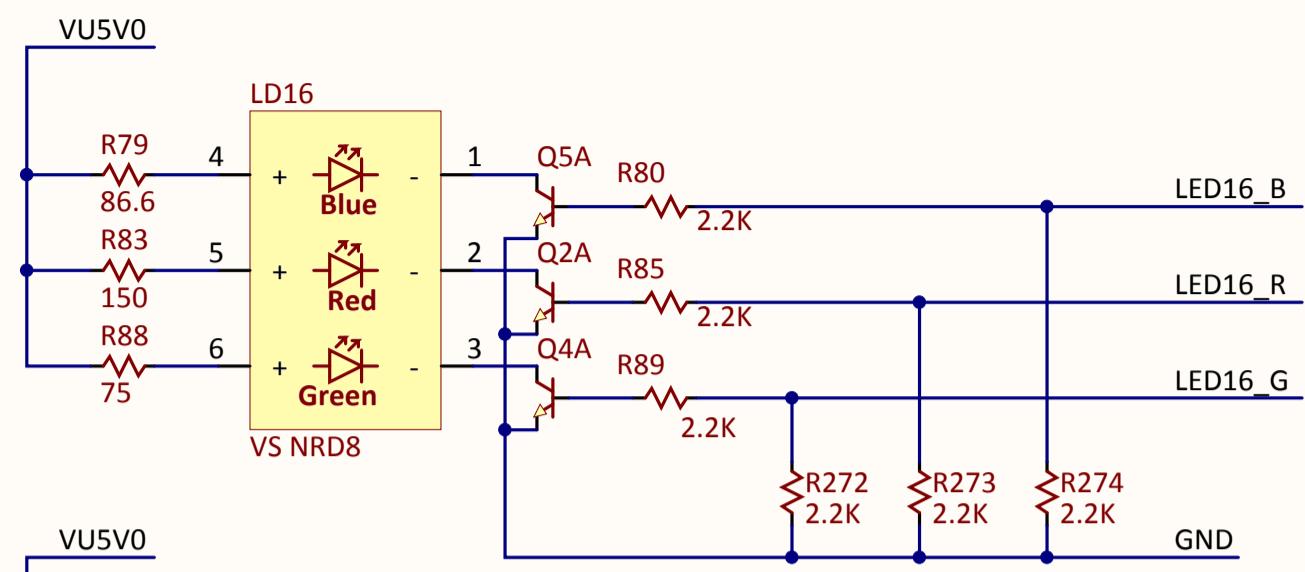


- F1 Foot
- F2 Foot
- F3 Foot
- F4 Foot

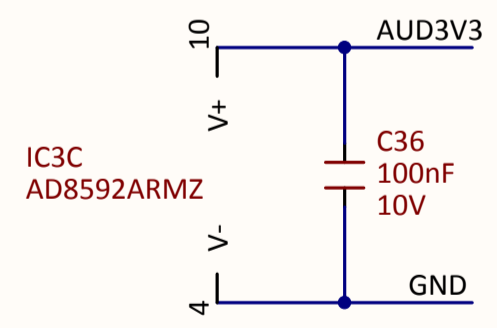
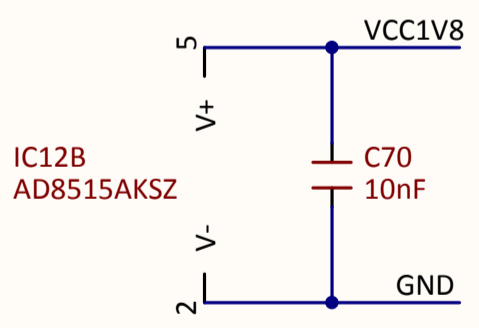
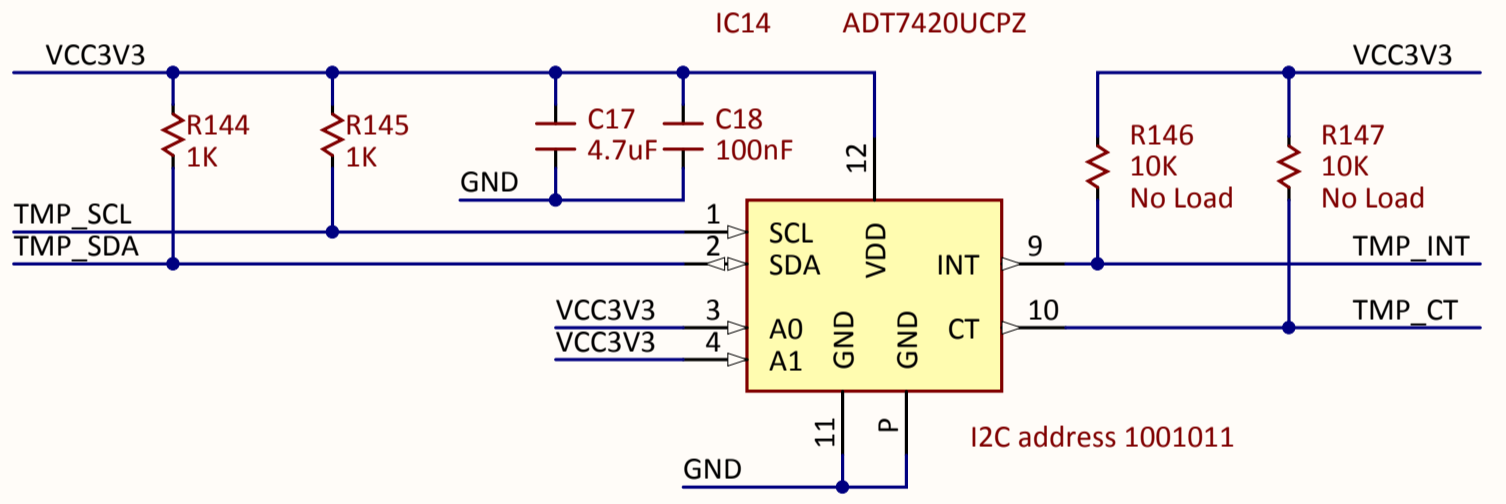
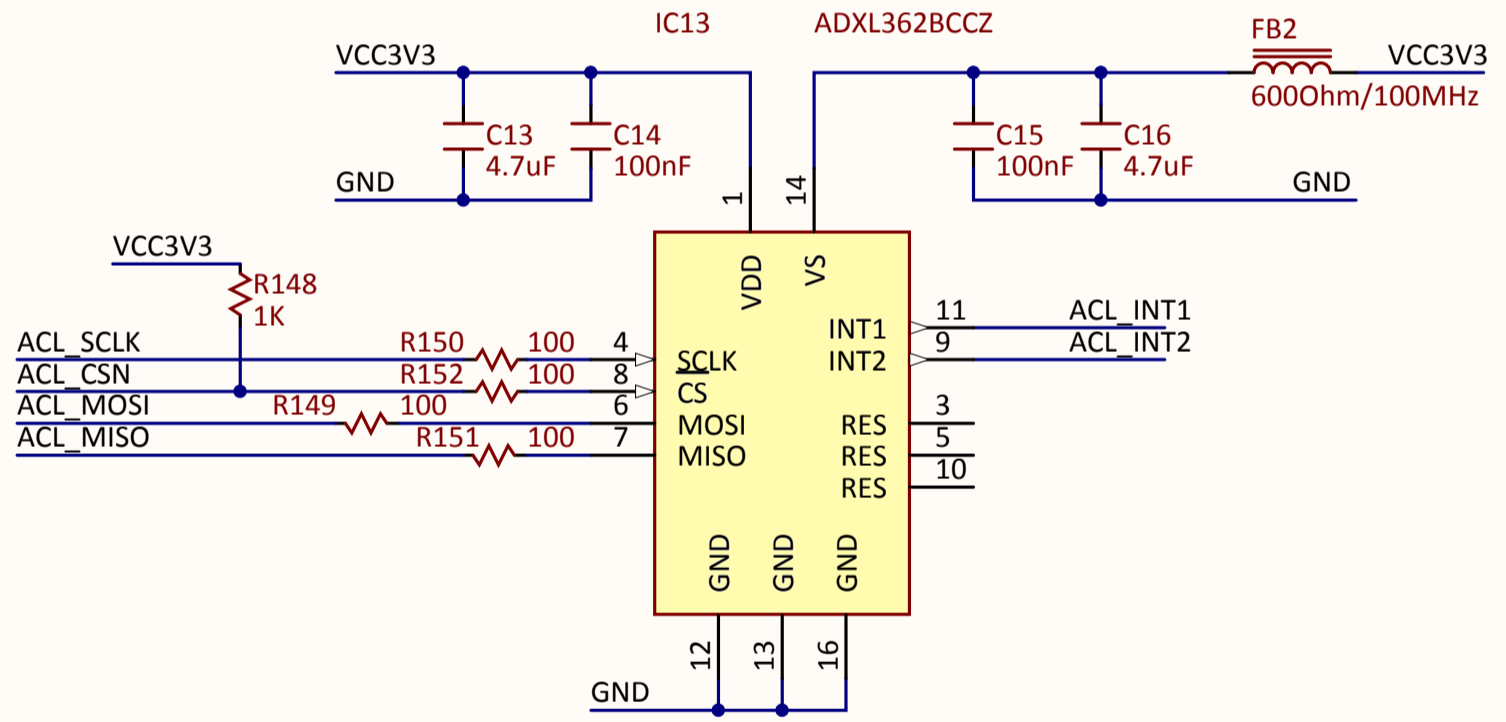
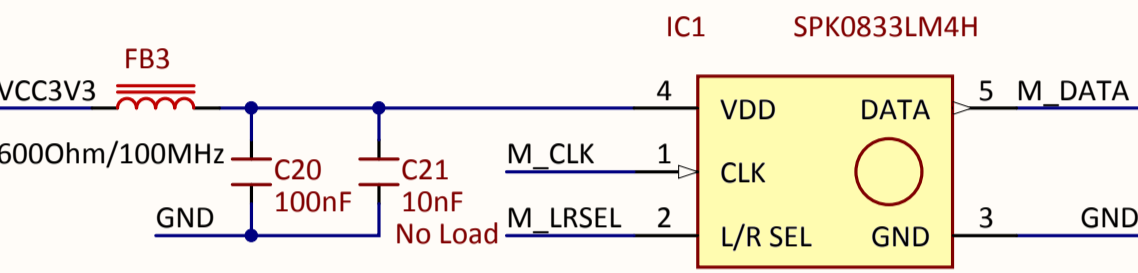
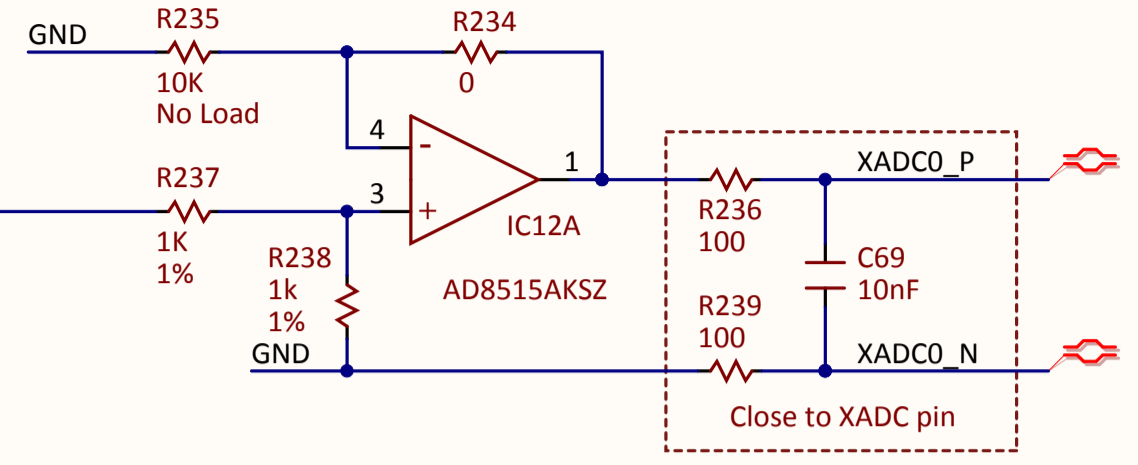
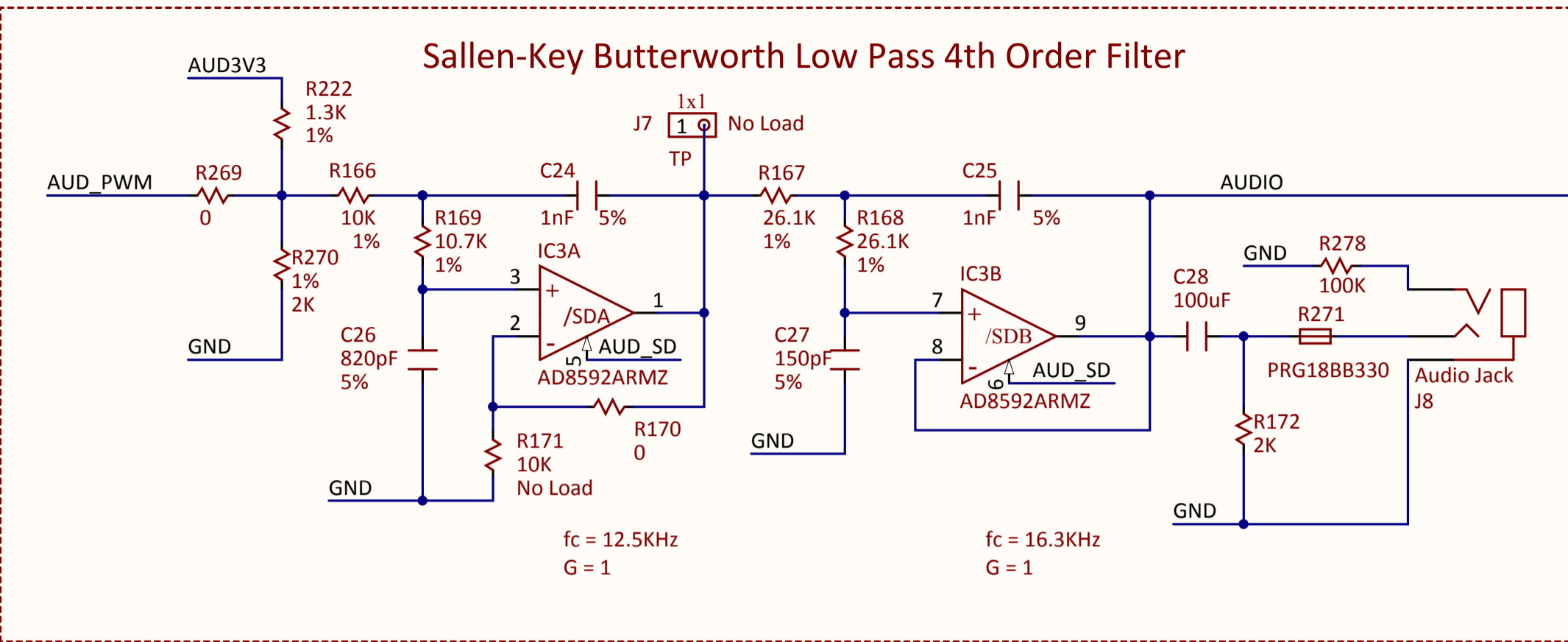
- CE
- ROHS
- Xilinx
- Digilent Inc.
- Nexys 4 DDR
- Chinese ROHS
- Analog Devices

Title Nexys 4 DDR		Rev C.1 Copyright 2014
Circuit PMOD, I/O		
Doc# 500-292		
Engineer EG		
Author DL		
Date 6/10/2014		
Sheet# 1 out of 11		



Title		Rev	
<h1>Nexys 4 DDR</h1>		C.1	
Circuit		Copyright 2014	
7 SEG, VGA, SD			
Doc#	500-292		
Engineer	EG		
Author	DL		
Date	6/10/2014		
Sheet#	2 out of 11		

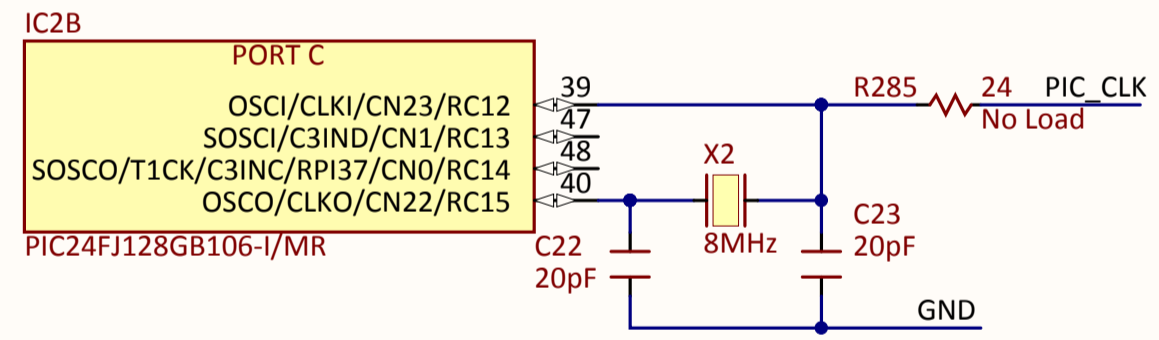
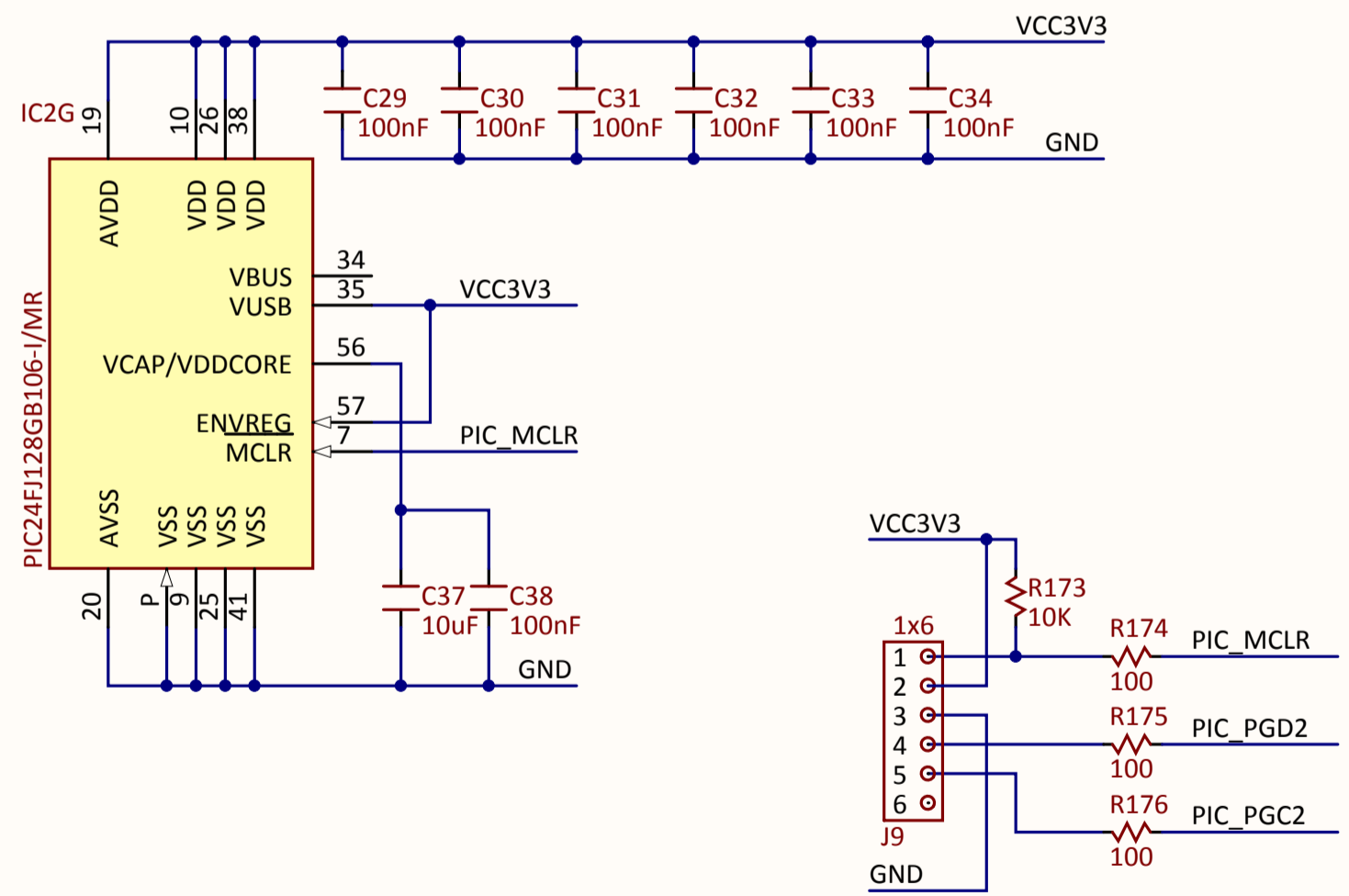
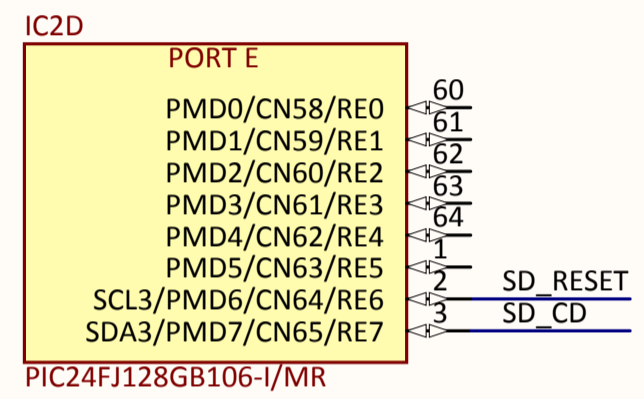
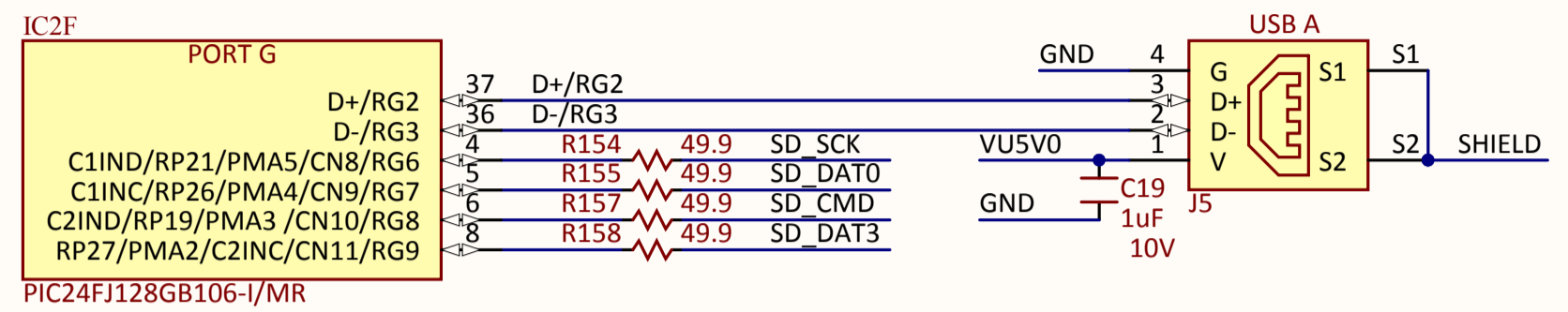
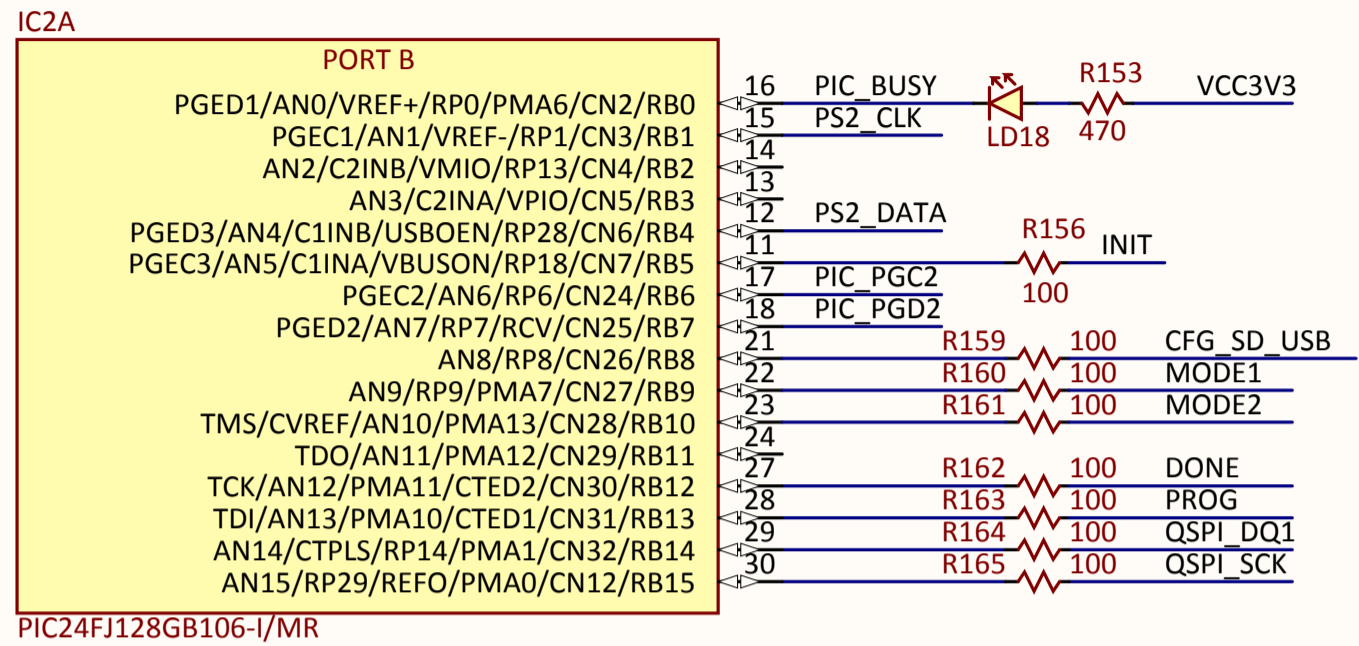
Sallen-Key Butterworth Low Pass 4th Order Filter



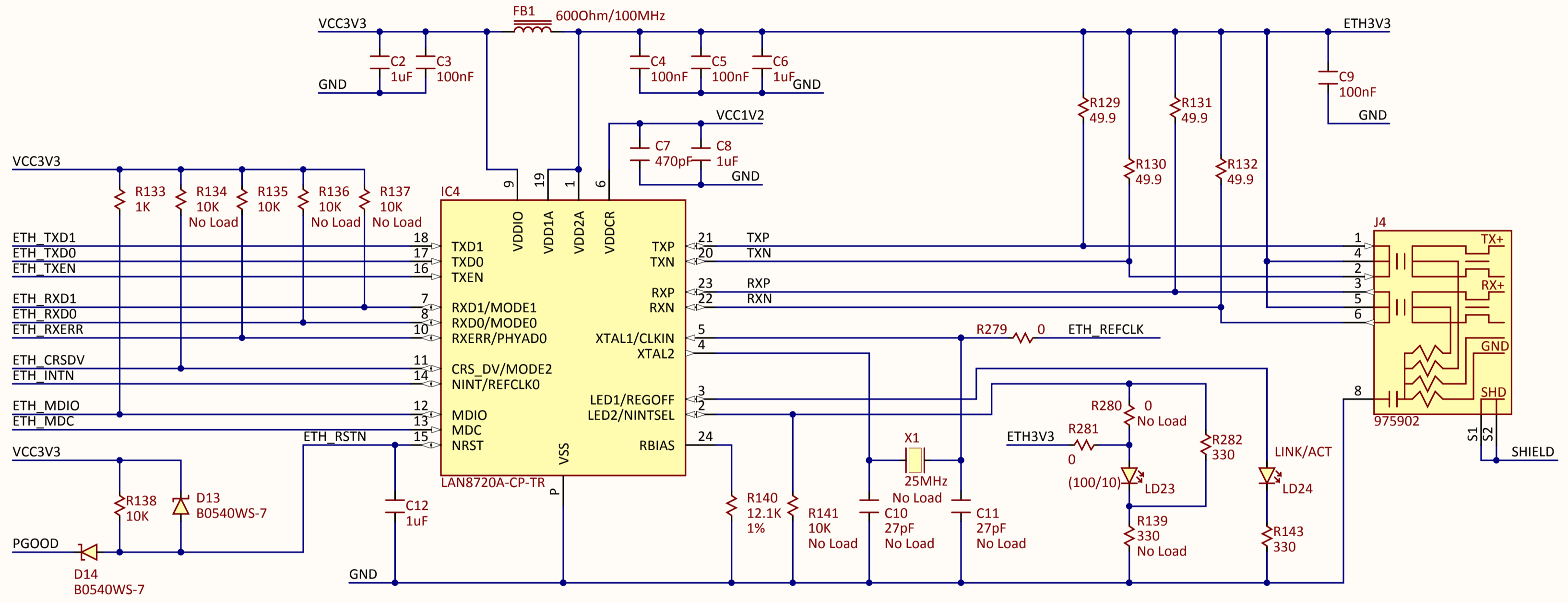
For more information on the parts used in this design, please refer to:

- <http://www.analog.com/ad8592> (CMOS Single Supply RRIO Dual Op Amp with ±250 mA Output Current and Shutdown Mode)
- <http://www.analog.com/ad8515> (1.8 V Low Power CMOS Rail-to-Rail Input/Output Operational Amplifier)
- <http://www.analog.com/adxl362> (Micropower, 3-Axis, ±2 g/±4 g/±8 g Digital Output MEMS Accelerometer)
- <http://www.analog.com/adt7420> (±0.25°C Accurate, 16-Bit Digital I2C Temperature Sensor)

Title		Rev
Nexys 4 DDR		C.1
Circuit		Copyright 2014
ETH, TMP, ACL,AUDIO		
Doc#	500-292	
Engineer	EG	
Author	DL	
Date	6/10/2014	
Sheet#	3 out of 11	



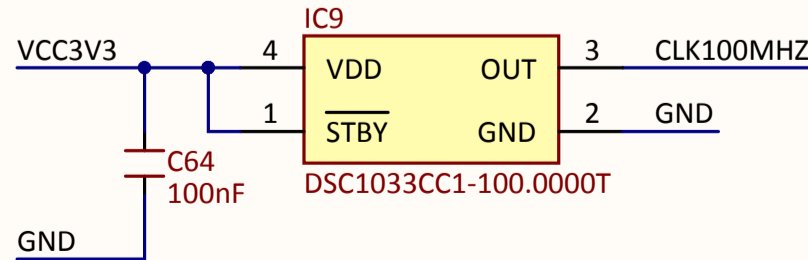
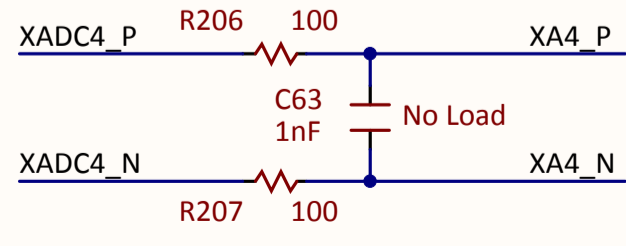
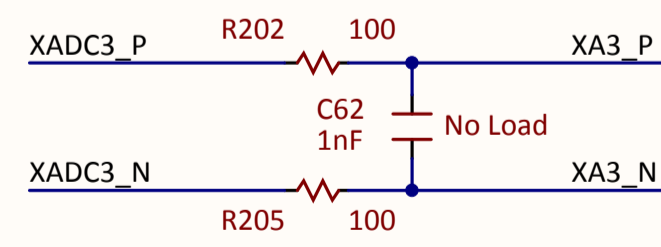
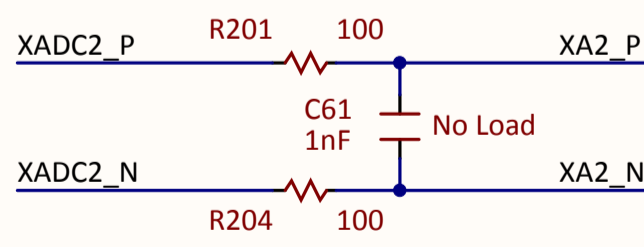
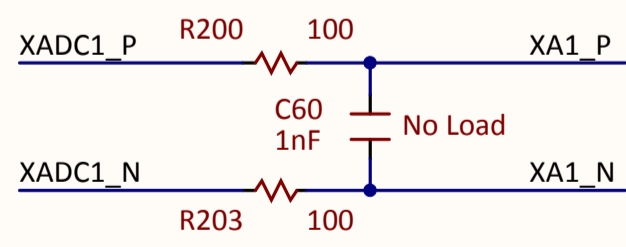
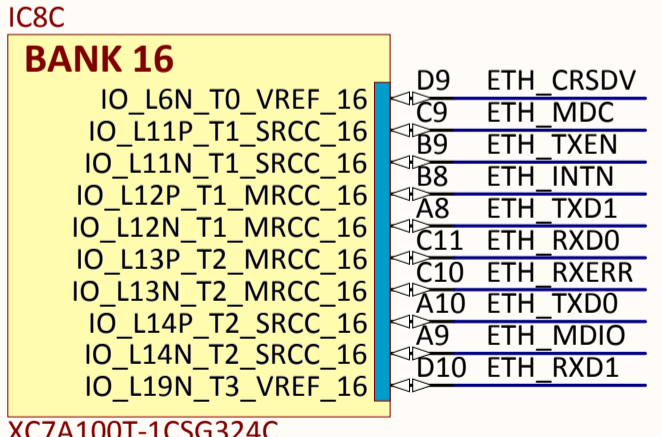
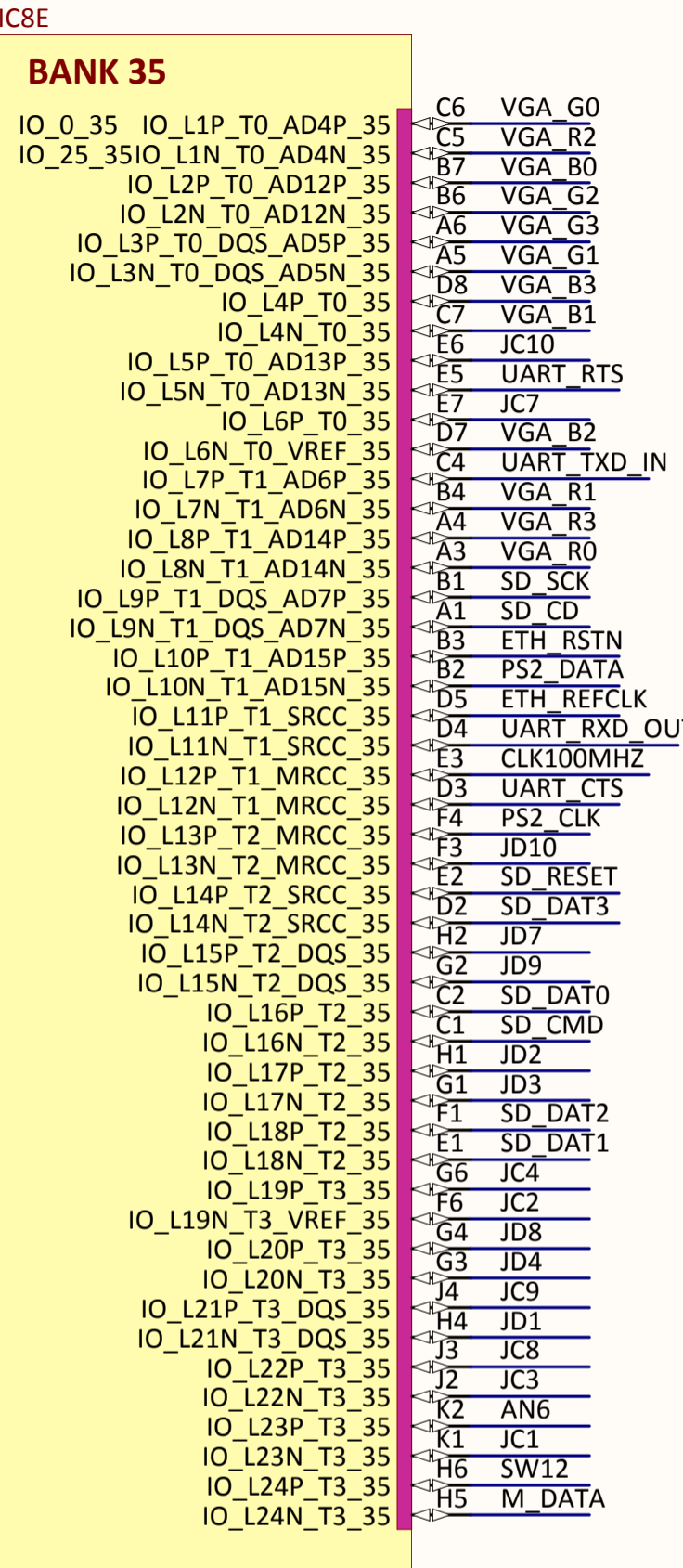
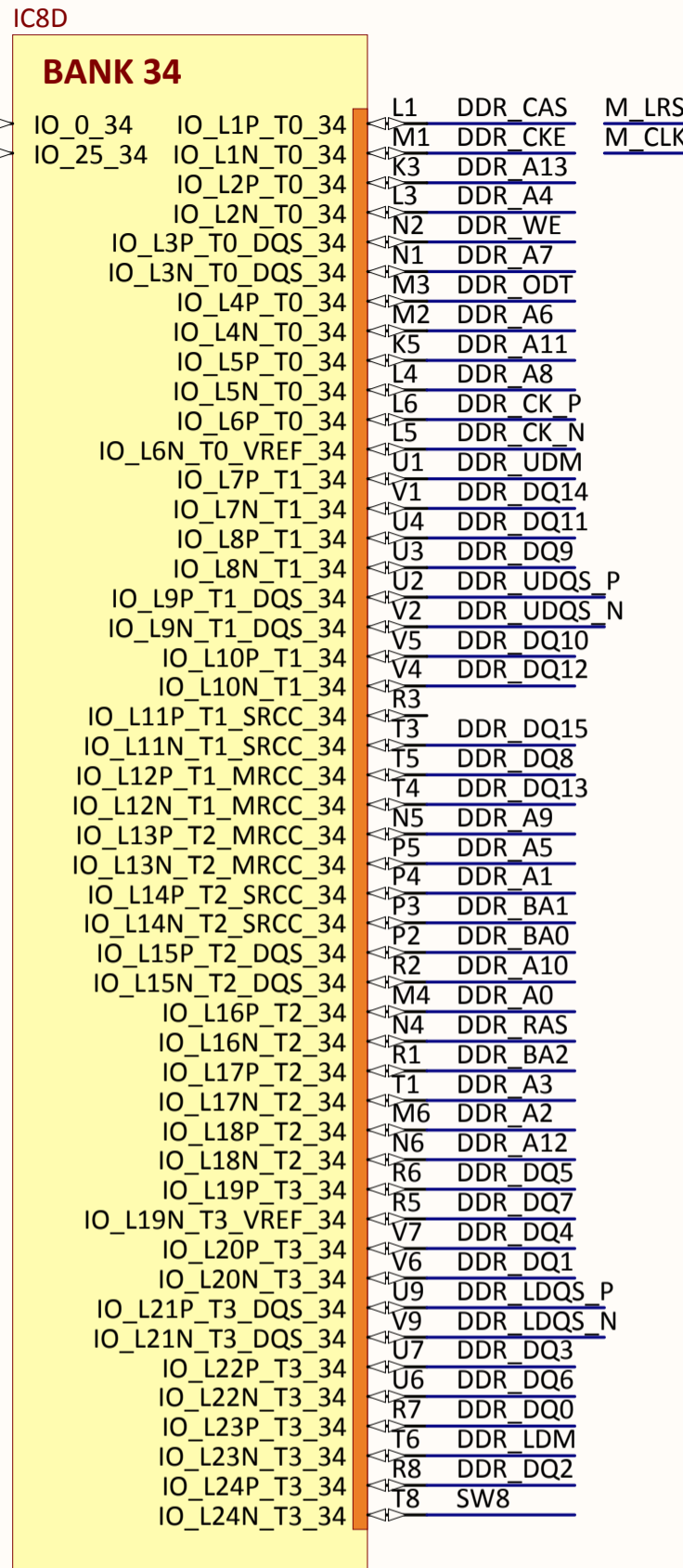
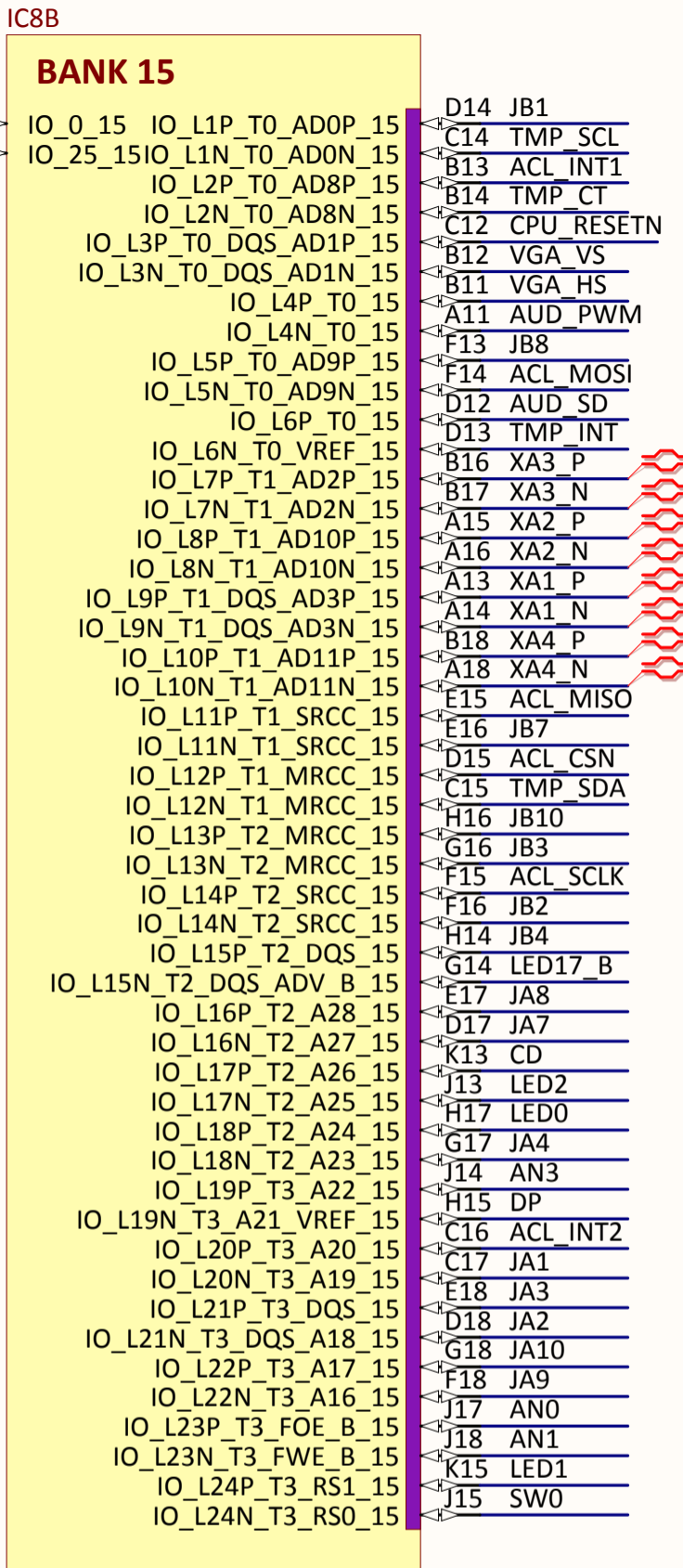
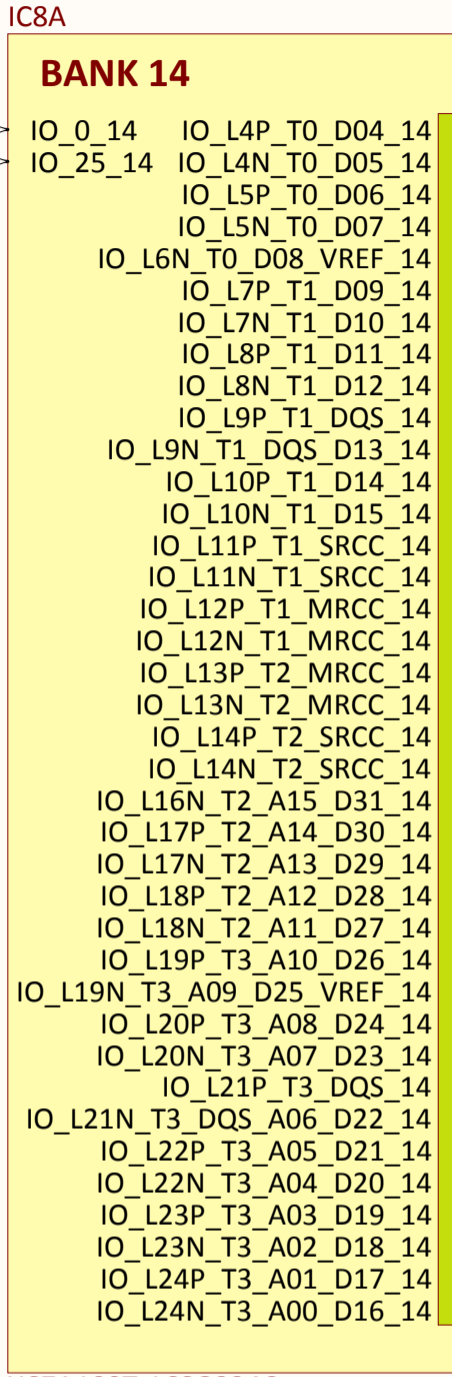
Title		Nexys 4 DDR		Rev		C.1	
Circuit		USB HID		Copyright		2014	
Doc#		500-292					
Engineer		EG					
Author		DL					
Date		6/10/2014					
Sheet#		4 out of 11					



NOTE: REF_CLK In Mode (ETH_REFCLK = 50MHz)

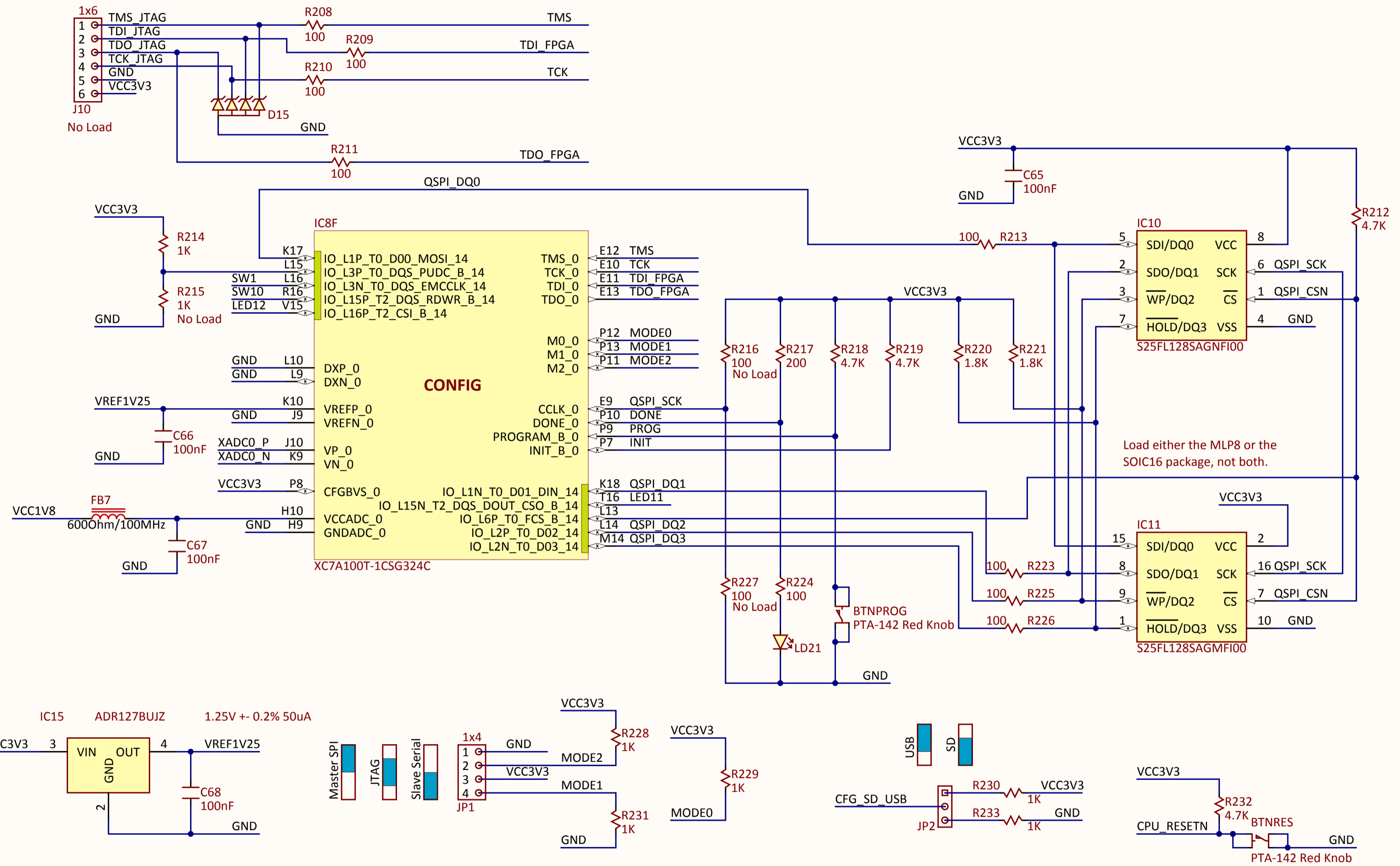
Title Nexys 4 DDR		Rev C.1 Copyright 2014
Circuit ETHERNET		
Doc# 500-292		
Engineer EG		
Author DL		
Date 6/10/2014		
Sheet# 5 out of 11		

This page intentionally left blank.



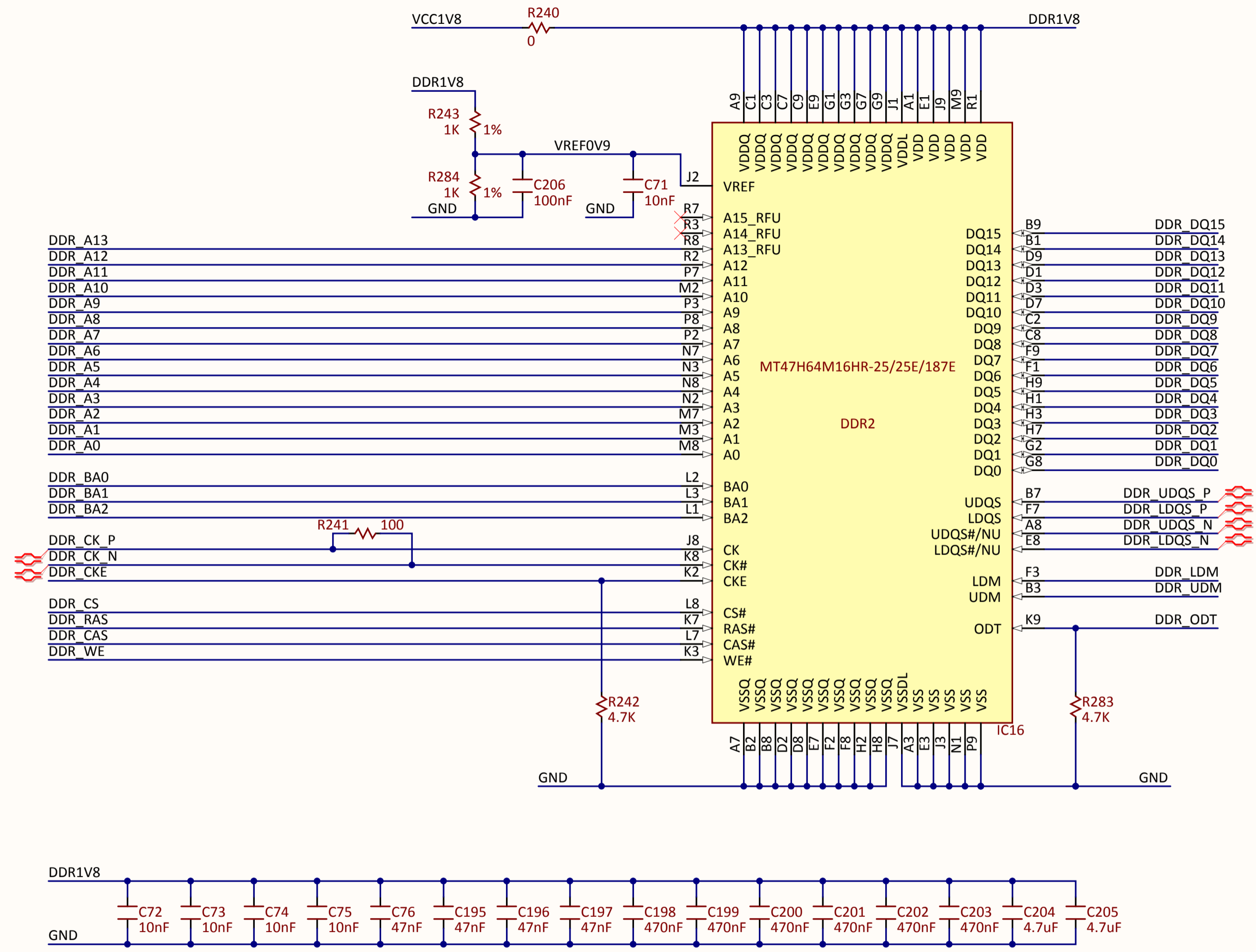
Title		Rev	
<h1>Nexys 4 DDR</h1>		<h1>C.1</h1>	
Circuit		Copyright 2014	
FPGA BANKS			
Doc#	500-292		
Engineer	EG		
Author	DL		
Date	6/10/2014		
Sheet#	7 out of 11		





For more information on the parts used in this design, please refer to:
<http://www.analog.com/adr127> (Precision, Micropower LDO Voltage References in TSOT)

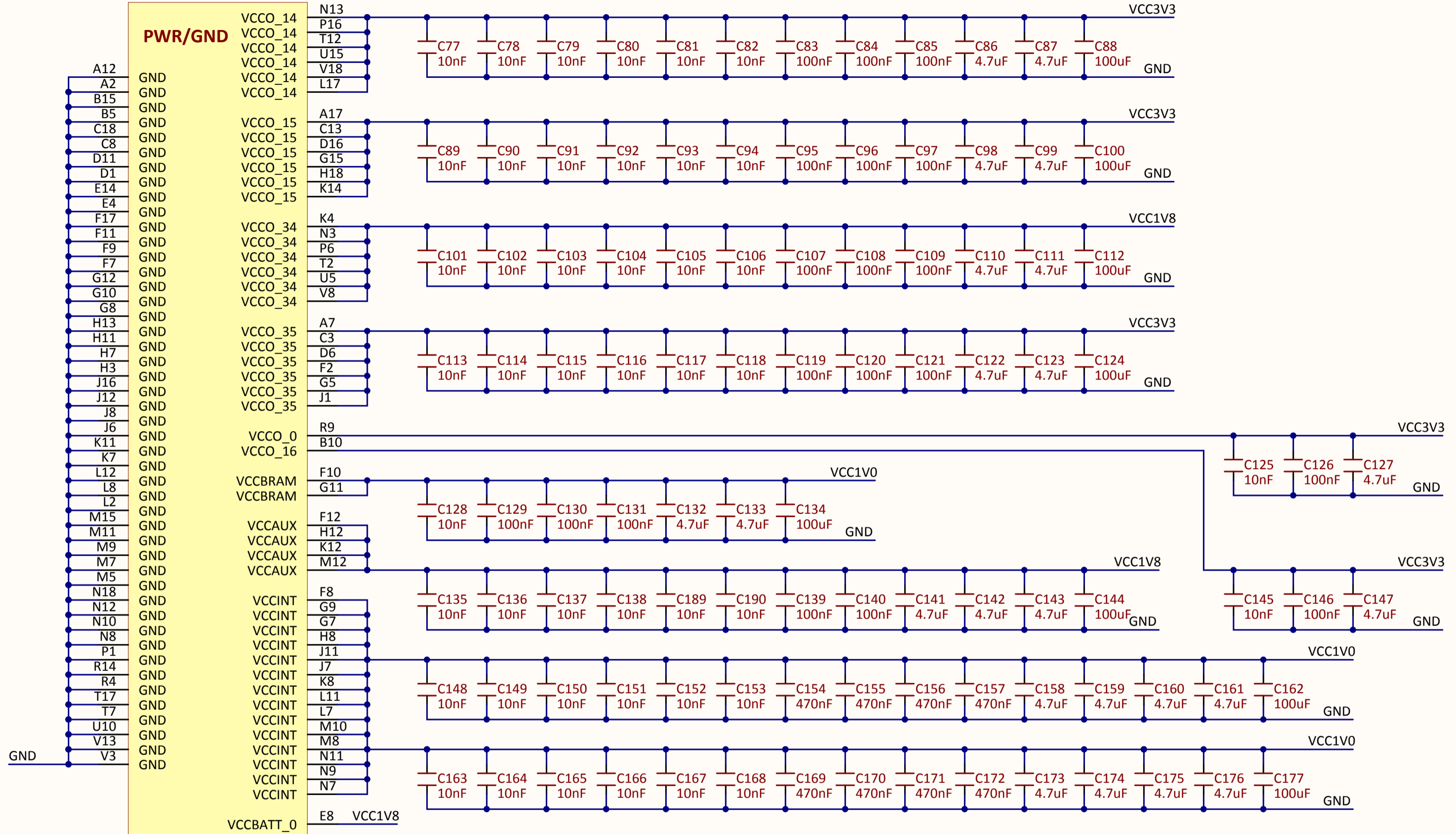
Title		Rev	
<h1>Nexys 4 DDR</h1>		C.1	
Circuit		Copyright 2014	
CONFIG, SPI FLASH			
Doc#	500-292		
Engineer	EG		
Author	DL		
Date	6/10/2014		
Sheet#	8 out of 11		



Title Nexys 4 DDR		Rev C.1 Copyright 2014
Circuit DDR2 Memory		
Doc# 500-292		
Engineer EG		
Author DL		
Date 6/10/2014		
Sheet# 9 out of 11		

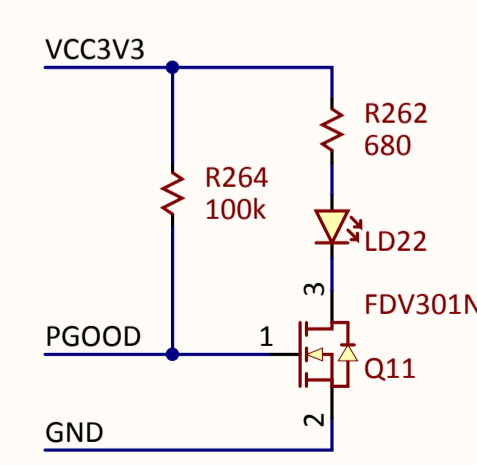
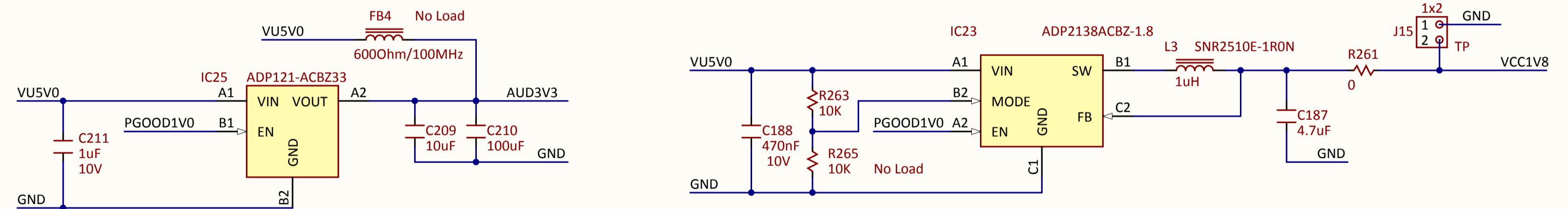
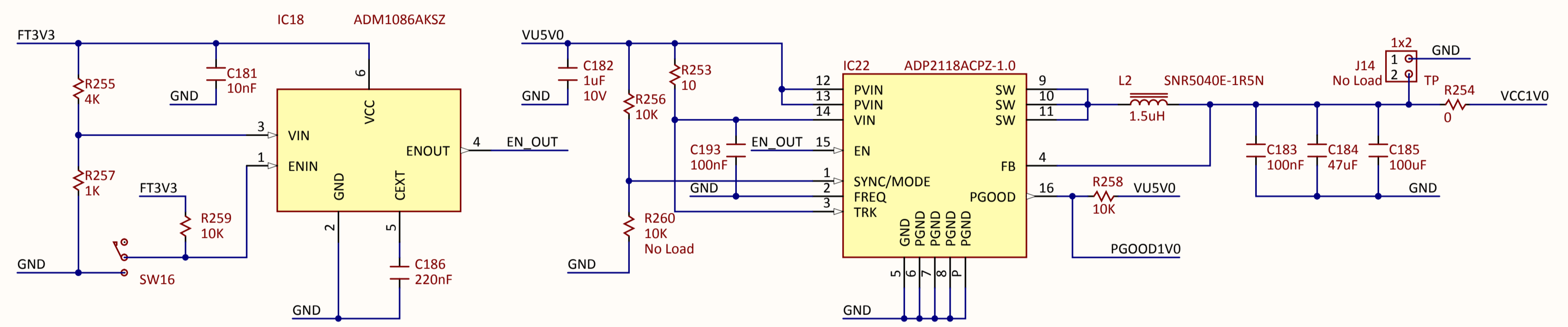
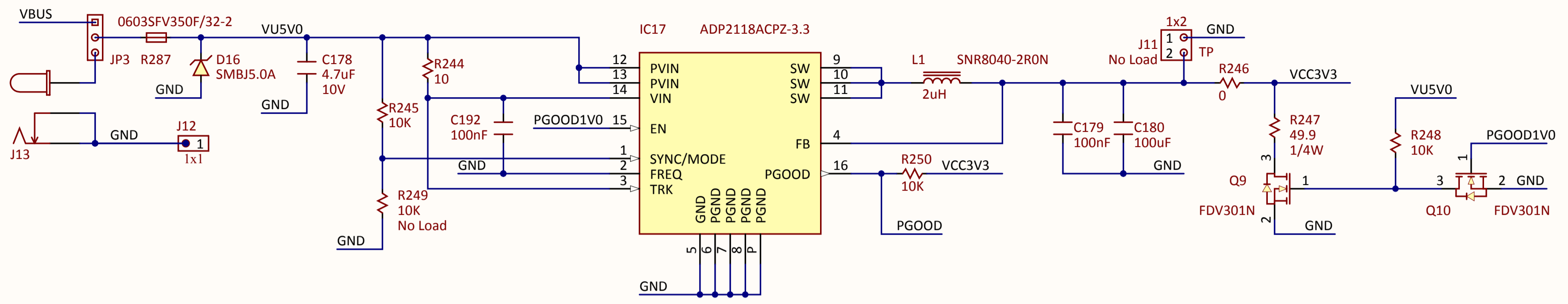
IC8G

PWR/GND



XC7A100T-1CSG324C

Title Nexys 4 DDR		Rev C.1 Copyright 2014
Circuit FPGA POWER		
Doc# 500-292		
Engineer EG		
Author DL		
Date 6/10/2014		
Sheet# 10 out of 11		



For more information on the parts used in this design, please refer to:

- <http://www.analog.com/adp2118> (3 A, 1.2 MHz/600 kHz High Efficiency Synchronous Step-Down DC-to-DC Regulator)
- <http://www.analog.com/adm1086> (Voltage Sequencer with Active High, Push-Pull Enable Output)
- <http://www.analog.com/adp2138> (Compact, 800 mA, 3 MHz, Step-Down DC-to-DC Converter)
- <http://www.analog.com/adp121> (CMOS Linear Regulator, 150 mA, Low Quiescent Current)

Title		Rev	
Nexys 4 DDR		C.1	
Circuit		POWER	
Doc#		500-292	
Engineer		EG	
Author		DL	
Date		6/10/2014	
Sheet#		11 out of 11	