A 4.2-4.7GHz, 3.7mW Digitally Controlled Oscillator RFIC

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***Abstract*: This paper presents an 8-bit LC tuned digitally controlled oscillator (DCO) implemented in a 130nm CMOS technology. The DCO oscillation frequency can be tuned from 4.2 to 4.7GHz with 11.2% tuning range and an average frequency resolution of 2 MHz/bit. The oscillator consumes a 3.7mW power from a 1.2V power supply. The DCO phase noise is measured as -103dBc/Hz @ 500KHz offset and exhibits a figure of merit of -177.**

***Keywords:* PLL, DPLL, oscillator, VCO, DCO, phase noise.**

I. Introduction

Digitally controlled oscillators (DCOs) find wide applications in communication systems. The DCO is a key component for use in digital phase lock loop (DPLL) development that replace analog functions in a PLL synthesizer using digital circuits [1]. So far, low power CMOS technologies have been employed for DCO designs. One of the commonly used CMOS oscillator topologies is the controlled delay ring oscillator that exhibits poor phase noise performance for most RF applications. For low phase noise applications, LC-tuned oscillators are used. However, the oscillation frequency is normally controlled by an analog tune voltage. In deep submicron CMOS process, the voltage headroom is greatly reduced and analog tuning for wide tuning oscillators becomes more and more difficult. Varactors in deep submicron process are highly nonlinear with reduced linear operation region and poor frequency tuning resolution. DCOs implement digital frequency tuning by switching the varactors to achieve one of two distinct capacitance values. The proposed DCO is a differential LC-tuned oscillator with the digital frequency tuning that is achieved by switching an array of capacitances.

II. Binary Weighted Varactor Bank

The varactors are designed using the PMOS transistors, which are well shielded by the n-well and thus less susceptible to the substrate noise. The reduced linear range of the C-V curve and higher oscillator gain (K_{VCO}) in deep submicron process makes the synthesizer deterministic jitter sensitive to ground noise. Also, the variation of K_{VCO} is larger across PVT variations for deep submicron process.

Three distinct regions of operation for the MOS capacitor can be categorized as accumulation region, depletion region and inversion region [3]. When the gate voltage is sufficiently greater than the bulk voltage, the voltage at the oxide semiconductor interface is sufficiently positive to allow the electrons to accumulate and the device is said to operate in the accumulation region. On the other hand, when the bulk voltage is sufficiently larger than the gate voltage, an inversion channel with mobile holes is built up and the MOS capacitor is in its inversion mode.

In order to obtain two distinct capacitance values that can be used as the on and off states of varactors in a DCO design, the MOS capacitors should be prevented from operating in the accumulation region. By connecting the bulk to the highest voltage potential such as the VDD [2], as shown in Fig. 1, the MOS capacitor operates always in either the depletion region or the strong inversion region, which provides two distinct capacitance values for the varactors needed in a DCO.

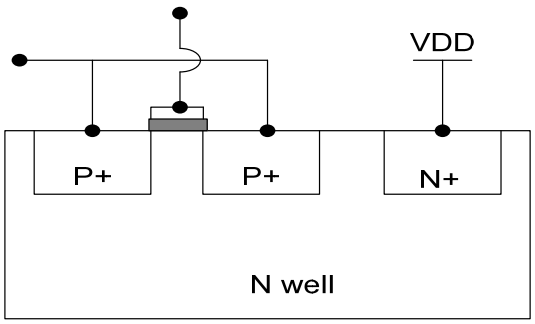

Fig. 1 A PMOS varactor in inversion mode with source and drain terminals tied together and the bulk node connected to VDD.

Moreover, quality factor of the MOS varactor is strongly dependent on the layout. The quality factor is affected by the parasitic resistor in series with the capacitor in a varactor. The series parasitic resistance is due to the combination of gate resistance, inversion channel resistance and the contact resistance to the polysilicon and diffusion. To reduce the loss

due to this resistance, the varactors are laid out in a multi finger structure. In the inversion region, the PMOS channel resistance can be approximated as [4]

$$R_{mos} = \frac{L}{12K_p W(V_{bg} - |V_t|)} \quad (1)$$

where L/W is channel length to width ratio, K_p is the gain factor, V_{bg} represents the bulk to gate voltage and V_t is the threshold voltage. The above equation suggests that *L* should be minimized to reduce the series resistance. The series resistance of the varactor is the sum of the channel resistance and the gate poly resistance. The channel resistance is proportional to L/W, while the poly gate resistance is proportional to W/L. Since the sheet resistivity of the channel is greater than the sheet resistivity of poly, small L and large W should be chosen to minimize the channel resistance, while good care should be taken to make sure that poly gate resistance does not dominate the total resistance.

Although a PMOS varactor has higher parasitic series resistance than the NMOS device, the choice of PMOS is due to the fact that it is less susceptible to the substrate noise and it is well shielded by the n-well. The entire PMOS structure is placed in a common n-well with low resistance n^+ bulk contacts connecting the n-well to VDD between each finger section of the varactor.

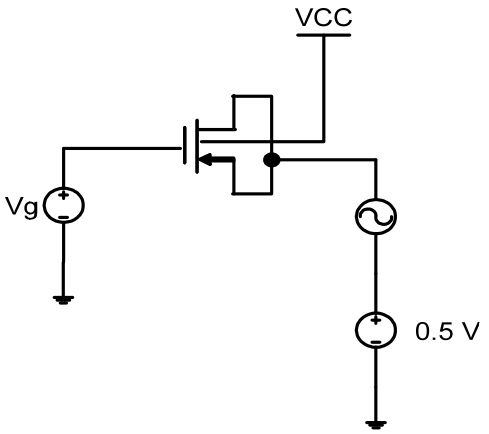

Fig. 2 C-V characteristic of the varactor used in the design. 0.5 V voltage at the source/drain is the dc operating point of that node in the oscillator.

The C-V characteristic of the varactor used in the DCO design was simulated using the setup shown in Figure 2. The 0.5 V voltage source applied at the source/drain terminals is the dc operating point corresponding to that used in the DCO design. The ac source represents the magnitude of the swing at that node. Vg is the bias tuning voltage. The varactor is implemented using two inversion mode transistors such that their drain and source are tied together to the voltage tuning control and the gates are connected in parallel to the DCO tank inductor. Hence the total capacitance seen across the tank is half the value provided by a single transistor.

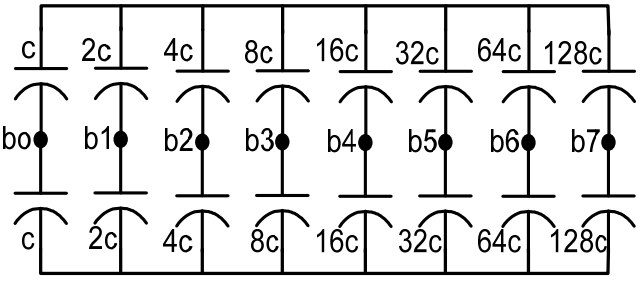

Fig. 3 Binary weighted varactors used to form the DCO tank.

The varactor bank consists of eight binary weighted capacitors shown in Fig. 3. The total varactor capacitance across the tank is controlled by the 8-bit control word (b0 to b7). The tail-to-tail CMOS logic values of the control bits ensure that the varactors are operating either in depletion or inversion mode. The basic unit varactor cell controlled by bit b0 consists of a single MOS transistor with W/L aspect ratio of 20.25/1. Next varactor cell consists of two unit varactors. Using multiplicity of the unit varactor cell ensures better component matching and the parasitic fringing capacitance is also well compensated among the varactors. Figure 4 shows the simulated plot of the effective switching capacitance provided by the 8-bit varactor bank when all the bits are switched from zero to one. The on- and off-capacitances of the tank differ by about 175 fF. This technique also avoids using transistors for switching the caps, which results in better phase noise. The switches usually placed in series with the varactors. The turn-on resistance of the switches would reduce the tank quality factor and degrade the oscillator phase noise [5].

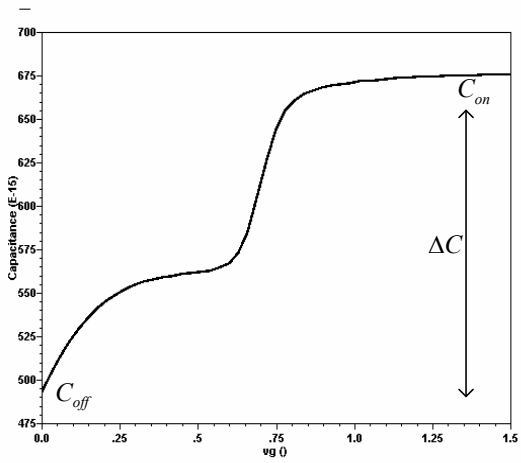

Fig. 4 Simulated maximum and minimum capacitances provided by the 8-bit varactor bank.

III. DCO CIRCUIT DESIGN

Figure 5 shows the schematic diagram of the proposed DCO circuit with the device ratio W/L labeled. The DCO

configuration consists of NMOS and PMOS cross coupled pairs that provide a negative resistance of $-1/g_m$ to overcome the loss due to the parasitic tank resistance. The transistors are sized such that each pair provides half the trans-conductance required to overcome the tank loss. The combination of NMOS and PMOS is chosen because it reduces the power consumption required to achieve the same negative resistance as compared to NMOS only or PMOS only oscillator topologies. CMOS inverters are used as buffers, which provide high impedance to the oscillator output. They are biased with current sources to improve their drive capability.

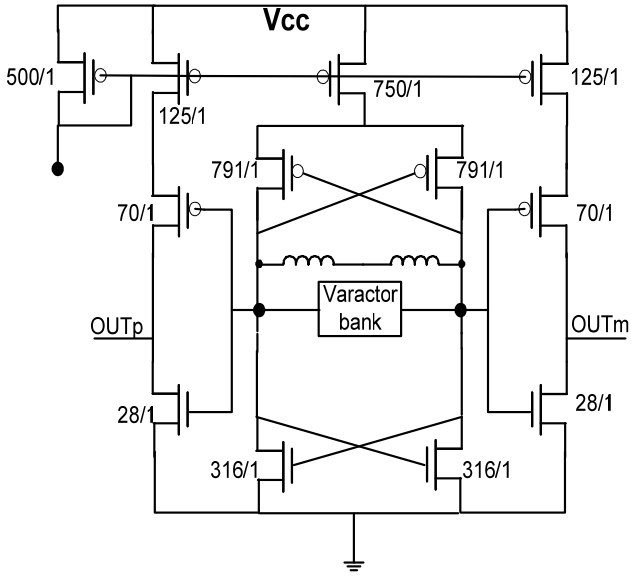

Fig. 5 Simplified DCO circuit schematic diagram.

When all the bits are set to zero, the DCO oscillation frequency is given by

$$F_{osc} = \frac{1}{2\pi\sqrt{LC_{off}}} \tag{2}$$

where C_{off} includes the total off capacitance of the varactor bank shown in Fig. 4, and the junction capacitances of the NMOS-PMOS cross-coupled pairs and other routing capacitances. When the control bits are turned on (set to one), the DCO oscillation frequency becomes

$$F_{osc} = \frac{1}{2\pi\sqrt{L\left(C_{off} + \sum_{n=0}^{7} b_n 2^n \Delta C\right)}} \tag{3}$$

where ΔC is the additional switching capacitance provided by the corresponding bit The frequency resolution of the DCO is given by

$$F_{resolution} = \frac{F_{\max} - F_{\min}}{2^b} \tag{4}$$

where $F_{\max}$ and $F_{\min}$ are the maximum and minimum DCO oscillation frequencies and b represents the number of varactor control bits.

IV. Measured Results

The DCO was designed and fabricated in a 0.13µm CMOS process. The 8-bit DCO oscillates from 4.2 GHz to 4.7 GHz with 11.2% tuning range and provides an average frequency resolution of around 2MHz/LSB. Figure 6 shows the measured K_{DCO} gain curve. Since the varactors are binary weighted, maximum discontinuities in the output frequency can be observed at the periodic intervals of two's power at major bit transitions, when large number of varactors are turned off, causing glitches in the tuning curve.

The die of the DCO RFIC was wire-bonded directly to Ni-Gold plated FR4 test board to facilitate the testing. Figure 7 gives the measured the output spectrum of the oscillator. The power delivered to a 50 ohm load is approximately -7dBm at 4.6GHz. The phase noise was measured using the phase noise utility software in the Agilent 8563EC spectrum analyzer. Figure 8 shows the measured phase noise of the oscillator versus the offset frequency. The phase noise is measured as -103.17dBc/Hz @ 500KHz and -110.8dBc/Hz at 1MHz offset from the 4.7GHz carrier frequency. This design achieves a figure of merit (FOM) of -177dBc/Hz according to the following FOM [6],

$$\text{FOM} = 10\log\left[L(\Delta f)\right] + 10\log\left(\frac{\Delta f^2}{f_{osc}^2}\frac{P_{diss}}{1mW}\right) \tag{5}$$

where $[L(\Delta f)]$ is the measured phase noise, Δf is the carrier offset frequency, f_{osc}^2 is the oscillation frequency, P is the power consumed.

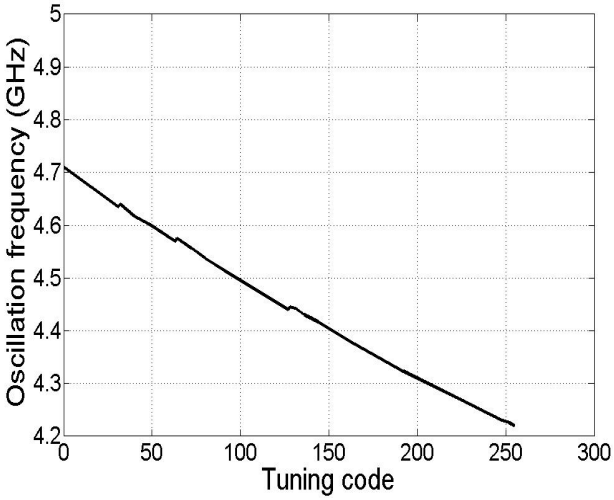

Fig. 6 Measured DCO output frequency versus tuning code.

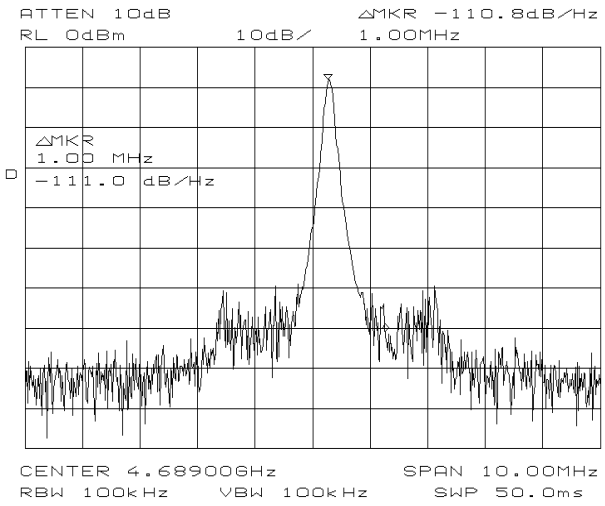

Fig. 7 Measured DCO output spectrum. The output power delivered to a 50 ohm load is -7dBm.

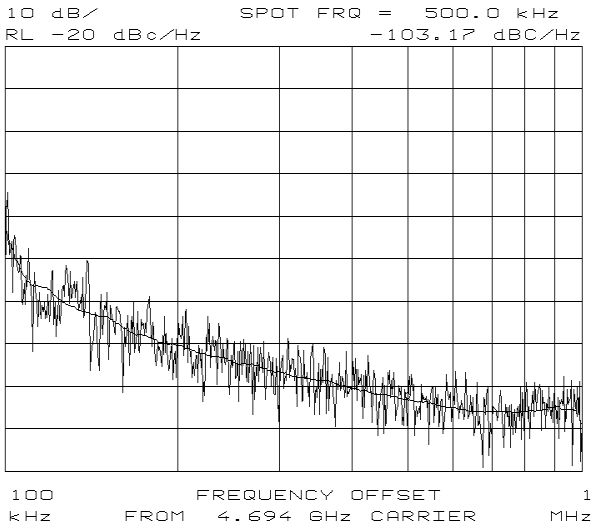

Fig. 8 Measured DCO phase noise versus offset frequency. The phase noise is -103dBc/Hz @ 500kHz offset from the 4.7GHz carrier frequency.

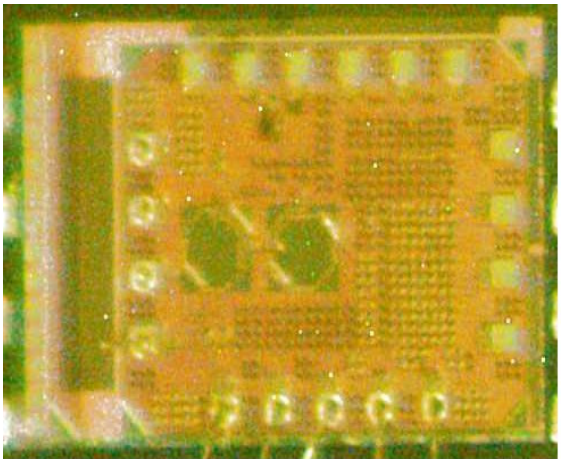

Fig. 9 Die photo of the 8-bit DCO RFIC.

The DCO oscillator core consumes a current of 3.1mA from a 1.2V supply. Figure 9 shows the DCO micrograph with the die area of 1.7mm × 1.3mm including the pads. Table I summarizes the proposed DCO performances compared to the previously published DCO designs. Comparing to other works, this DCO design achieves equivalent FOM with wide tuning range at higher oscillation frequency. The DCO RFIC operates under 1.2 V supply with 3.7mW power consumption and exhibits a measured phase noise of -103 dBc/Hz @ 500KHz that leads to a FOM of -177. The DCO chip outputs 4.7GHz signal with -7 dBm power on a 50 Ohm load.

Table I. DCO performance comparison.

Ref.	[2]	[6]	This work
Technology	130nm CMOS	65nm CMOS	130nm CMOS
Supply (V)	2.5	1.1	1.2
f_{OSC} (GHz)	2.4	10	4.5
Tune range	20.8%	10%	11.2%
L (dBc/Hz)	-112	-102	-103.17
Offset Δf	500 KHz	1 MHz	500 KHz
P_{diss}	3.4 mW	3.3 mW	3.7 mW
FOM	-180	-177	-177

V. Conclusions

We have presented a 4.5GHz 8-bit digitally controlled oscillator fabricated in a 130nm CMOS technology. The oscillation frequency can be tuned from 4.2 to 4.7GHz with an average frequency resolution around 2 MHz/bit. The DCO exhibits -177dBc/Hz measured figure of merit.

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