Noise Figure Measurement Using Mixed-Signal BIST

Jie Qin, Charles Stroud, and Foster Dai
Dept. of Electrical and Computer Engineering, 200 Broun Hall
Auburn University, Alabama 36849-5201, USA

***Abstract*—A Built-In Self-Test (BIST) approach for functionality measurements, including noise figure (NF), linearity and frequency response of analog circuitry in mixed-signal systems, is presented. The BIST circuitry consists of a direct digital synthesizer (DDS) based test pattern generator (TPG) and a multiplier/accumulator based output response analyzer (ORA). The BIST approach has been implemented in hardware and used for actual NF measurements for comparison with measurements from external test equipment.**

I. INTRODUCTION

Mixed-signal Built-In Self-Test (BIST) is now in more demand than ever. Analog functionality tests based on the traditional methodology of manual testing costs much more money and time due to the ever-increasing operational frequency and complexity of modern mixed-signal integrated circuits (ICs). For example, RFIC test cost can be as high as 50% of the total cost, depending on the complexity of the functionality to be tested [1]. The operational frequency and complexity of modern mixed-signal ICs make it difficult to perform tests on these ICs. With a rapidly increasing level of integration, the number of input/output (IO) pins does not increase accordingly such that observability of internal components is lower compared with traditional ICs [2]. Therefore, it becomes more attractive to automate the analog testing process with low-cost, built-in test circuitry.

In order to perform a suite of analog functionality tests in a BIST environment, such as linearity, frequency response, and noise figure (NF) measurements, the frequency spectrum of the signal coming from the device under test (DUT) needs to be measured and analyzed by an output response analyzer (ORA) included in the BIST circuitry [3]. A few techniques have been proposed to perform on-chip frequency-domain testing of mixed-signal circuits in [4]–[7]. However, most of these approaches focus only on one or two simple parameter tests such as cut-off frequency of a filter and cannot perform complete analog tests such as frequency response, linearity, noise measurements [1].

A new mixed-signal BIST approach has been proposed based on direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based ORA. Because the signal is in digital form, it is easy to include different modulation capabilities in the DDS. Therefore, many analog functional tests, such as magnitude and phase response in the frequency domain, 3rd order intercept point (IP3) and noise figure (NF) can be performed in such an architecture [1]. Some experimental results for IP3 and frequency response (both phase and gain) using this BIST architecture have been presented in [1] to demonstrate the feasibility and accuracy of the BIST approach.

In this paper, we show how the proposed BIST approach can be extended from the current suite of functional measurements to include NF measurements of the analog circuitry in a mixed-signal IC or system. The paper is organized as follows. An overview of the BIST approach is given in Section II. Next, the theoretical background of NF measurement and how the measurement is conducted in our BIST architecture are presented in Section III. Some experimental results of actual hardware NF measurements are given in Section IV. Finally, we summarize the paper in Section V with some concluding remarks.

II. OVERVIEW OF BIST APPROACH

The mixed-signal BIST architecture, illustrated in Figure 1, includes a DDS-based TPG, a MAC-based ORA, and a test controller [1]. The test scheme utilizes the existing digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) typically associated with most mixed-signal architectures to minimize the hardware added for BIST. The only test circuitry added to the analog domain is loopback capabilities needed to facilitate return paths for test signals to the ORA. The number and location of loopback capabilities determines the accuracy and resolution of tests and measurements associated with a given analog function.

The DDS-based TPG consists of three numerically controlled oscillators (NCOs) and utilizes an existing DAC from the mixed-signal system to complete the DDS. Figure 2 shows a more detailed view of an NCO used in the TPG. The phase accumulator is used to generate the phase word based on the frequency word f and initial phase word θ. A look-up table is utilized to convert the truncated phase word sequence to a digital sine wave sequence. The output sine wave frequency is determined as

$$f' = \frac{f \cdot f_{clk}}{2^n}, \qquad (1)$$

where n is the word width of the phase accumulator.

1-4244-0921-7/07 $25.00 © 2007 IEEE.

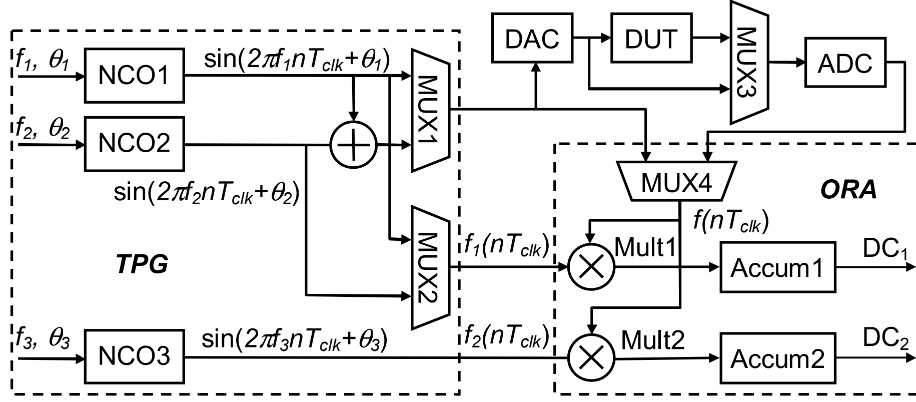

Figure 1. General model of BIST architecture

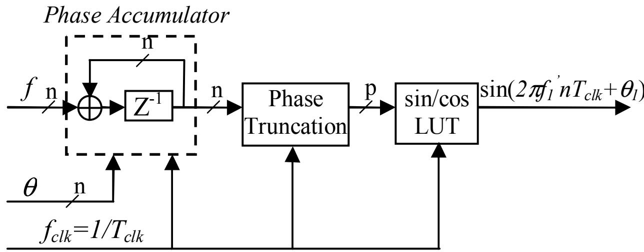

Figure 2. NCO used in TPG

The ORA consists of an $N\times N$-bit multiplier and an M-bit accumulator. In the design of the ORA, N is the number of bits from the DDS and ADC and M is chosen such that $K<2^M$, where K is the length of the BIST sequence in clock cycles. While performing frequency response, linearity and NF measurements, $f_1(nT_{clk})$ and $f_2(nT_{clk})$ (refer to Figure 1) are set to $cos(\omega nT_{clk})$ and $sin(\omega nT_{clk})$, respectively. As a result, the DC_1 and DC_2 accumulator values can be described as

$$\mathrm{DC}_1 = \sum_n f(nT_{clk}) \cdot \cos(\omega nT_{clk}), \tag{2}$$

$$\mathrm{DC}_2 = \sum_n f(nT_{clk}) \cdot \sin(\omega nT_{clk}) \cdot \tag{3}$$

Reference [3] presents three approaches to calculate the amplitude response $A(\omega)$ and phase response $\Delta\phi(\omega)$ using DC_1 and DC_2 and points out that the most preferable approach for NF, linearity and frequency response measurements is based on (4) and (5) as follows

$$A(\omega) = \sqrt{DC_1^2 + DC_2^2}\,. \tag{4}$$

$$\Delta\phi(\omega) = -tg^{-1}\frac{DC_2(\omega)}{DC_1(\omega)}, \tag{5}$$

In order to achieve accurate results for analog functional measurements, not only must the DUT's phase response be considered and measured as in Equation (5), but also the phase delay caused by the BIST circuitry itself (including the DAC and ADC) needs to be measured for calibration of measurements [1][3]. This is done by controlling MUX3 in Figure 1 to select the signal path without the DUT to measure and calibrate for phase delay in the BIST circuitry.

III. NOISE FIGURE MEASUREMENT

Noise figure (NF) measurement is an important analog functionality test along with the IP3 and frequency response measurements. Noise introduced by analog circuitry includes thermal noise, shot noise, flicker noise, etc. [8]. The noise from these sources will be mixed together with the signal of interest. The more noise that is introduced by circuit components, the more difficult it is to extract the signal of interest. Therefore, the noise is a critical issue to any electrical system's performance. If the noise introduced by critical components, like low noise amplifiers (LNAs), can be measured in the system, it will be much easier for IC and system manufacturers to test and diagnose potential problems related to noise in mixed-signal systems. Therefore, it is important to include NF measurements in the BIST approach.

There are two important parameters widely used to characterize the system noise. One is the signal-to-noise ratio (SNR), which is defined as

$$SNR = \frac{Signal\ Power}{Noise\ Power\ in\ Interested\ Bandwidth} \tag{6}$$

Alternatively, the noise added in a circuit can be characterized by the noise figure (NF), which is defined as

$$NF = \frac{SNR_{in}}{SNR_{out}}, \tag{7}$$

where SNR_{in} and SNR_{out} are the SNRs measured at the input and output of the circuit, respectively [8].

The noise introduced by a DUT can be mathematically modeled as illustrated in Figure 3 where $y_{out}(t)$ is the response of the DUT's ideal model to the input signal $y_{in}(t)$, while $y_n(t)$ represents the noise generated by the DUT. Without loss of generality, $y_n(t)$ is usually assumed to be a white Gaussian additive noise. The measurement of noise is computed in the frequency domain instead of the time domain mainly due to the following two factors. First, it is very hard to estimate $y_n(t)$'s power from the time domain and, second, even if we can find a way to determine $y_n(t)$'s power, it is still meaningless because we only care about the noise over the bandwidth of interest, which is usually much smaller than $y_n(t)$'s real power [2][8].

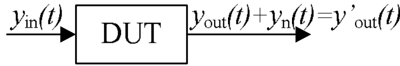

Figure 3. Noise introduced by DUT

According to the periodogram method [9], the noise's power spectrum density (PSD) in sampled discrete format can be expressed as

$$S(k)=\frac{1}{Nf_{clk}}\left|\sum_{n=0}^{N-1}\left[y'_{out}(nT_{clk})-y_{out}(nT_{clk})\right]e^{j\frac{2\pi}{L}nk}\right|^2 \quad (8)$$

Usually, Equation (8) can be computed through the FFT algorithm. However, there is a large area penalty and power consumption associated with an on-chip (or in-system) FFT processor [3][7]. To perform the NF measurement in our BIST approach (refer to Figure 1), NCO1 in the TPG of the BIST circuitry generates a sine wave $sin(\omega_1 t)$ to stimulate the DUT. At the same time, an in-phase tone and an out-of-phase tone at frequency ω_2 are produced by NCO2 and NCO3, respectively, and fed into the ORA. In this case, frequency words to NCO2 and NCO3 were be the same, $f_2 = f_3$, while θ_2 and θ_3 are used to control the in-phase and out-of-phase tones at frequency ω_2. By sweeping ω_2 over the frequency band of interest, the ORA can then obtain $y'_{out}(t)$'s spectrum information as illustrated in Figure 4. Since the signal of interest only appears at frequency f_1, the spectrum of the noise $Y_n(f)$ can be easily obtained from the samples at all other frequencies. Then the noise's PSD and SNR can be measured based on Equations (8) and (6), respectively. The test controller is capable of bypassing the DUT through MUX3 (see Figure 1) such that input and output SNRs of the DUT can be measured. From these two SNRs, the NF of the DUT can be determined using Equation (7).

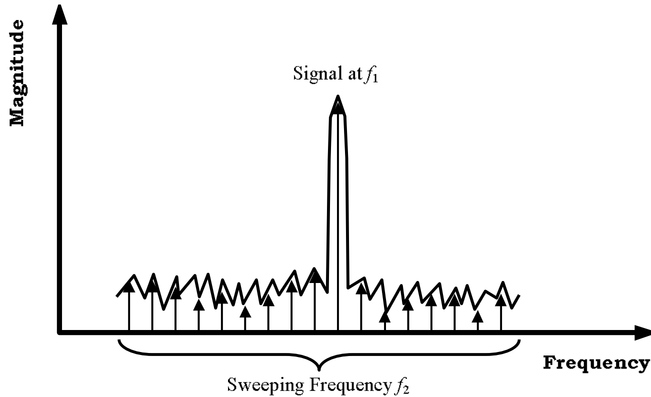

Figure 4. SNR measurement using BIST

IV. EXPERIMENTAL RESULTS

In order to prove the effectiveness and feasibility of the proposed BIST architecture for NF measurements of analog circuitry in addition to linearity and frequency response measurements, we implemented the BIST architecture shown in Figure 1 in hardware. The digital portion of the BIST circuitry was implemented in a Xilinx Spartan XC2S50 Field Programmable Gate Array (FPGA) on an XSA50 printed circuit board (PCB). A DAC (AD9752AR by Analog Devices) with low-pass filter and an 8-bit ADC (AD9225AR by Analog Devices) were implemented on another PCB. An op-amp built on a separate board served as the DUT for the NF measurement.

A. NF Measurement using External Test Equipment

In order to verify the accuracy of the BIST-based NF measurement, a reference NF measurement was conducted using external test equipment, including an Agilent 33250A waveform generator and an Agilent 8563EC spectrum analyzer. The DUT was driven by the waveform generator and the DUT's input and output were analyzed by the spectrum analyzer with a *resolution bandwidth* (RBW) of 100Hz. The spectrum of the DUT's input and output were captured and are shown in Figures 5 and 6, respectively. It should be noted that the maximum signal level in Figure 5 coincides with the top of the plot.

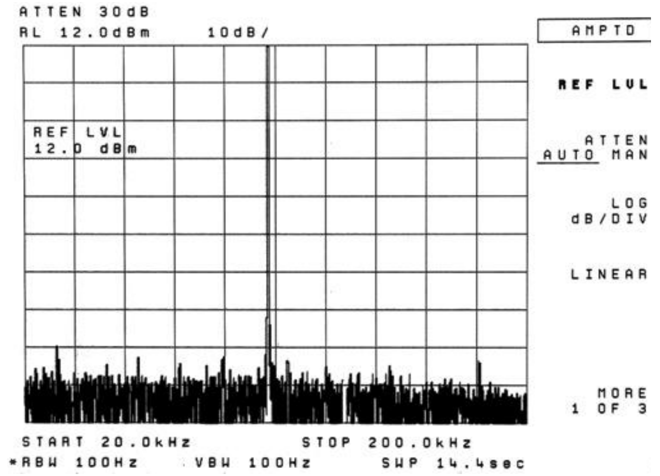

Figure 5. DUT input spectrum analyzer SNFR measurement of 90 dBc/Hz

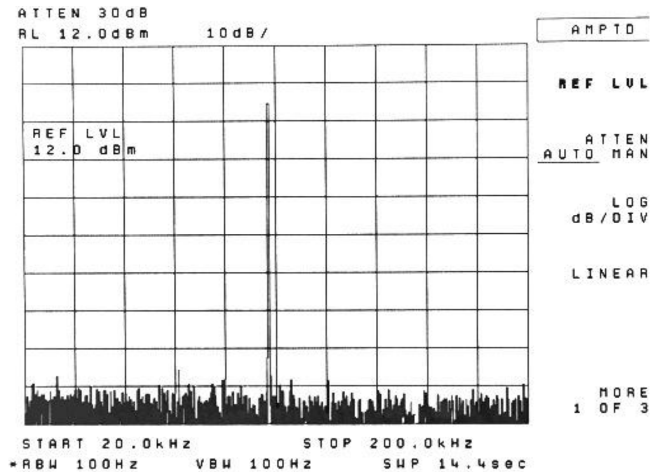

Figure 6. DUT output spectrum analyzer SNFR measurement of 76 dBc/Hz

It is known from [10] that the SNR can be read from the spectrum analyzer as follows

$$SNR = SNFR - 10\log_{10}\left(f_s / (2 \bullet RBW)\right), \quad (9)$$

where *SNFR* is the signal-to-noise floor ratio displayed directly on the spectrum analyzer. The $SNFR_{in}$ and $SNFR_{out}$ at the DUT's input and output as read from these two figures are 90 dBc/Hz and 76 dBc/Hz, respectively. The DUT's NF can be now be calculated as follows

$$NF_1 = SNFR_{in} - SNFR_{out} = 90 - 76 = 14dB \qquad (10)$$

B. NF Measurement using BIST circuitry

The BIST-based NF measurement was conducted and the actual input and output spectrums obtained from the BIST circuitry are shown in Figures 7 and 8, respectively. From these two figures, the $SNFR_{in}$ and $SNFR_{out}$ of the DUT are read as 60 dBc/Hz and 45 dBc/Hz, respectively, using the noise floor indicated in the figures. The DUT's NF can be calculated in the same way as Equation (10) and the result is

$$NF_2 = SNFR_{in} - SNFR_{out} = 60 - 45 = 15dB \qquad (11)$$

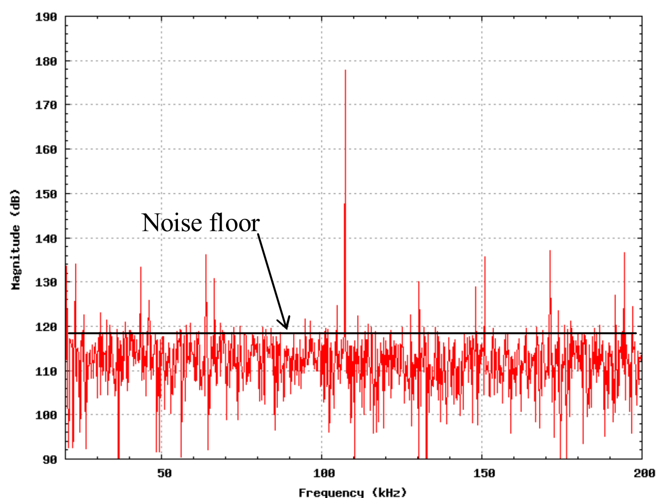

Figure 7. DUT input BIST-based SNFR measurement of 60 dBc/Hz

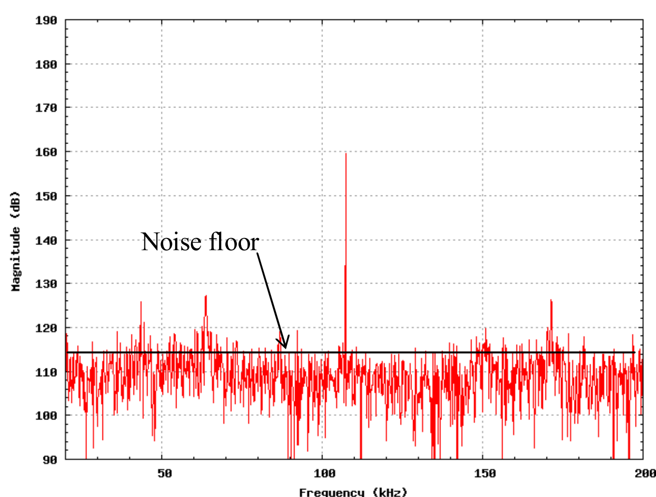

Figure 8. DUT output BIST-based SNFR measurement of 45 dBc/Hz

Comparing the NF_1 from Equation (10) using external test equipment and NF_2 from Equation (11) using the BIST circuitry, we find that there is only 1 dB difference between the two measurements. This illustrates the feasibility and accuracy of the BIST approach for NF measurements. One possible reason for the 1dB difference is the choice of noise floor for the measurement indicated in the figures. Another possible reason is switching noise produced by the FPGA that is not observed by the external test equipment.

V. Conclusions

A BIST approach for analog circuit functional tests, including NF measurements as well as linearity and frequency response, in mixed-signal systems was presented. The experimental results show the feasibility and accuracy of the BIST architecture for on-chip NF measurements. The BIST architecture has been implemented in Verilog and parameterized for specification of the desired size of the DDS-based TPG and MAC-based ORA based on the sizes of the DAC and ADC targeted for the mixed-signal system. The BIST implementation is efficient in terms of area and easily fits into the smallest FPGAs on the market. As a result, it can be easily incorporated in any mixed-signal system design. This facilitates permanent residence of the BIST circuitry in system applications with access to the DAC/ADC pair for on-chip analog functional test and measurement. It should be noted that the BIST architecture shown in Figure 1 includes all of the circuitry, features, and capabilities needed for linearity and frequency response (both gain and phase) measurements as well as NF measurement. Furthermore, the NF measurement requires only a subset of the circuitry shown in Figure 1 and does not impose any additional circuitry on the existing BIST architecture.

References

[1] F. Dai, C. Stroud, and D. Yang, "Automatic Linearity and Frequency Response Tests with Built-in Pattern Generator and Analyzer," *IEEE Trans. on VLSI Systems*., vol. 14, no. 6, pp. 561-572, 2006.

[2] M. Bushnell and V. Agrawal, *Essentials of Electrnonic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2006.

[3] J. Qin, C. Stroud, and F. Dai, "Phase Delay Measurement and Calibration in Built-In Analog Functional Test," to be published in *Proc. IEEE Southeastern Symp. on System Theory*, March 2007.

[4] C.-Y. Chao, H.-J. Lin, and L. Milor, "Optimal Testing of VLSI Analog Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 16, no. 1, pp. 58-76, 1997.

[5] M. Toner and G. Roberts, "A BIST Technique for a Frequency Response and Intermodulation Distortion Test of a Sigma-Delta ADC," *Proc. IEEE VLSI Test Symp*., pp. 60-65, 1994.

[6] B. Provost and E. Sanchez-Sinencio, "On-chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test," *IEEE J. Solid-State Circuits*, vol. 38, pp. 263-273, 2003.

[7] J. Emmert, J. Cheatham, B. Jagannathan, and S. Umarani, "An FFT Approximation Technique Suitable for On-Chip Generation and Analysis of Sinusoidal Signals", *Proc. IEEE International Symp. on Defect and Fault Tolerance in VLSI Systems*, pp. 361-367, 2003.

[8] B. Razavi, *RF Microelectronics*, Prentice-Hall, 1997.

[9] A. Oppenheim and R. Schafer, *Discrete-Time Singal Processing,* Prentice-Hall, 1989.

[10] W. Kester, Editor, *Analog-Digital Conversion*, Analog Devices Inc, 2004.