A 5-GHZ Low-Power Series-Coupled BiCMOS Quadrature VCO With Wide Tuning Range

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***Abstract*—This letter presents a novel quadrature voltage controlled oscillator (QVCO) implemented in a 47-GHz SiGe BiCMOS technology. The QVCO is a serially coupled LC VCO that utilizes SiGe heterojunction bipolar transistors for oscillation and metal oxide semiconductor field effect transistors for coupling. The SiGe BiCMOS QVCO prototype achieves about 14.6% tuning range from 4.3 to 5 GHz. The phase noise of the QVCO is measured as −114.3 dBc/Hz at 2-MHz offset. The 5-GHz QVCO core consumes 6-mA current from a 3.3-V power supply and occupies 0.88 mm^2 area.**

***Index Terms*—BiCMOS, oscillator, phase noise, quadrature voltage controlled oscillator (QVCO), SiGe.**

I. Introduction

WIRELESS transceivers require quadrature local oscillator (LO) generation for up- and down-conversions with image-reject mixing. There are various ways to generate quadrature signals: 1) A divide-by-two frequency divider following the voltage controlled oscillator (VCO) running at double the LO frequency. This approach generally shows poor phase noise and quadrature accuracy, as it requires a 50% duty cycle for VCO output. 2) A divide-by-four frequency divider following the VCO running at four times that of the LO frequency. Although this approach doesn't need a 50% duty cycle for VCO output, it requires the VCO to operate at much higher frequency, which leads to higher power consumption. 3) A VCO followed by a passive poly-phase RC complex filter. An integrated poly-phase network is narrow band with poor quadrature accuracy. A typical RC phase filter also loads the VCO and has large loss such that a power hungry buffer is needed after the poly-phase filter. It becomes harder to implement the poly-phase filters for high frequency (e.g., beyond 5 GHz) due to the reduced R and C component values that become more sensitive to parasitics and process variation. 4) Two VCOs are forced to run in quadrature using transistor or transformer coupling. This technique provides wide-band quadrature accuracy and superior phase noise performance at the expense of increased power and silicon area. It should be pointed out that the power and area for quadrature VCO option may not be a disadvantage comparing to the power-hungry and bulky poly-phase filter option.

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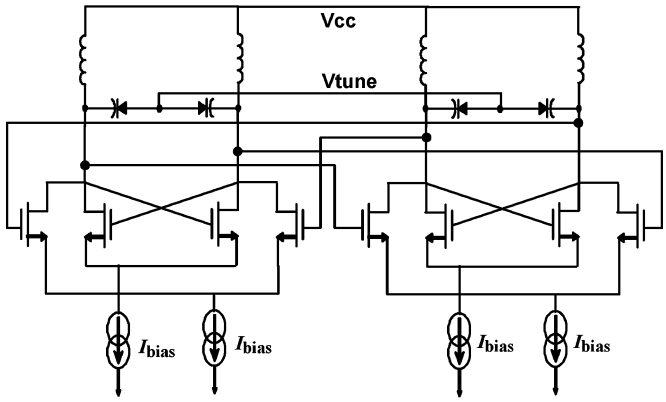

Fig. 1. Prior art P-QVCO circuit schematics.

There are various ways to couple the two VCOs and lock their oscillation frequency. The most common quadrature VCO (QVCO) topology shown in Fig. 1 utilizes the parallel coupling proposed by Rofougaran *et al.* [1]. The parallel VCO (P-QVCO) delivers quadrature signals with low phase and amplitude errors, yet it consumes large current to bias both the oscillation and coupling transistors. QVCOs can also be serially coupled by placing the coupling transistors in series with the oscillation transistors [2], [4]. By connecting the coupling transistors in series in a cascode current reuse topology, the series QVCO (S-QVCO) reduces the noise from the cascode devices and provides better isolation between the VCO outputs and its current sources. In the P-QVCO and S-QVCO reported so far, the same type of transistors has been used for oscillation and coupling.

II. Proposed S-QVCO Topology

This letter presents a novel QVCO implemented in a 47-GHz SiGe BiCMOS technology with minimum allowable channel length being 0.5 μm. The proposed QVCO is a series-coupled LC VCO that utilizes SiGe heterojunction bipolar transistors (HBTs) for oscillation and metal oxide semiconductor field effect transistors (MOSFETs) for coupling. The oscillation NPN transistors achieve high oscillation frequency and low phase noise, while the NMOS coupling transistors provide more headroom, better isolation and increased tuning range.

The proposed S-QVCO circuit is illustrated in Fig. 2, in which the NPN transistors Q1 and Q2 form a cross-coupled negative transconductance LC-tuned VCO and Q3 and Q4 form another identical LC-tuned VCO. The coupling between the two VCOs is realized using four NMOS transistors M1, M2, M3, and M4. Thus, the proposed S-QVCO utilizes different types of transistors for oscillation and coupling. The advantages of this technique will be discussed in the coming paragraphs.

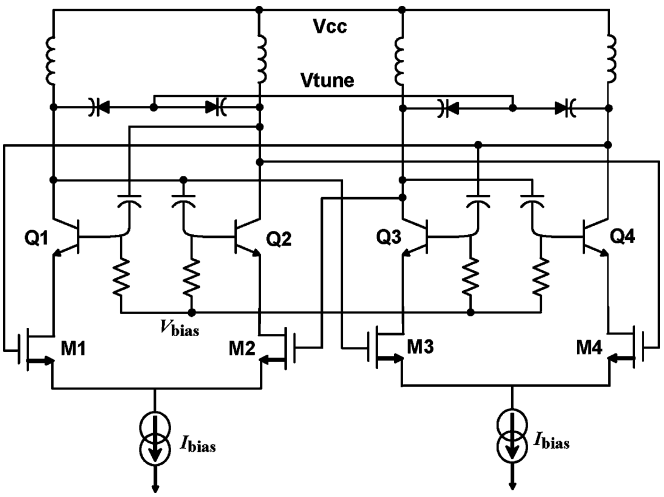

Fig. 2. Proposed S-QVCO circuit schematics using NPN for oscillation and NMOS for coupling.

Compared to a P-QVCO, the S-QVCO achieves lower current consumption, since the coupling and oscillation transistors share the same bias current. In a P-QVCO, the coupling pair of transistors usually consumes an additional 30%–40% of the core oscillator current for reasonable compromise between phase noise and phase error. In an S-QVCO, the coupling transistors are in series with the $-g_m$ transistors. Additional bias currents are not required for the coupling transistors, resulting in considerable power saving. Also, the coupling and oscillation transistors are connected in a cascode manner such that the noise coming from the coupling transistors and current sources are isolated from the LC-tank that is connected to the VCO outputs. The phase noise and phase error are relatively independent of each other in this topology. However, for the same voltage supply, the S-QVCO has less voltage headroom for output swing due to the insertion of the coupling transistors.

As known, NPN transistors can achieve higher oscillation frequency due to enhanced unit power gain bandwidth product, $f_{\max}$, of the devices. On the other hand, NMOS transistors have higher output impedance, reduced voltage headroom requirements between the drain and source, and much relaxed bias scheme compared to their BJT counterparts. Since both types of transistors are available in a BiCMOS technology, we can combine the advantages of both types of transistors and achieve better QVCO performance. By using NPN transistors for oscillation, high oscillation frequency can be achieved. By using MOS transistors for coupling, higher output swing can be provided due to the reduced headroom required by the MOS transistors. The larger swing for the VCO output leads to lowered phase noise. In the proposed S-QVCO, the MOS coupling transistors are directly connected to the VCO output nodes, providing a much easier biasing scheme.

The bias current of the S-QVCO is selected to provide the trans-conductance of $g_{m,osc} \geq \chi R_{\tan k}$, where $R_{\tan k}$ is the effective resistance (loss) of the tank and χ is an empirical parameter with value from three to five to provide design margin for reliable VCO startup. Having determined the bias current, the emitter length of the NPN transistor is chosen such that it operates at close to its peak f_T. The emitter length chosen in this design is 7 μm.The oscillation frequency of the S-QVCO is given by $f_{osc} = (2\pi\sqrt{LC})^{-1}$, where C is the total capacitance seen across the inductors which includes the varactor capacitance C_v and the fixed parasitic capacitance C_p. The VCO frequency tuning range (FTR) can be found as

$$FTR = \frac{C_p + C_{v\max}}{C_p + C_{v\min}}. \tag{1}$$

The fixed parasitic capacitance C_p consists of the parasitic capacitance contributed by the inductor, the varactor, and the junction capacitances of the coupling and oscillating transistors. For high frequency oscillation, this fixed capacitance contributes a large portion to the overall LC-tank capacitance and thus limits the tuning range and maximum attainable oscillation frequency. To a first-order approximation, the fixed capacitance provided by the oscillating transistor for the P-QVCO can be found as $(1/2)C_\pi + 2C_\mu$ for the bipolar version and $(1/2)C_{gs} + 2C_{gd}$ for the MOSFET version.

The total fixed capacitance seen across the LC-tank for S-QVCO and P-QVCO shown in Figs. 2 and 1 are given by (2) and (3), respectively

$$C_P = 2C_\mu + \frac{C_{gs}}{2} + \frac{C_\pi C_{gd} C_{gs}}{2(C_\pi C_{gd} + C_\pi C_{gs} + C_{gs} C_{gd})} \tag{2}$$

$$\text{and } C_p = 2C_{gd} + C_{gs} + \frac{1}{2}\left(\frac{C_{gd} C_{gs}}{C_{gd} + C_{gs}}\right). \tag{3}$$

As shown in the above equations, the use of MOS transistors for serial coupling considerably reduces the fixed parasitic capacitance seen across the tank due to the increased capacitive degeneration (C_{gs} and C_{gd}) of the serially coupled MOS transistors at the emitter terminals of the $-$gm pairs. This enables more tuning range and maximum attainable oscillation frequency. For high frequency oscillation, where the influence of parasitics becomes dominant, the S-QVCO provides a better topology for quadrature signal generation than the P-QVCO topology.

The NMOS coupling transistors are sized with aspect ratio of 24/1 such that they provide about the same gm as that of the NPN transistors. This balances the load impedance of the tanks, which leads to reduced quadrature phase/amplitude errors and improves the phase noise as well. While the above argument would also be valid if we use bipolar transistors for coupling instead of MOS, the bipolar version of the S-QVCO would require current consuming level shifters and would consume larger headroom for coupling transistors.

III. Measured Results

The 5-GHz series-coupled quadrature oscillator was implemented in a 47-GHz SiGe BiCMOS technology with four metal layers. The circuit occupies a die area of 0.88 mm^2.The VCO core consumes 6 mA of current from a 3.3-V supply.

As shown in Fig. 3, the series-coupled quadrature oscillator achieves phase noise of -114 dBc/Hz at 2-MHz offset from the carrier at 4.67 GHz. Fig. 4 gives the measured phase noise versus the offset frequencies, indicating that the wideband noise of the VCO at -120 dBc/Hz at 10-MHz offset. The measured oscillation frequency versus the tuning voltage, i.e., the reverse bias voltage across the varactor, is given in Fig. 5.

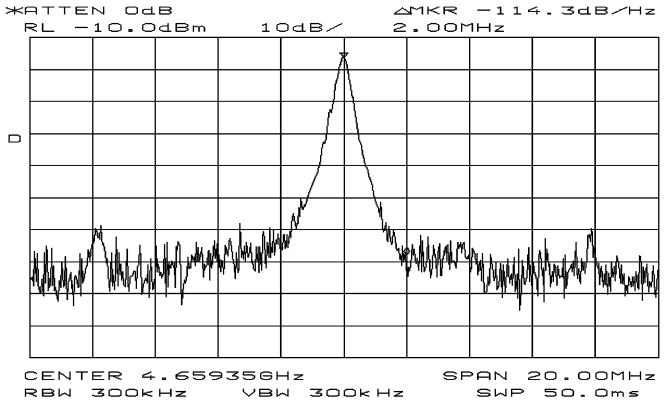

Fig. 3. Measured QVCO output spectrum. The phase noise is measured as −114.3 dBc/Hz at 2-MHz offset from the carrier.

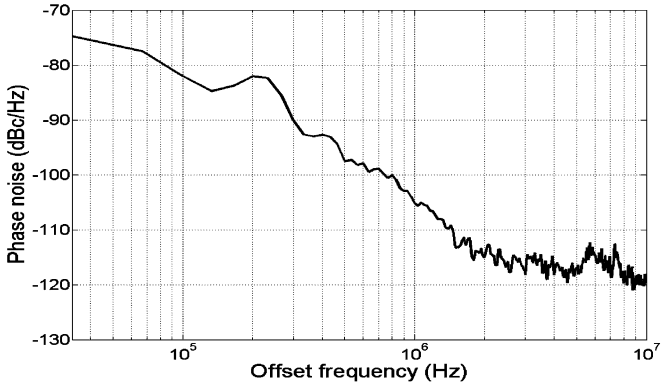

Fig. 4. Phase noise versus offset frequency. The phase noise is measured as −114.3 dBc/Hz at 2-MHz offset from the carrier.

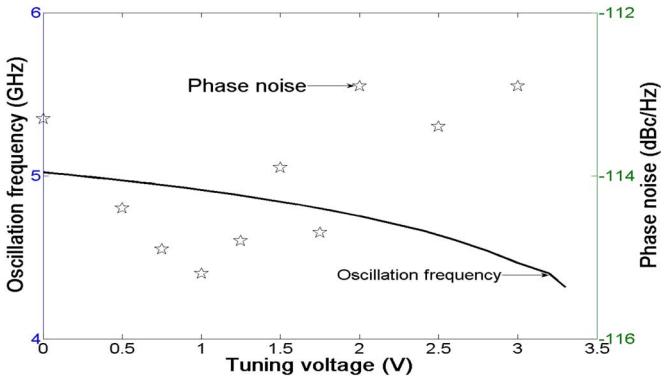

Fig. 5. Measured oscillation frequency and phase noise versus tuning voltage. The measured tuning range is from 4.3 to 5 GHz.

As shown, the tuning range of the oscillator covers from 4.32 to 5 GHz when tuning voltage is from 0 V to the supply voltage. The achieved high tuning range of 14% is due to the coupling MOSFET transistors in series with $-g_m$ pairs. With the wide tuning range, the oscillator also achieves fairly linear VCO tuning gain (k_{vco}), which is important to avoid VCO chirping and pulling in phase locked loop synthesizer designs. The measured VCO gain is about 206 MHz/V. Fig. 5 shows the measured oscillator phase noise versus the tuning voltage. The maximum variation in phase noise at 2-MHz offset over the entire tuning range is 2.3 dBc/Hz. Thus, the VCO achieves better than −113 dBc/Hz phase noise at 2-MHz offset over the entire 14% wide tuning range.

TABLE I
QUADRATURE VCO PERFORMANCE COMPARISON [3]

Ref.	[1]	[2]	[3]	[5]	This work
Topology	P-QVCO	CMOS S-QVCO	P-QVCO	P-QVCO	BiCMOS S-QVCO
f_{OSC}(GHz)	0.9	1.8	5	12	5
Tune range	17%	18%	6.4%	37%	14.6%
L (dBc/Hz)	-110	-140	-115	-112	-114.3
Offset Δf	1 MHz	3 MHz	2 MHz	10 MHz	2 MHz
Core P_{diss}	30 mW	50 mW	21mW	39 mW	19.8 mW
FOM	154	178	169	157	169

Table I compares the performance of this quadrature oscillator to the previously published QVCO designs. Comparing to other 5-GHz QVCO designs, this P-QVCO design achieves one of the best figure-of-merits (FOM) defined as $-10\log(L(\Delta f)) - 10\log((\Delta f^2/f_{osc}^2)(P_{diss}/1\text{ mW}))$. The proposed S-QVCO also achieved the widest tuning range at 5 GHz with low power consumption compared to other LC-tuned QVCO designs. Reference [5] gives a 37% wide tuning range VCO using switch capacitor topology, which is intrinsically noisy.

IV. CONCLUSION

We presented a novel series-coupled quadrature oscillator implemented in a 47-GHz BiCMOS SiGe technology. The BiCMOS S-QVCO uses NPN transistors for oscillation and NMOS devices for coupling. The oscillator prototype achieves greater than 14% tuning range from 4.3 to 5 GHz. The oscillator phase noise is measured as −114.3 dBc/Hz at 2-MHz offset from the carrier. The power consumption of the 5-GHz QVCO core is 3 mA per tank with a 3.3-V supply. The proposed S-QVCO achieves one of the best figure-of-merits at 5-GHz oscillation frequency reported so far.

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