A 10GHz Nonlinear Cosine-Weighted Digital-to-Analog Converter For High-Speed Direct Digital Synthesis

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Abstract **— A SiGe cosine-weighted digital-to-analog converter (DAC) with 10GHz sampling rate is presented. The nonlinear DAC is used in a direct digital synthesis (DDS) to replace the conventional look up table and the linear DAC. It takes the advantage of high switching speed of SiGe current switches and uses the current mode logic (CML) circuits to realize the digital control logics. The DAC is designed using a 47GHz SiGe technology and achieves a maximum 5GHz output frequency with 10GHz clock.**

Index Terms — DDS, nonlinear DAC, SiGe, high-speed IC.
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I. INTRODUCTION

In conventional digital frequency synthesizer (DDS), it's not easy to achieve output frequency bigger than 2GHz because of the time and area consumed by ROM look up table. At present, ROM-less DDS gains popularity because it uses a nonlinear DAC to replace the ROM lookup table and the linear DAC and thus can generate much higher output frequency [1]-[2]. However the nonlinear DAC in ROM-less DDS presented so far can hardly run at GHz speed and it consumes much power and area. This paper presents the design of a nonlinear cosine-weighted current mode DAC in a novel structure composed of DAC cells with different output currents. The current mode logic (CML) switches controlled by thermometer codes are used to switch each DAC cells at high speed. The DAC is designed in a 47GHz SiGe technology and can generate 5GHz sine wave and only consumes about 1W power, which is much smaller than that of a prior art cosine-weighted DAC implemented in InP [3].

II. NONLINEAR DAC DESIGN CONSIDERATIONS

The function of a nonlinear DAC in DDS is to convert the linear phase information W at the output of the accumulator directly into analog sine waveform as shown in Fig.1.

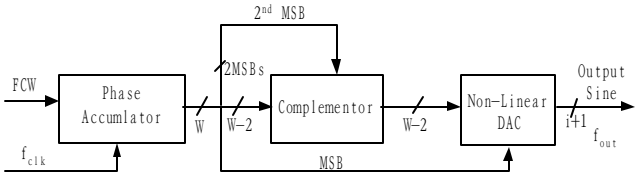

Fig. 1. High-speed DDS with a nonlinear DAC.

The first two MSBs of the phase accumulator output W are used to decode the quadrant of the sine function so that the nonlinear DAC only needs to generate sine wave from 0 phase to $\pi/2$ phase. Conventional static performances such as offset error, gain error, INL, DNL are not directly applicable to the nonlinear DAC. We consider the DAC power consumption and the following dynamic performances to determine the nonlinear DAC architecture:

1. Spurious free dynamic range (SFDR): the difference in decibels between the rms power of the fundamental and the largest spurious signal within a specified frequency band.

2. SINAD: the difference in decibels between the rms power of the fundamental and the noise and

distortion that falls within the Nyquist frequency.

Based on the SFDR requirement, we can determine the nonlinear DAC number of input phase bits W and DAC number of output bits. Fig.2 plots the decibel difference between the largest spurious (the worst case spur) and the fundamental signal versus the number of phase bits W and the number of DAC output bits in a MATLAB simulation. It's shown that the worst-case spur decreases as the number of DAC bits and/or the number of phase bit W increase.

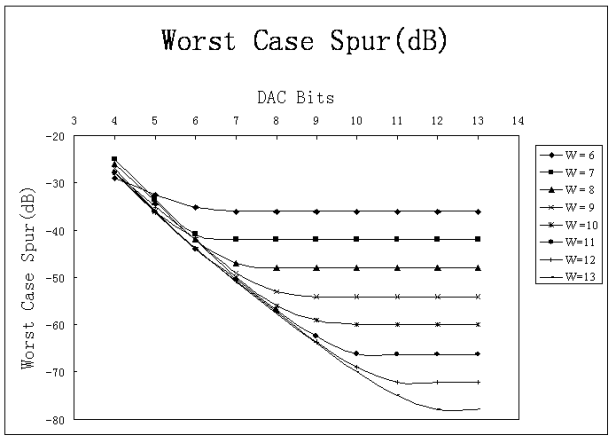

Fig.2. The worst-case spur in dBc versus the number of phase bits W and number of DAC output bits.

On the other hand, the total output current doubles when DAC bit increases by one bit and the number of DAC cells also doubles when phase bit W increases by one bit. Thus, the DAC bit and the phase bit W should be chosen as small as possible to minimize the area and power consumption. Moreover, the DAC output using an open collector resistor may encounter headroom problem if the total output current is too large. For low power application, we first choose a reasonable number of DAC output bits based on the required SFDR. Then, we choose the number of phase bits slightly larger than that of the DAC output bits such that the overall quantization noise is dominated by the number of DAC bits. For example, if the SNFR is required to be below -45dB, then according to Fig.2, the DAC bit is at least 8. This result is obtained under the assumption that that the phase bit W is equal or greater than the DAC bit. Having known the output DAC bit, the value of phase bit W can be obtained by the SINAD requirement in simulation. By adding a sigma-delta modulator in DDS, the quantization noise can be pushed away from the Nyquist band and thus increase the SINAD. So the phase bit W can be reduced using sigma-delta modulation, which further reduces the decoder size and thus increases the circuit speed.

III. NONLINEAR DAC ALGORITHM

Assume the nonlinear DAC output has i+1 bit resolution and its input phase word has W bits. The phase bit W can be divided into 3 parts: the first two MSBs, the middle a bits and the least b bits ($W\text{-}2=a+b$). Each DAC cell output (O_k) can be written as [4]:

$$O_{k=}\begin{cases}\text{int}\left[(2^i-1)\sin\dfrac{\pi(0.5)}{2(2^{a+b}-1)}\right], & for \quad k=0 \\ \text{int}\left[(2^i-1)\sin\dfrac{\pi(k+0.5)}{2(2^{a+b}-1)}-\sum_{n=0}^{k-1}o_n\right], & for \quad 1\le k\le 2^{a+b}-1\end{cases} \tag{1}$$

In equation (1), the first quadrant of sine wave is divided into 2^{a+b} phase steps and k is the different phase step from 0 to $\pi/2$. The DAC output at step k is the sum of the outputs of the DAC cell from 0 to k. The architecture to realize the nonlinear DAC composed of current cells is shown in Fig. 3.

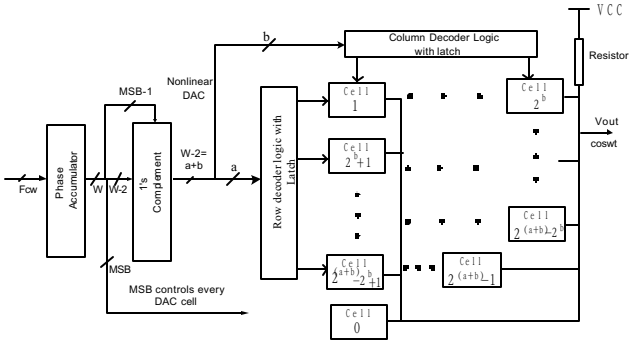

Fig .3. Architecture of the nonlinear cosine-weighted DAC in DDS.

The phase bit W from the phase accumulator is fed into a 1's complementor. The complementor output bits

(W-2 in length) are separated into MSBs (a bits in length) and LSBs (b bits in length) and passed to the row and column control blocks using thermometer-decoding scheme. These blocks translate the binary input into thermometer code and pass the values to the control logic in each DAC cells for the selection of the current–cell matrix. The sine wave output is obtained by summing the output currents from all the selected current cells. The thermometer decoding reduces dynamic errors by ensuring that the minimum number of cells switches simultaneously. The number of current sources that are turned on should be equal to the value of the thermometer input code. Let the W=6 and a=b=2, the thermometer decoder logic function is shown in Table 1.

Table 1 Thermometer-code representation of 2-bit binary values.

Phase	Binary (a or b)		Thermometer decoder output		
step(k)	a1(b1)	a2(b2)	R1(C1)	R2(C2)	R3(C3)
0	0	0	0	0	0
1	0	1	1	0	0
2	1	0	1	1	0
3	1	1	1	1	1

Note that a value of 0.5 introduces a 1/2 LSB amplitude offset in equation (1) such that XOR gates can be used as 1's complementor. During the negative region (π to 2π), the sine wave amplitude is generated by the complementation of the amplitude values in positive region (0 to π). If there is no 1/2 LSB offset, the amplitude in the last phase step of positive region and the amplitude in the first phase step of negative region would be both zero. This would destroy the symmetry of the output sine wave form. Therefore, the 1/2 LSB is introduced to offset the sine output from value 0 when K equals 0. Yet, this offset conflicts with thermometer decoding. Thus, in this design the first DAC cell 0 is placed out of the thermometer decoder cell matrix and is separately controlled by the MSB. When MSB is low (positive region of sine wave), it turns on and vise versa. The proposed DAC architecture can reduce the glitches in thermometer decoder and meanwhile keep the amplitude symmetry of the output sinusoidal wave. The rest DAC cells from 1 to 2^{a+b}-1 are placed in the DAC cells matrix as shown in Fig.4. For the nonlinear DAC with W=6 and a=b=2, the output currents of DAC cells from 0 to 15 are given as follows:

O_k= 6 13 13 13
12 12 10 10
9 8 7 5
4 3 1 0

The first DAC cell O_0=6 is moved out of the cell matrix and is separately controlled by MSB. Because the last DAC cell O_{15} =0, this DAC cell is neglected in the DAC cell matrix.

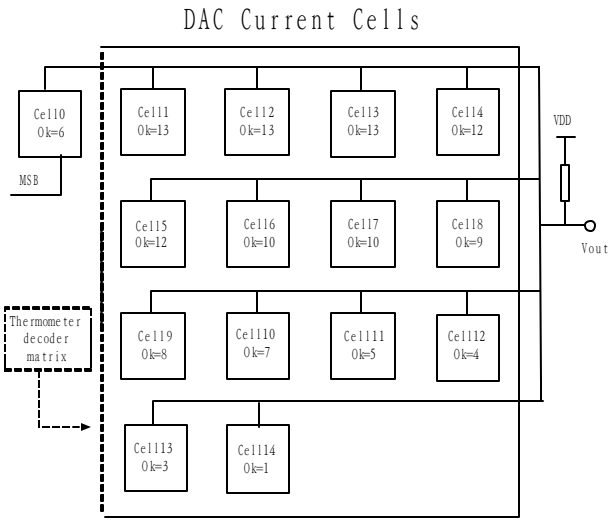

Fig. 4. DAC cell matrix with W=6(a=b=2).

IV. DAC CURRENT CELL DESIGNS

The DAC cell with different current source O_k is shown in Fig.5, where *n* represents the number of duplicated minimum current tails that form the desired current value O_k. The CML circuits are used to implement the current switches and the differential transistors both operate in the forward-active region with 400uA bias current. Although higher bias current can speed up the circuit slightly, it's not preferable because

the total power consumption increases and the output pull-up resistor value decreases in order to keep the same full-scale output voltage. A differential input voltage of 400mV is used to switch the current cells.

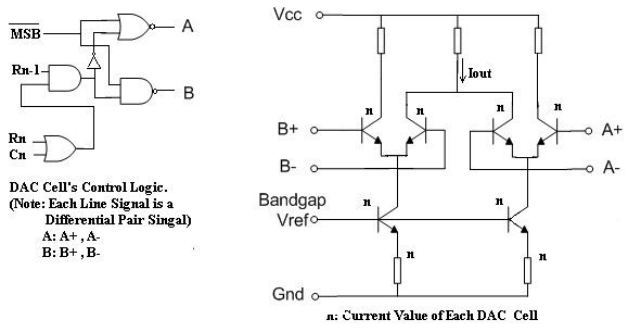

Fig. 5. DAC current cell circuitry.

Moreover, during a sampling period, the current is held constant. The two pairs of current switches A and B are used for producing the positive and negative regions of the sine wave outputs, respectively. For the positive region, the signal MSB is low, and the current switch pair A in all the DAC cells are turned on. The thermometer-code decoders will turn on the pair B according to cell control logic. For the negative region, the signal MSB is high and all the current switch pair B are turned off. The thermometer code decoder will turn on each cell's switch pair A according to the logic control circuit shown in Fig4.

V. SIMULATION RESULTS

We have designed the proposed nonlinear DAC in a 47GHz SiGe technology. Simulations were run with 6-bit phase input W (a=b=2) and 8-bit DAC output under f_{clk}=10GHz. There are total $2^{(a+b)}$=16 phase steps in one quadrant and the output frequency is set as 10GHz/(16*4)=125.25MHz. The 125.25MHz output waveform is shown in Fig.6. Fig.7 gives the simulated DAC output waveform with the maximum output frequency of 5GHz with clock frequency of 10GHz. Using the minimum size transistor with 1um emitter length, the total nonlinear DAC power consumption is estimated as 0.57 W, including the DAC cells and decoders.

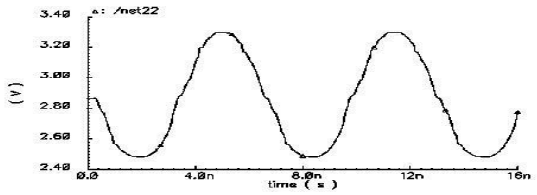

Fig. 5. Simulated DAC output waveform at 125.25MHz with clock at 10GHz

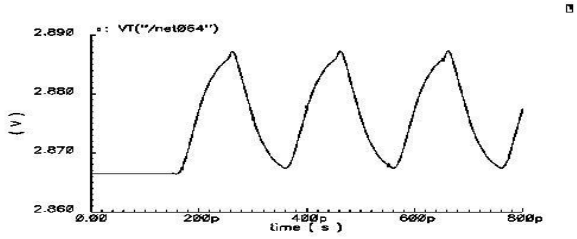

Fig.6 Simulated DAC output waveform at 5GHz with clock at 10GHz after the deglitch filter.

VI. CONCLUSIONS

This paper presented a cosine-weighted nonlinear DAC used for high-speed DDS applications. The DAC is designed in a 47GHz SiGe technology with maximum clock frequency of 10GHz. A novel DAC current cell architecture with thermometer decoding scheme is presented for high-speed and low power frequency synthesis and modulation applications.

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