A Tutorial on the Emerging Nanotechnology Devices

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Abstract

This paper provides an overview of the research on nanometer scale electronic switching devices. Such devices are likely to be used for building ultra-density integrated electronic computers of the future. We first describe the problems faced by the downscaling of FET devices and then discuss the emerging alternatives: 1) Carbon Nanotube transistors 2) Quantum effect and single-electron devices and 3) Molecular electronic devices. We discuss the basic operating principle of each type of device. Here mathematical details have been suppressed in favor of simpler understanding. The present state of the art for each new device is given, outlining the open problems for research. Finally, a possible time-line for their large-scale implementation is given.

1 Introduction

In the past 40 years, the metal-oxide semiconductor field effect transistor (MOSFET) has become the basic building block for almost all computing devices. The steady growth of their popularity is due to the steady shrinking of the feature size which at present has reached 0.1 micron. However, the laws of *quantum mechanics* and limitations of fabrication techniques may soon prevent the further decrease of feature size. Hence, researchers are investigating several alternatives to the transistor for ultra-dense circuitry. These new devices whose dimensions are on the order of tens of nanometers are called *nano-devices* and their science is termed *nano-technology.*

Unlike today's MOSFETs, which operate via the movement of masses of electrons in bulk matter, the new devices take advantage of the quantum mechanical phenomena that emerge at the nanometer scale geometries, where the discrete nature of electrons cannot be ignored. How will such devices look like? What will be their operating principles? These are the questions that we discuss in this paper. Some known answers are presented while others may be forthcoming through research.

This tutorial builds upon several earlier, more specialized papers and we combine them into one single manuscript [1, 2, 10, 23, 28, 29, 31, 32, 34, 45–49]. Goldhaber *et al.* [23] provided a comprehensive survey on the subject a few years ago. Recent research, however, has brought new devices like the carbon nanotubes and the quantum cells into focus, making that survey incomplete. In a recent special issue of the *IETE Technical Review* [1], Ahmad and other authors survey the work in progress in India. There is, however, a need for a tutorial incorporating the latest research developments to initiate a new researcher.

The devices are classified into three broad categories based on the operating principles and fabrication techniques:

- Carbon nanotube transistors
- Solid state quantum effect devices
- Molecular electronic devices

Devices in the first class are similar to the conventional MOSFET but are different in dimensions and in the material (carbon nanotube) they are made of. The second and third classes both use quantum effects but are fabricated differently. The solid state devices use fabrication techniques similar to those employed for MOSFETs. Even though these devices use quantum mechanical phenomena they take advantage of the years of experience in the MOSFET fabrication technology.

Molecular electronics is a new approach that requires new raw materials and a new operating principle. The incentive for such radical change is that molecules naturally occur in nano-scale dimensions. Unlike nano-structures built from bulk solids,

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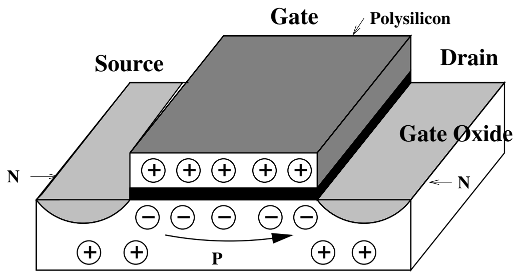

Figure 1: An n-type metal oxide Semiconductor field effect transistor (nMOSFET).

molecules can be made identically, cheaply and easily. Two significant challenges are to devise molecular structures that act as switches and to assemble those switches into precise structures needed for reliable computation.

In this paper we first give an overview of the problems faced by further shrinking of the current MOS technology. Then, we discuss the working principles of each new class, the devices in each class and the problems facing them. We finally summarize by giving time prediction on when these devices may become a reality for mass produced integrated circuits.

2 Nano-scale MOSFETs

In a digital circuit, a transistor is a switch, that controls the flow of current through its channel depending on the state of the gate terminal of the device. The condition that turns the device ON or OFF determines the type of the device. If voltage at the gate is used to control the current through the channel the device is called a *Field Effect Transistor (FET)* and if a current at the gate is used as the control then it is called a *Bipolar Junction Transistor (BJT)* [52]. A *Metal Oxide Semiconductor FET (MOSFET)* is a variant of the FET and is the predominantly used transistor in today's circuits. In this section we will examine the working principle of the device to study the problems of miniaturizing the MOSFET below 0.1 micron.

2.1 Structure and operation of a MOSFET

The MOSFET is a three terminal device with *source*, *drain* and *gate* terminals [52]. The structure of a MOSFET is shown in Figure 1. It is built on a crystalline substrate of doped silicon. Pure silicon is a poor conductor so dopant impurities, such as boron or arsenic, are introduced into silicon to create an excess of mobile positive or negative charges. Negatively doped (n-type) silicon contains excess electrons and positively doped (p-type) silicon contains electron vacancies known as *holes* which act as positive charge carriers.

As shown in Figure 1, an n-type MOSFET contains a lightly doped p-type channel between two heavily doped n-type source and drain regions. A metal electrode separated from the channel by an insulating oxide barrier serves as the gate terminal. The voltage at the gate alters the electric field through the channel of the MOSFET and hence the flow of current through the device. When the voltage on the gate is low, the channel contains few negative charge carriers and very little current flows. However, if the gate is maintained at high voltage, more carriers are attracted to the region below the gate and hence the channel freely conducts resulting in larger current through the device. Thus, the MOSFET acts as a two-state device, switching between on (high channel conductivity) and off (low channel conductivity) states based on the voltage of the gate terminal.

Integrated circuit technology has progressed over the past three decades based on the simple principle of *scaling*. The MOSFETs can be made smaller by just shrinking all the dimensions of the circuit including wire lengths and widths and transistor sizes. The parameter that determines the size of the circuit relative to the previous generation circuits is the *feature size*. It is the minimum conductor (wire) width that must be fabricated on the chip. All lengths are multiples of this smallest measure. In order to fit more transistors on a chip of a given area designers would like to decrease the feature size. The feature size has been decreasing continuously over the decades and has now reached 0.1μm. This has made possible dense chips like the Intel Pentium. However, further scaling down could cause problems as discussed in the next section.

2.2 Problems with nano-scale MOSFETs

Despite major challenges, the industry and many research groups want to further decrease the feature size and extend the MOSFET technology. The MOSFET-based CMOS technology[1] has been the

[1] CMOS (complementary metal-oxide semiconductor) is a technology in which both n-type and p-type MOSFETS are used together to implement logic functions.

mainstay of the industry for several decades and shifting to a new technology involves a major investment. There have been working transistors fabricated with a feature size of $25nm$, but large-scale circuit design presents problems that are yet to be solved [4,37,45].

2.2.1 High electric fields

The power supply voltage cannot be decreased in proportion to the channel length (see next subsection) and hence the scaling down increases the electric field strength across the gate oxide. For 0.1μm channel length devices, the oxide field has reached a maximum of 5 MV/cm, while the field in silicon has exceeded 1 MV/cm [45]. These values will further increase as the channel size reduces into the nanometer dimensions. The high fields produce higher leakage currents that degrade the device performance. In worst cases the field causes avalanche breakdown of the barrier and the electrons are conducted freely, producing current surges and damage to the device.

2.2.2 Power supply and threshold voltage

As the MOSFET channel is scaled down one would like to proportionately reduce the supply voltage to keep the active power and electric field within reasonable limits. However, the threshold voltage cannot be scaled down much. This is because the quiescent state power, i.e., the power consumed by the device in the steady state should be controlled. The major power consumed in this state is due to leakage current through the device and to reduce that, the threshold voltage is kept high. But the large threshold voltage results in much finer demarcations between on and off states and there will be a higher probability that the device would enter an undetermined state, which is neither on nor off. Besides the noise margin, inductive effects also make voltage scaling a critical problem.

2.2.3 Heat dissipation

Transistors expend their energy in the form of heat in the resistive parts. This heat, if not dissipated properly, can create *hot spots* on the circuit. These hot spots cause the material to overheat, resulting in deteriorated performance and malfunction, or even destruction, of the device.

2.2.4 Interconnect delays

The decrease in wire width increases the resistance and hence increases the delay. Shrinking would increase the interconnect delays enormously in comparison to the gate delays. The purpose of scaling is not only to increase the density of the chip but also to increase its speed. The devices may not be much faster due to large interconnect delays.

2.2.5 Vanishing bulk properties

The doping of the substrate is done by using an optical filter during the fabrication procedure. As the feature size decreases the finer doping regions are tougher to demarcate and hence the bulk may be nonuniformly doped at such small scales. This can fail to create transistors at the right places and hence the circuit would malfunction.

2.2.6 Shrinkage of gate oxide layer

For a 0.1μm CMOS devices operating at 1.5 V, an oxide thickness if 30Å is needed [45]. This corresponds to roughly ten layers of silicon atoms. With such a thin oxide layer quantum mechanical tunneling takes place and hence there is leakage through the gate. This decreases the feasibility of reducing the oxide thickness further.

The above mentioned obstacles are due to inefficient doping methods and the onset of quantum effects. The industry is trying to circumvent these obstacles and make devices that would account for the quantum effects. An effort in this direction is the *silicon on insulator* (SOI) device where the substrate is an insulator that is partially depleted [14]. Another approach is to use silicon germanium (SiGe) instead of the conventional silicon to make MOSFETs. Further explanation of these devices is beyond the scope of this paper [15,21]. The problem is not in the basic concept of the transistor but is caused by the use of silicon as the material. Hence some research groups have used tiny tubes of carbon for making switching devices that are smaller and faster than the silicon MOSFET. This is the focus of the next section.

3 Carbon nanotube field effect transistors (CNFET)

A carbon nanotube device is similar to a MOSFET in that a gate is used to control the flow of current through the device by varying the field through a channel. The innovation here is the mechanism of transport of electrons from the source to drain. Instead of having a channel whose field can be controlled by a gate electrode, these devices have a tiny tubular structure known as *carbon nanotube.*

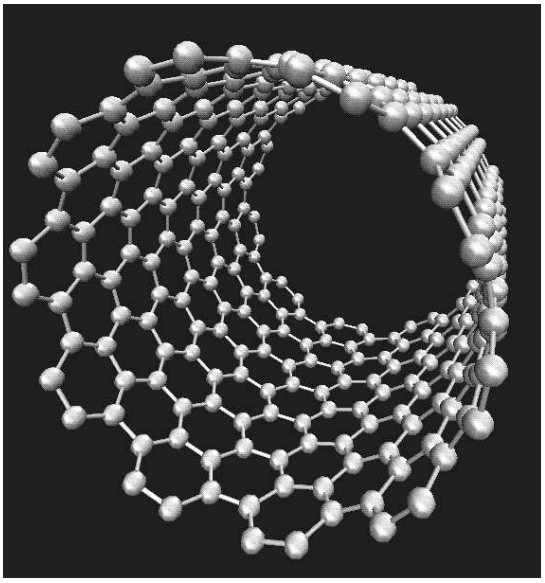

Figure 2: A single walled carbon nanotube.

This tube can be made conducting or semiconducting based on whether it is straight or twisted [1,16,17,28]. These devices are much smaller and more compact than silicon MOSFETs. This section explains the basic physics of a carbon nanotube and its role in the working of a CNFET.

3.1 Basic physics of the carbon nanotube

A carbon nanotube is a cylindrical rolled up sheet of graphene, which is a single layer of graphite atoms arranged in a hexagonal pattern like a chicken wire mesh [28]. Its structure is shown in Figure 2. Because of the hexagonal structure the graphene molecules belong to a class known as *fullerenes*, which are close-caged molecules containing only hexagonal and pentagonal inter-atomic bonding networks. Their hexagonal structure gives them great tensile strength and elastic properties. The tubes are tough and when bent or squeezed, spring back to their original shape. They also transfer heat very efficiently and hence are useful in circuits as they can be cooled faster. Their electrical conduction properties are also unique. They can be made to perform as a metal or a semiconductor depending on the way they are rolled.

We define a few basic terms that will be useful in understanding the carbon nanotubes. Consider the unrolled nanotube shown in Figure 3. The two unit cell vectors $\vec{a_1}$ and $\vec{a_2}$ are as defined in the figure. A *chiral vector* is defined as the vector normal to the

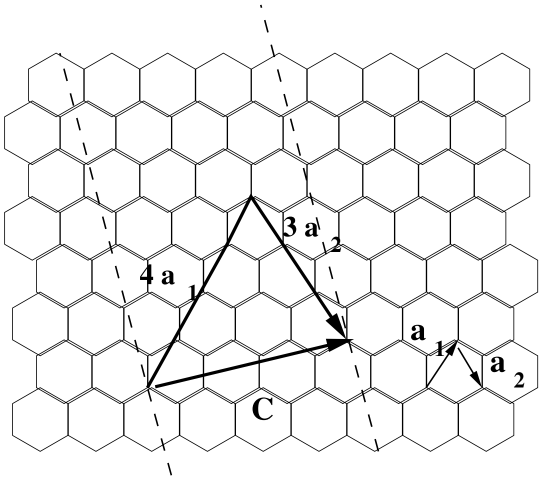

Figure 3: Chirality of a (4,3) carbon nanotube.

circumference vector in the direction in which it is being rolled. Hence the chiral vector is the horizontal vector from one open end of the tube to the other after it is rolled [16]. The chiral vector can be described in terms of the unit vectors as shown in the Figure 3.

$$\vec{C} = n\vec{a_1} + m\vec{a_2} \tag{1}$$

where n and m are integers. The nanotube is described by these numbers as (n, m). For example the tube shown in Figure 3 would be a $(4, 3)$ tube if it is rolled along the chiral vector shown. To distinguish between the metal and semiconductor tubes, a simple thumb rule has been established:

- If $n-m$ is divisible by 3 then the tube is metallic.
- If $n - m$ is not divisible by 3 then the tube is a semiconductor.

The chirality also gives us a basis for dividing the tubes into three different classes. Consider the tubes shown in Figure 4. A carbon nanotube described by (n, m) can be classified as:

- *Zig-zag* if either $n = 0$ or $m = 0$
- *Armchair* if $n = m$
- *Chiral* if $n \neq m$

By combining with the condition for the metallic properties we see that the armchair type is always metallic whereas the other two types can be either metallic or semiconducting based on their chiral condition.

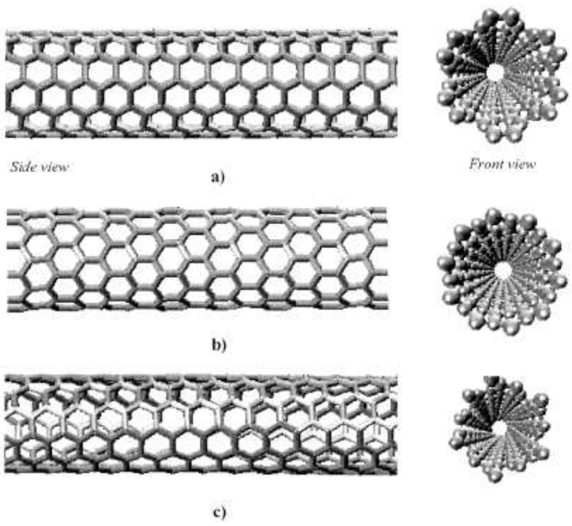

Figure 4: Three major types of tubes, (a) Zig-zag, (b) Armchair, and (c) Chiral.

The tubes can be made into single walled nanotubes (SWNT) or multi walled nanotubes (MWNT) [16]. The MWNTs are SWNTs wrapped one over the other. Both types of tubes can be used to make CNFETs, as we describe in the next section.

3.2 Basics of CNFETs

Externally, a CNFET is similar to a MOSFET. Both have three terminals, source, drain and gate. A carbon nanotube between the source and drain forms the channel [28]. The gate controls the field across the nanotube, thereby controlling the current flowing from the source to the drain. The channel of a conventional MOSFET is substituted by the nanotube in a CNFET.

The first generation CNFETs contained gold electrodes upon which the tube was laid to provide the channel. The gate was located on either side or underneath the tube, separated by an insulator. A problem with this design was that the tube was exposed to the air and hence due to a property (see next paragraph) of the tube it could operate only as a *p-type* transistor.The gate oxide also had to be thick in order to provide the insulation, which in turn increased the size of the device.

The CNTs are naturally occurring *p-type* devices

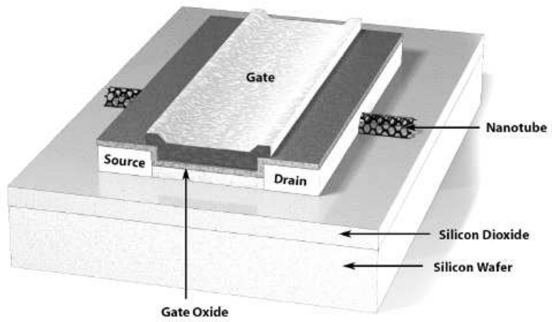

Figure 5: Structure of a second generation CNFET.

when they are exposed to air. This is because the oxygen in the air causes the Fermi level at the contacts to shift closer to the valence band. The result is that the holes see a smaller barrier than the electrons, and thus are able to tunnel through the device faster than the electrons. Since a conductor of holes is a p-type device, the undoped CNFET exposed to air gives a *p-type* CNFET.

The second generation CNFETs were a major improvement. The CNFET looks as shown in Figure 5. The gate electrode is placed on top of the tube to isolate it from the atmospheric air. This decreased the overall capacitance of the circuit as well.

In order to design conventional CMOS circuits we need an *n-type* device along with the *p-type*. This can be done in two ways, *annealing* and *doping*.

Annealing is the process of heating the tube to a temperature of 450^oC in nitrogen environment for a few seconds. This process drives out the oxygen absorbed by the tube and hence shifts the Fermi level up to the conduction band and the barrier seen by the electrons is reduced. Hence the electrons are more freely conducted than the holes by the tube, which behaves as an *n-type* device.

Another technique to convert a *p-type* tube to *n-type* is *doping*. In this technique the tube is doped with an electron donor such as potassium. The extra electrons reduce the barrier strength and once the tube is doped heavily enough, the electrons tunnel through the barrier and the device acts as *n-type*.

Although we have succeeded in converting the *p-type* tubes to *n-type*, exposure to air will revert the tubes back to their original *p-type* behavior. Hence the tubes need to be covered once they are converted to *n-type*. This is another reason why the second generation CNFETs are more successful, as the gate provides a natural cover to the tube.

A reader interested in the details of the electronics of carbon nanotubes may refer to Ahamad [1], Kanwal [28] or similar references.

3.3 Fabrication

CNFETs were envisioned and created in laboratories over 10 years ago, but the real hurdle was the lack of a mass production technology that would enable integrated circuits to be made. The main problem was that the tubes cannot be placed at exact locations automatically and there was no way to know whether a tube placed at some specific location is going to be metallic or semiconducting. This proved a major hurdle until the Avouris group at IBM came up with a method called *constructive destruction* [7]. They use MWNTs with metallic and semiconducting tubes rolled one over the other. Once the MWNTs are placed in the right locations the unwanted tubes are peeled off. If a tube needs to be made metallic then the metallic tube is left and the semiconducting tube is destroyed through chemical depositions. If a semiconducting tube is required at a location, then the metallic tube in the MWNT is destroyed. In this fashion the type and location of tubes in a circuit no longer remains a problem.

3.4 Summary: CNFET

The CNFETs are devices that work on a similar principle as the MOSFET except the channel is made of a carbon nanotube. Carbon nanotubes are structures that can be made metallic or semiconducting based on the way in which they are rolled. The semiconducting tubes are used in the transistors. Both p and n type devices have been fabricated and IBM claims to have found a way to mass-produce them [7]. This makes them worthy contenders to replace the MOSFET. However, several problems remain:

- Further scaling is a problem.
- Multi level interconnects, such as different metal layers are still unavailable with carbon nanotubes.
- New fabrication technology is not at the production level.

Despite these problems, the industry is eagerly looking forward to production of experimental carbon nanotube chips.

4 Solid state quantum devices

Why circumvent the quantum effects when they are an eventuality? Can we use them to our advantage in building new devices? These are the questions that motivated some pioneers of nanotechnology.

A number of nanometer scale bulk effect semiconductor devices have been proposed as replacements for the current MOSFET [23]. These take advantage of the quantum effects. An essential common feature of all these devices is a small island in which electrons are confined. This island is analogous to the channel of a MOSFET. The extent of confinement of the electrons in the island defines two sub-categories of such solid-state devices:

- *Single electron transistor*
- *Quantum dots*

The composition, shape and size of the island gives the device its distinctive properties. Controlling these factors permits the designer of the device to employ quantum effects in different ways to control the passage of electrons on to and off the island. In this section we first explain the common principles and terminology of these devices. Then we explain the different classes of devices.

4.1 Islands, potential wells and quantum effects

The place of confinement of electrons is called the *island*. The smallest dimension of the island ranges from 5 to 100 nm. The island is embedded between two narrow walls of some material, or an insulating defect zone in the substrate. These boundaries create potential energy barriers, which impede the movement of electrons through the island. This is shown in Figure 6.

Electrons can cross the potential barrier if they attain higher energy than the potential energy of walls of the barrier [20]. Within the island the electrons form a puddle that is much smaller than the dimensions of the island. The puddle is surrounded by a depletion region because electrons in the puddle are repelled from surface charges that collect on the boundaries of the island. Thus, the physical features that form the island need to be fabricated much larger than the required island dimensions. This factor might prevent further miniaturization of quantum effect devices.

There are two useful properties exhibited by electrons confined to these islands [20]. The first is the

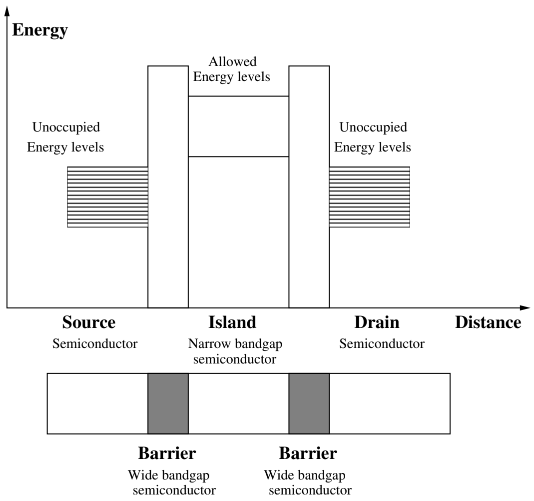

Figure 6: Potential structure of a quantum well showing the allowed and unoccupied energy levels on either side of the well.

quantization of energy levels. In a MOSFET an electron can occupy any energy level in the channel as energy levels are continuous. But in the quantum case, the energy is quantized in the well regions. In Figure 6, this is the region where the energy of the electron is less than the energy of the walls, which in our case forms the island. This means that the electron can occupy only certain specific states that satisfy Schroedinger's wave equation. If a well has large number of these energy levels, then the electron has higher probability of staying in one of them, but if a well has very low energy levels then there is low probability of the electron staying in the region. For nanoscale devices, if an electron needs to cross the barrier onto the island, it needs to be charged enough to occupy one of these energy levels. Hence it is preferable to have larger number of energy levels on either side of the island. Thus, quantization needs to be considered while designing these devices.

The second effect is *tunneling*. If the potential barriers are thin enough the electrons can cross them without any external energy source and this effect is called tunneling. However, for an electron to tunnel through a barrier, there must be a vacant state with the same energy on the other side of the barrier [20]. Nanoscale devices use this fact for the conduction of current by designing thinner barriers and forcing tunneling as we shall later see.

These two effects, energy quantization and tunneling strongly influence the working of nano-electronic devices. When a bias voltage is applied across the island, it induces mobile electrons in the conduction band of the source region to attempt to move through the potential well in the island region to get to the region of lower potential in the drain region. The only way for electrons to pass through the device is to tunnel on to and off the island through the two tunnel barriers that define the island and separate it from the source and drain. This is illustrated in Figure 6.

Figure 6 shows the allowed energy levels in various regions of the device. The bulk semiconductor has closely packed energy levels but the island region has very sparsely spaced ones. This confines the number of electrons allowed onto the island. Tunneling can occur from the source to the drain only if there is an unoccupied energy level with the same energy in the drain region. Since the drain region has several unoccupied energy levels this would not prove to be a problem for these devices. So the real barrier is the first barrier from the source to the island [23]. Once an electron is able to travel from the source to the island it is usually free to complete its passage through the device by tunneling once again from the well to the drain.

Before we study various devices we need to learn a few basic principles of tunneling. Consider the barrier graph shown in Figure 7. It shows the potential barrier distribution of a two tunnel barrier device. It is crucial to the operation of the tunneling devices that the energy of the quantum states in the potential well on the island can be adjusted relative to the bands in the source and the drain. Since the source contains electrons, we know that the source conduction band is occupied (metals have occupied conduction bands). The allowed energy levels in the well are as shown.

As we increase the bias voltage across the island, the energy of all the states in the well is lowered relative to the energies of the electrons in the source. When the bias voltage is sufficient to lower the energy of an unoccupied one-electron quantum state inside the well to be within the range of energies for the source conduction band, the quantum well is said to be in *resonance* or "on" state and current can flow onto the island and out to the drain. If the energy is not sufficient the electrons are blocked and the device is said to be "off". This two state operation of the device determined by an applied bias characterizes the operation of a two terminal resonant tunneling device.

The quantum dot (QD) and the single-electron transistor (SET) are resonant tunneling devices. The point to note here is the decrease in potential of the energy levels in the well relative to those in the source. This can also be done by adding an extra gate termi-

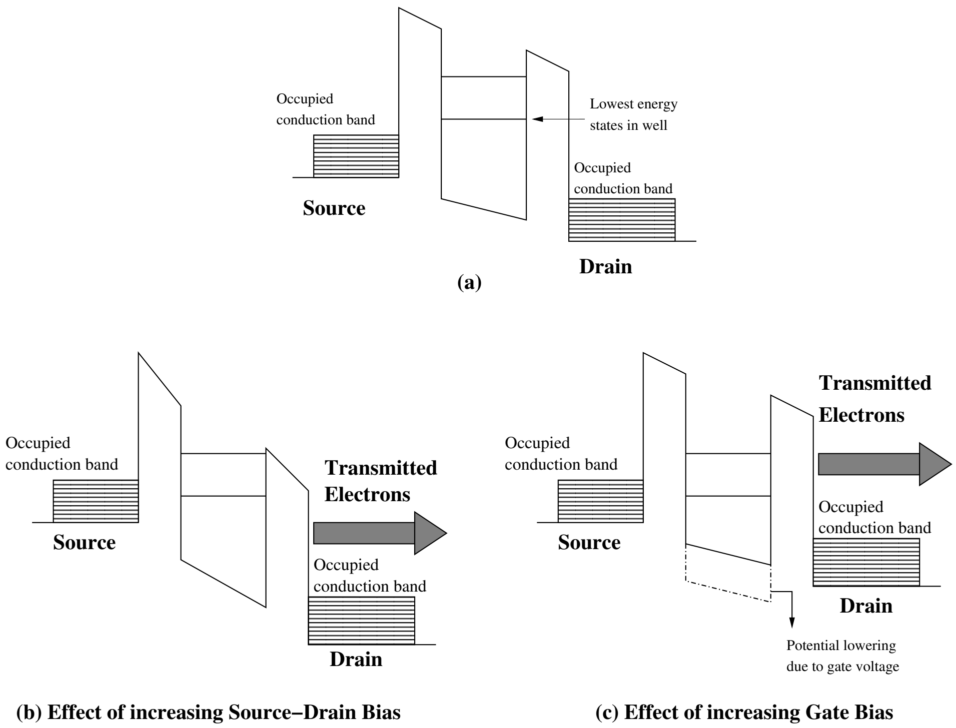

Figure 7: Potential structure of a quantum well showing the allowed and unoccupied energy levels with various bias conditions: (a) Small source-drain voltage – no conduction, (b) Large source-drain voltage – conduction, and (c) Small source-drain voltage, large gate voltage – conduction.

nal that lowers the potential as shown in Figure 7(c).

This gate is the third terminal that is added to the pair of tunnel junctions to form an SET. The SET is confined only to a single dimension barrier, but if the confinement of electrons is done in all three dimensions, then we have a quantum dot. As we see the two devices are different and yet quite similar in their operating principles.

These are the governing principles of both the quantum devices. The methods by which the well to confine the electron is created and the means by which the bias is applied is what distinguishes one device from another.

5 Single-electron transistor (SET)

This section describes the principles and physics behind the SET. We present typical I-V characteristics and the conductance graphs of the device.

5.1 Principle of the SET

The structure of an SET is shown in Figure 8. The details may be found in a book [48] and many recent references [2, 3, 9, 13, 22, 30, 35, 39, 49–51]. The device consists of two tunnel junctions characterized by a junction capacitance C, a tunneling resistance R. The two junctions are separated by an *island* which is coupled to a gate bias, while a source-drain bias is applied across the tunnel junctions as shown.

An SET can be visualized as having a double barrier potential. The double junction is a circuit consisting of two tunnel junctions in series, which form an *island* between them. The junctions are biased with a voltage source connected between the source and drain. For very small bias no current flows as the electrons do not have enough energy to overcome the barrier. We initially assume that no bias voltage is applied to the gate terminal. Increasing the source to drain bias voltage steadily, at some point it becomes possible for an electron to tunnel through the first junction. This electron enters the island thus increasing the energy level of the island from Ne to $(N+1)e$. This in turn forces an extra electron to exit from the island through the second barrier, thus re-

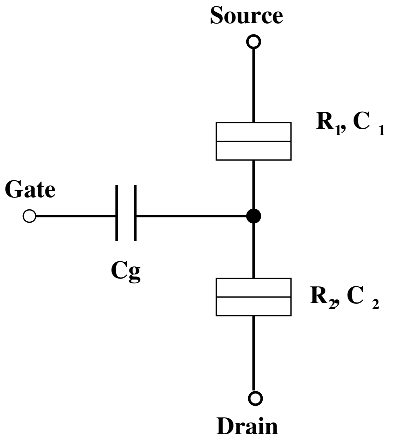

Figure 8: Schematic of an SET.

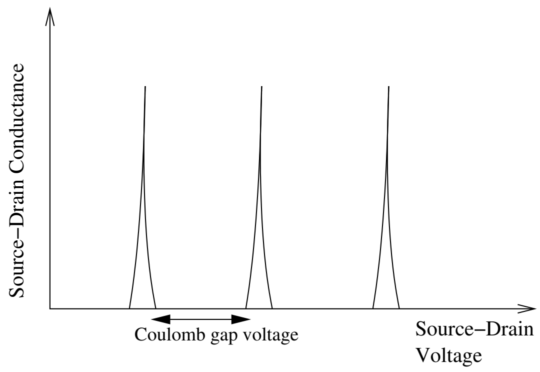

Figure 9: Plot of conductance of an SET as a function of source to drain voltage.

turning the island to its earlier energy state Ne. Since the source to drain bias voltage has not changed, another electron enters the island through the first junction resulting in a steady current through the double junction.

If we make the second tunnel junction barrier higher than the first barrier, then certain number of electrons will have to be accumulated on the island before any electron can tunnel through to the drain. This phenomenon of blocking an electron from immediately leaving the island is called *coulomb blockade*. The source to drain voltage increase necessary to overcome the coulomb blockade is called the *coulomb gap voltage*.

As we increase the drain-source voltage, due to the quantization of the electronic charge an increase in current occurs only at increments of the coulomb gap voltage as depicted by the conductance graph of Figure 9. Hence, the waveform looks like a staircase called the *coulomb staircase*.

Suppose, we keep the drain-source voltage below the coulomb gap voltage. If the gate voltage is increased that increases the initial energy of the system, while the energy of the island with one excess electron decreases gradually. At the gate voltage corresponding to the point of maximum slope on the coulomb staircase, both of these configurations equally qualify as the lowest energy states of the system. This lifts the coulomb blockade, allowing the electrons to tunnel into and out of the island. We find that the coulomb blockade is lifted when the gate capacitance is charged with exactly minus half an electron, which is not as surprising as it may seem. The island is surrounded by insulators, which means that the charge on it must be quantized in units of e, but the metallic gate is a supplier of plentiful of electrons. The charge on the gate capacitor merely represents a displacement of electrons relative to a background of positive ions. More about the mathematics of the SET is explained in the next subsection.

If we further increase the gate voltage so that the gate capacitor becomes charged with $-e$, the island again has only one stable configuration separated from the next lowest energy states by the coulomb energy. The coulomb blockade is set up again, but the island now contains an excess electron. The conductance of the SET therefore oscillates between minima for gate charges that are multiples of e and maxima for half integer multiples of e.

We have a device that switches between conducting and non-conducting stages by the addition of a single-electron at the gate terminal. Hence it can be used for building logic circuits similar to CMOS circuits.

5.2 I-V characteristics of SET

In the previous subsection we dealt with the operating principles of the SET without any mathematical analysis. Now we will deal with the actual physics of the SET and the equations that describe the complete operation of the device.

Consider the double junction system shown in Figure 10. The parameters shown are the characterizing values of both junctions shown in the circuit. Assume initially that $C_1 \ll C_2$ and $R_1 \ll R_2$ so that the tunneling rate through the first junction is far greater than that through the second. Set the external source to drain bias voltage V so that the charge flow from left to right is preferred, and increase the bias voltage above the coulomb gap voltage. The gov-

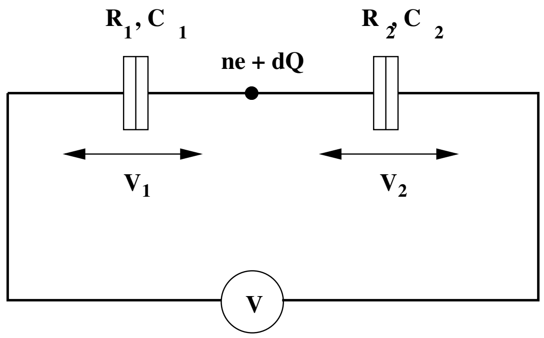

Figure 10: Circuit of an SET.

erning circuit equations are:

$$V_1 = \frac{C_2}{C_1 + C_2}.V - \frac{ne + \delta Q}{C_1 + C_2} \tag{2}$$

$$V_2 = \frac{C_1}{C_1 + C_2}.V + \frac{ne + \delta Q}{C_1 + C_2} \tag{3}$$

where $ne + \delta Q$ is the charge on the central electrode. This is the result of n electrons on the electrode due to tunneling events, and an initial charge δQ due to external voltages coupled to the electrode via the gate capacitance [48].

For given external voltage V, electrons will tunnel onto the central electrode until V_1 becomes smaller than $e/(C_1 + C_2)$, at which point the junction becomes coulomb blockaded. Because of the tunneling rate assumptions above, the blockade condition is always reached before we need to consider charge tunneling out through C_2. Since tunneling rate through C_2 limits and governs the current through the device and since V_2 is pinned by the blockaded condition of junction 1, current through the device remains constant for a range of external V.

In order to raise the number of electrons on the central electrode by 1, V_1 must be raised by

$$\Delta V_1 = \frac{e}{C_1 + C_2} = \frac{C_2}{C_1 + C_2}.\Delta V \Rightarrow \quad \Delta V = \frac{e}{C_2} \tag{4}$$

which in turn allows a current increase,

$$\Delta I = \frac{\Delta V}{R_2} = \frac{e}{R_2(C_1 + C_2)} \tag{5}$$

Thus, the I-V curve of such a device shows distinct steps of width ΔV and height ΔI. As the junction parameters are brought nearer, $C_1 \approx C_2$ and $R_1 \approx R_2$, the tunneling rates through the two junctions become comparable, blockade conditions are less likely to build up and the I-V curve tends to be linear as shown in Figure 11.

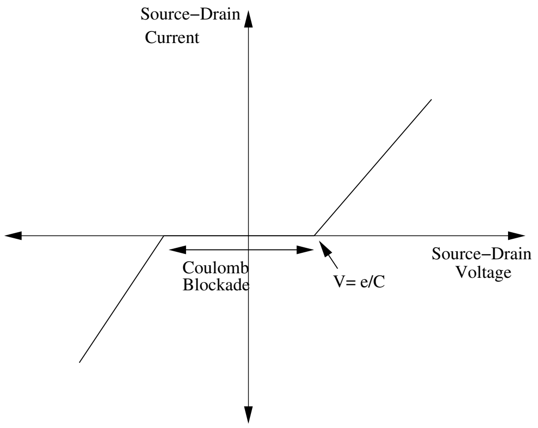

Figure 11: I-V characteristic of the SET in Figure 10.

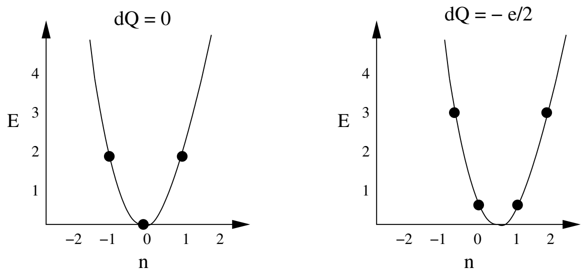

Figure 12: Energy diagram illustrating the effect of fractional charge on the central electrode of a double junction. Charge can only change by an integral amount, into the states marked by solid dots.

5.3 Conductance of SET

Consider the schematic of the SET shown in Figure 10. Let the external bias applied to the source-drain be zero ($V \approx 0$). The capacitive energy of the central electrode is

$$E = \frac{(ne + \delta Q)^2}{2(C_1 + C_2)} \tag{6}$$

where n is the net number of electronic charges that have tunneled through the first junction and δQ is a fractional charge due to the gate electrode. If we plot the electrostatic energy of the central electrode as a function of n we expect the curve to be a parabola. The curves for two limiting values of δQ are shown in Figure 12. Note that due to the discrete nature of the tunneling only those energies with the solid dots are allowable [48].

The *tunneling activation energy* is defined as the energy required to add another electron to the island.

It is given by

$$\Delta E = E(n+1) - E(n) \tag{7}$$

When $\delta Q = 0$, we have

$$E = \frac{e^2}{2(C_1 + C_2)} \tag{8}$$

which is the coulomb blockade energy. This is the normal condition that we have seen already. Now for $\delta Q = -e/2$, the activation energy is reduced to 0 and both energy states $E(n+1)$ and $E(n)$ are degenerate. Hence the charge transfer can occur freely and the conductance has a peak at this value of charge.

We must note that this particular point of increased conductance is precisely the point where the I-V curve has a step on the coulomb staircase. The steps are spaced with the coulomb gap voltage at the gate terminal.

5.4 Summary: Single-electron transistor

In this section, we explained the basic principle and operation of the SET. The SET is ailed by a problem of background charge which will be discussed later. The operation of SET circuits can be upset by the presence of one single stray charge and hence they are not likely to be used for large CMOS type applications but are quite useful for designing memories.

6 Quantum dots (QDs)

In the previous section we have seen the operation of the SET and also noted that the background charge is a problem. At such small dimensions even a single-electron matters and hence the flow of electrons cannot be guaranteed to be an exact number that we desire. Essentially, for logic operation we do not need the actual flow of electrons. We need an efficient encoding system that transfers the state of a dot through an array of devices. This is where the quantum dots come into the picture. Quantum dots are devices with tunnel junctions in all three dimensions of the island. Thus, we have an *electron box*, which the excess electron is confined to. This excess electron determines the state of the system and when these dots are arranged in cells it is possible to design logic circuits that can function efficiently. This will be the focus of this section. First we will describe the structure and operating principles of a quantum dot. Then we describe a quantum cell array and its two state operation. We then explain the procedure by which circuits and interconnects can be designed using the quantum cell arrays.

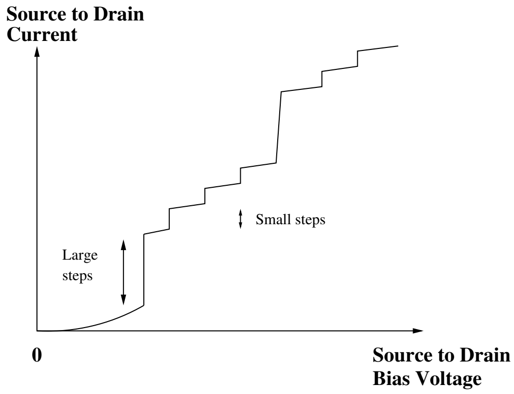

Figure 13: I-V characteristics of a quantum dot.

6.1 Physics of a quantum dot

The quantum dot has become a buzzword in the industry and is often used to denote many nanoscale devices. But the widely accepted definition of the quantum dot is an area or region, which an electron can be confined to. The quantum dot receives its name from the fact that it is confined by barriers in all three dimensions [29,38].

In contrast, the SET is a two dimensional device where the electron movement is in one direction from the source to drain along a single dimension. But in quantum dot the energy spacing is different in all three dimensions x, y and z. Hence the dot is a potential well in all three dimensions. Since the direction does not matter, we do not care for the flow of charge anymore. The presence of an excess electron means a change in state of the device.

The dot-like island may be made of either metal or semiconductor. It can consist of small deposited regions, self organized droplets or nano-crystallites grown or deposited on a film. Using the physical ideas outlined above, we observe that making an island short in all three dimensions leads to widely spaced energy levels for an electron on the island [19,24,34,38,47].

6.2 I-V characteristic of a quantum dot

The I-V characteristic of a quantum dot is shown in Figure 13. As we increase the bias voltage across the dot two interesting things happen. First, the current rises to a level where the electrons flow one at

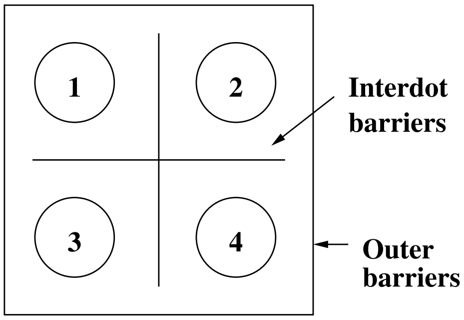

Figure 14: A quantum cell array (QCA).

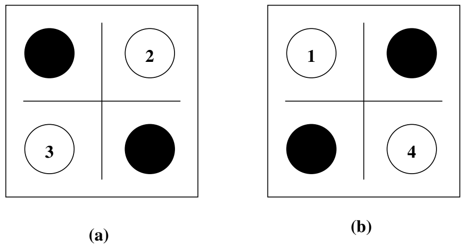

Figure 15: (a) A QCA depicting logic state 1, and (b) QCA depicting logic state 0.

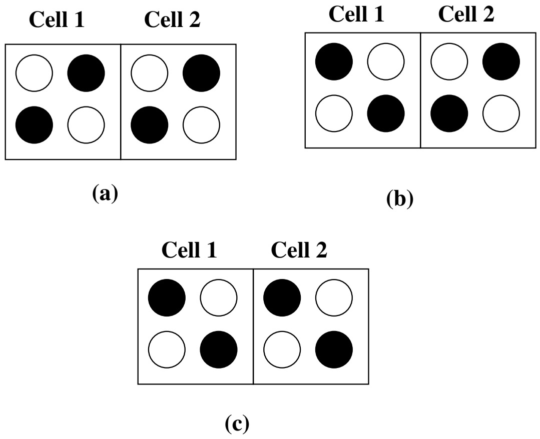

Figure 16: Transmission of state through cells: (a) shows a stable configuration of cell array, (b) Cell 1 is changed in value by changing the inter-barrier potentials; this is an unstable configuration, and (c) The Cell 1 forces Cell 2 to be of the same value; this is a stable configuration.

a time. Then, as we increase the bias voltage there is a series of steps in which the current rises. These steps correspond to the different energy levels for the same electron. But as the bias voltage is increased above a certain level where more than one electron can be accommodated in the dot, then the current is increased by another steep rise and the intermediate steps occur again. Essentially the smaller steps are for the different energy levels available in the dot and the larger steps are for the number of electrons that can flow at the same time. This shows that it is possible to put as many or as few electrons in the dot by varying the squeezing voltage. That is why the quantum dots are sometimes referred to as *artificial atoms.* The dot acts as a nucleus that attracts electrons and the valency of the atom (or dot), is controlled by the external gate voltage. Hence we have our own way of creating an atom with the desired number of electrons trapped in it or revolving around it. This leads to the creation of new devices that are not like the transistor but are useful in computing. These are the quantum cell arrays that are discussed in the next section.

6.3 Quantum cell array (QCA)

A quantum dot by itself has very little computing value. It has similar problems as the SET. The current flow is too weak to create any significant logic function change. The device proposed for computing is the *quantum cell array* (QCA) or *quantum cellular automata.* This is a set of four dots as shown in Figure 14. Sometimes a fifth dot is added in the center but we will ignore it as it does not change the functional value of the array.

The array consists of four tunnel barriers between the dots and eight barriers on the outside of the barrier. The cells are designed such that the barriers on the outer side of the cell are much higher than the inner barriers. Suppose, there are two excess electrons confined in the whole array. Since electrons repel each other, they tend to stay as far from each other as possible. Hence they occupy the diagonal dots as this gives them the largest separation.

By altering the inter-barrier potentials the electrons can be shifted from their positions as shown in Figure 15(a) to those in Figure 15(b). Even in the state shown in Figure 15(b) the electrons are separated by their maximum distance and hence are in equilibrium. Thus, we have two states in which the cell can be polarized. These two states can be classified as the two binary values. Let us suppose that the state in Figure 15(a) is 1 and that in Figure 15(b) is 0. Now let us see what happens when two cells are placed close to one another.

Consider the setup shown in Figure 16. Let the

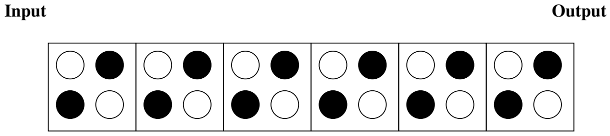

Figure 17: A quantum wire as a row of cells.

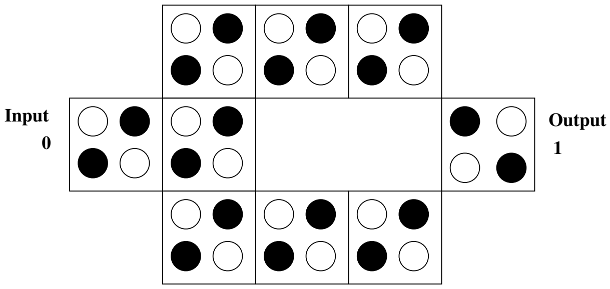

Figure 18: An inverter gate in QCA logic.

initial polarization of a cells be as shown. Now if they are brought together and the configuration in cell 1 is changed by manipulating the inter-barrier potentials, then due to repulsive forces of electrons, the electrons in cell 2 are also polarized in the same fashion. We have a device that has two states of operation and can transmit its state to a neighboring device. It thus sounds like a transistor! This generates a whole range of possibilities for designing logic circuits. Some of these are described in the following subsections.

6.4 Quantum wires

A quantum wire can be assembled as a series of quantum cells as shown in Fiure 17. By changing the polarization on a cell at one end of the wire the whole wire can be made to transmit the information to the other end. Though unconventional, this is an effective way to send information over a physical distance.

6.5 Quantum computing

To compute a logic function using the cells we construct a majority gate. Consider the configuration shown in Figure 18. This is an inverter. If the input is polarized in a certain fashion, then the output is always polarized in the opposite fashion.

A majority gate can be constructed as shown in Figure 19. The cells are aligned in a fashion to min-

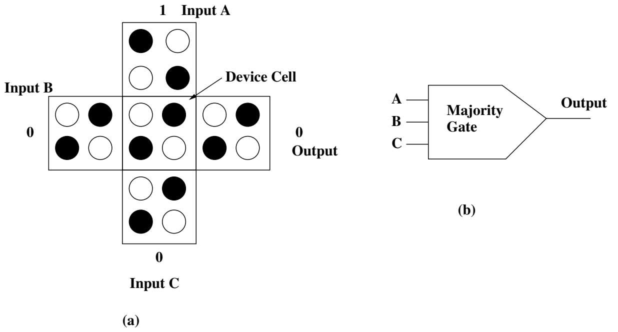

Figure 19: A majority gate in quantum cellular automata logic: (a) The cell array showing that the majority of the electron interactions determine the value of the cell, and (b) Symbol of the gate.

imize repulsive forces from the adjoining cells and hence the output will align to the state, which most of the inputs are aligned to. This allows a design of logic functions using neural networks. Further explanation of such implementations is beyond the scope of this paper.

6.6 Summary: Quantum dots

The quantum dots are zero dimensional devices that are either empty or contain an electron. They require a new way in which we should perceive computing by discarding the idea of the transistor switch. An array of these dots, called quantum cells, is used for computational purposes. We try to communicate information not by transmitting current but just by transmitting the state of the device. This eliminates many problems faced by the switching devices and hence the quantum dots appear to have a bright future. These devices can be used to construct logic gates and quantum wires and effectively functioning logic circuits. However they have problems that are explained in the next section.

7 Obstacles for solid-state quantum devices

Although the solid-state quantum devices show great promise, just like any nascent technology, they pose problems to be solved before real industry applications [23]. We outline some of these problems:

- *Background charge:* Random charge accumulates in semiconductor regions close to the quantum devices. This can make the device inoperable as it would alter or damage the intended charge distribution. Improved materials such as silicon on insulator (SOI) could alleviate this problem, but this has not been tried yet.

- *Extreme sensitivity of tunneling current to width of potential barriers:* This is a common problem to all the quantum effect devices. It requires such high precision lithography that may be difficult to guarantee in the near term.

- *Extreme sensitivity of making islands and tunneling barriers uniformly:* The large scale production of these tunneling devices need highly uniform distributions of barriers across the chip. This cannot be guaranteed unless the cutting and etching techniques reach very high resolution.

- *Cryogenic operation:* This is a problem for certain single-electron devices. The operation of quantum devices has been demonstrated at very low working temperatures. To get them to work at the room temperature would mean imparting the electrons lot more energy that could jeopardize the tunnel current. Some advances have been made toward room temperature operation of these devices, but mass production could still be a problem.

- *Valley Current:* When the quantum devices are off resonance, the tunneling current might not be completely cut off (see Sec. 4.1). There will be a small current through the device and with further miniaturization it may become difficult to distinguish between the on and off states. This is analogous to the leakage current in the present-day MOSFET technology.

- *Sensitivity to input voltage fluctuations:* The quantum devices can be very sensitive to input voltage fluctuations unlike the MOSFETs. Even a little blip could throw the device accidentally off resonance.

Despite these obstacles, the solid-state quantum devices hold promise and researchers are relentless in making integrated circuits with these devices.

8 Molecular electronics

One major obstacle for the solid state quantum devices is that the lithography is not precise enough to guarantee uniform devices all over the chip. The main principle in this technology is to make identical molecules combine into structures that make computing devices.

Individual molecules naturally occur in nanometer scale structures. These molecules are *exactly identical* and can be organically combined to form structures that function as electrical switches and even as solid-state transistors. This has driven investigators to design, model, fabricate and test new devices. Molecular electronics is a speculative research idea but considerable advances have been made since its inception [5, 12, 18, 25, 40, 43].

In this section we describe various types of molecular devices and some common ways of fabrication. We give a brief description of the molecular wires and insight into the working of the various devices. The understanding of molecular electronics is heavily intertwined with organic chemistry, but we do not elaborate on the actual reactions and formulae that govern these devices. The idea of this section is to acquaint the reader to the vast potential of molecular computing.

8.1 Molecular switching devices

There are four broad classifications of molecular switching devices [23]:

- *Quantum effect devices*, which operate by controlling the electric field across the device.

- *Electromechanical molecular devices*, which employ electrical or mechanical forces to change the configuration, or to move a switching molecule or group of them, to turn a current on or off.

- *Photoactive molecular switching devices*, which use light to change the shape, orientation and configuration of the device, thereby changing the current through the device.

- *Electrochemical switching devices*, which use electrochemical reactions to change the shape, orientation and configuration and hence alter the current through the device.

In this paper we focus on the first two categories of devices as they are most closely related to the solid state devices that we have described in the previous sections. The other two devices have greater limitations. The photoactive devices are fast and small but they cannot be switched individually as light cannot be confined to such small regions. Electrochemical devices have to be immersed in a solvent to operate which would prove messy for building integrated chips.

Before we describe the different devices of molecular electronics, we give a short description of the assembly techniques that made molecular electronics possible.

8.2 Fabrication and assembly of molecular structures

The whole field of molecular electronics is based on the concept that we can find chemical processes that can make the molecules bond in the exact same way as we intend to. There are many ways that have been tried but the two major ones are *mechanosysnthesis* and *chemosynthesis*.

Mechanosynthesis is the fabrication of nanostructures, molecule by molecule, using *nanoprobes* (high precision controlling instruments) such as *scanning tunneling electron microscope* (STM) and the *atomic force microscope* (AFM) [11,42]. These sensitive tools have made manipulation at the molecular levels possible. By manipulating individual molecules using nanoprobes, structures or devices that act as switches and transistors can be built.

Chemosynthesis is another way of making these nanostructues. It is the chemical *self assembly* of molecules into nanostructures [6, 36, 41, 53]. It includes certain biochemical methods that organically synthesize molecular electronic devices from individual molecules. This technique shows promise but research is still needed.

8.3 Molecular wires

The molecules can be made to assemble, but they must communicate with each other. *Molecular wires* are essentially a series of molecules that connect two devices and can conduct electrons between them. Many alternatives have been tried to build a simple chain of molecules, but the major problem was that molecules that conduct well do not have good bonding properties, and those that bond well and form chains do not conduct well. If the wires are just one molecule thick then they would exhibit very high resistance which would be a problem [27].

The most promising discovery in this field is a *buckyball*. This is a C_{60} molecule that has certain useful properties [26]. It can conduct electrons and can also attach itself to other C_{60} molecules as they have good co-ordination. Rows of these buckyballs can be made to combine with each other and form what is known as a *bucky tube*. It is similar to a carbon nanotube where the carbon atoms are chemically bonded to create fullerenes (see Section 3). These are virtually flawless hexagonal arrays of conducting atoms and are the best example of molecular wires.

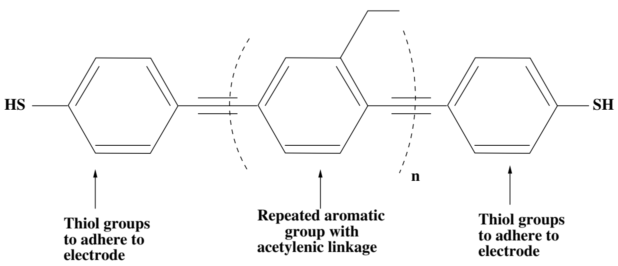

Figure 20: An atomic wire with thiol groups serving as clips to electrodes.

Other alternatives such as *thiol* functional groups at either end of the molecular wire have been tried [8]. These structures adhere to the metallic electrodes and form a bonded connection acting like an *alligator clip*. A sample molecular wire with these linkages is shown in Figure 20. The wire is composed of benzene like rings with acetylene linkages.

To manipulate and fabricate tiny molecular switching devices it is easier to embed them in wire like structures. Hence, the field of molecular wires is intimately linked to the future of molecular electronics.

8.4 Quantum effect molecular electronic devices

These devices in principle work with the same ideas of resonant tunneling and single-electron switching effects as the solid state quantum devices we discussed earlier. The idea is to create potential wells within molecules such that electrons can be confined to them. These potential wells must be controlled by electrical field to make them switch between on and off states. There have been significant discoveries showing this to be possible and demonstrating such effects as coulomb blockade with devices made from molecular electronics.

Alternatively, a quantum well can be embedded in a molecular wire like the one shown in Figure 20, by inserting pairs of barrier groups that break the sequence of conjugated orbitals. This would produce a potential distribution as shown in Figure 21.

When the molecule is subjected to a voltage bias the barrier can be lowered and resonant tunneling can be made to take place. The problem with such devices is that the charging energy on either side of the well can be larger than the energy level spacing

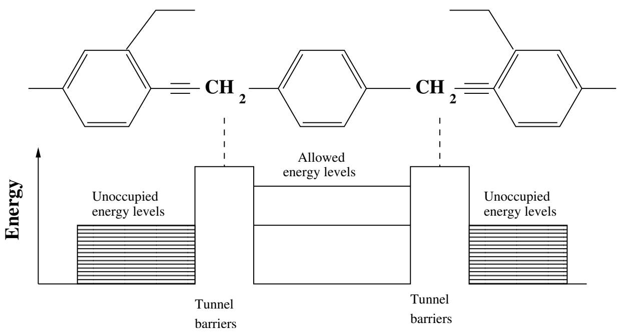

Figure 21: A potential barrier distribution created from inserted groups in an atomic wire.

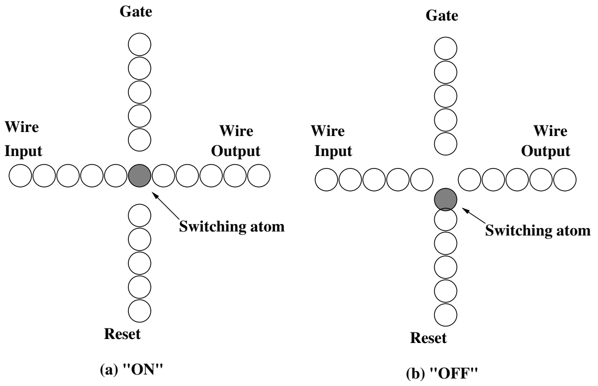

Figure 22: An atomic relay showing the action of the gate: (a) The switching atom is in ON phase as gate attracts it, and (b) The switching atom is in OFF state as the gate repels it; the reset terminal is to reset the switching atom to ON state.

within the well. This would mean that the source and the drain may not have matching energy levels and hence the device may tunnel in but may not tunnel out. Still, these provide flexible and uniform ways of building potential barriers which might be the future ways in which the quantum devices can be built.

8.5 Electromechanical molecular electronic devices

Electromechanical molecular devices use force to deform or manipulate the molecules and make them function in a certain fashion. The input can be mechanical rather than electrical, but the interesting thing is that they can stop the flow of current through two sections of the wire based on a condition. There are different types of such devices based on what inputs they take. We illustrate some of them below.

8.5.1 Single molecule amplifier

This is another application of the *buckyball* that was described in the previous section. The C_{60} molecule can be held between an scanning tunneling microscope (STM) tip and substrate and when the tip is pressed upon, the buckyball is deformed and its conductivity decreases [11]. Thus, the buckyball can be made to go on and off resonance by using a mechanical force. In real circuits this mechanical force would be provided by a piezoelectric gate or an actuator that can be controlled by an electric field [33].

8.5.2 Atom relay

The concept of an atom relay is shown in Figure 22. There is a mobile atom between two wires. Based on a controlling gate condition it switches the wires in connected *on* or unconnected *off* state. The atom shuttles between the conducting and non-conducting phases, thus producing the effect of a switch. A third wire analogous to the gate terminal can also be added and charged positive or negative. If the gate atom repels the switching atom then the switching atom moves to the off state whereas when it attracts the atom, the wire switches back to on state. However, the circuits that employ atomic relays are limited to two dimensions. Without crossing wires only a few logic functions can be implemented and this is a major drawback of this type of devices.

8.5.3 Refined molecular relays

These devices are based on similar atomic movements as in an atomic relay but they might use the rotation of a molecule for the purpose of movement. The switching atom in the atomic relay can be made more reliable by attaching it to a rotating group or a *rotamer* [44]. This rotamer is a part of a larger molecule. When the rotamer is in the wire, the switch is on and conducts current, but when the gate is charged the rotamer is rotated out of the wire and the switch is turned off. There is a third molecule that prevents the rotamer from rotating freely due to thermal fluctuations. This allows the relay to be designed in three dimensions permitting the circuit to be made more dense. However, there are issues such as the strength of bonds between the rotamer and how stray bonds might alter the configuration.

8.6 Summary: Molecular electronics

The inefficient etching techniques from bulk materials led to the idea of making the switching devices from exactly identical molecules, which naturally occur in nanoscale elements. These molecules can be made to self assemble or can be placed by manual intervention through nanoprobes. Molecular wires can be made by joining conducting atoms called buckyballs. Certain molecular devices use quantum effects to conduct electrons. Potential barriers can be made within a row of atoms and they even exhibit tunneling. Other devices using mechanical forces to alter the current through a wire have been made. Relays using switching atoms are also possible. Overall, the field of molecular electronics is promising but very nascent in nature. For it to unseat the solid state devices may need a series of discoveries in various fields.

9 Conclusion

In this paper we have described the problems ailing the current CMOS industry that prevent further scaling down of the feature size. There are many alternatives. The carbon nanotube transistors or CNFETs are devices that retain most of the concepts from MOSFETs but use carbon nanotubes as channels. At nanoscale, the quantum effects cannot be ignored. Some devices utilize these effects for their operation. We described the common principles of these devices and explained the SET and QD. We gave an insight into their principles of working and the obstacles they face. Molecular electronics is a revolution in the raw materials used for nanoscale devices. The molecules are chemically combined to produce the circuits from the bottom up instead of cutting them out of bulk matter as done in solid state. We described various types of devices and presented an overview of the fabrication and conduction techniques. The aim of this paper is to provide a window to the the nanotechnology research and its possible applications.

Nanocomputers will only be possible after breakthroughs on many fronts. It remains uncertain which discipline would provide the earliest breakthrough. However, once they arrive, they will change the face of electronic computing and our technological infrastructure.

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