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Editorial

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I am pleased to announce the *2022 JETTA-TTTC Best Paper Award*. The award selection committee consisted of Xiaoqing Wen, Chair (Kyushu Institute of Technology, Japan), Jennifer Dworak (Southern Methodist University, USA), Jiun-Lang Huang (National Taiwan University, Taiwan), and Erik Larsson (Lund University, Sweden). We congratulate the winning authors, Zhi-Wei Lai, Po-Hua Huang, and Kuen-Jong Lee. Their winning paper is, "Using both Stable and Unstable SRAM Bits for the Physical Unclonable Function," Journal of Electronic Testing: Theory and Applications, Volume 38, Number 5, pp. 511–525, October 2022. Please see the award and recipient details that follow this editorial.

Yervant Zorian, TTTC President, announced the *2022 JETTA-TTTC Best Paper Award* at a plenary session of the International Test Conference at Anaheim, CA, on October 12. 2023. In the absence of the authors, the award was received on their behalf by Professor Shi-Yu Huang of National Tsing Hua University, Taiwan.

This issue has nine articles. The topics discussed are printed circuit board testing (a survey), test generation, fault tolerance, single event upset (SEU), electromagnetic interference (EMI), hardware security, and software testing,

The issue begins with a survey of printed circuit board (PCB) testing. This is a sequel to a review of PCB defects by the same authors, that appeared last year (*JETTA*, volume 38, number 5, pages 481–491, October 2022). Since many defects are caused during manufacturing and are mechanical in nature, their detection uses image processing and machine intelligence. The authors are Gayathri Lakshmi, Udaya Sankar, and Siva Sankar from SRM University, AP, India.

Second paper describes an automatic test pattern generation (ATPG) tool adopted to the available MATLAB software. It uses evolutionary algorithms like genetic algorithm (GA) and particle swarm optimization (PSO) to derive compact tests for both combinational and sequential circuits. Contributors are P. Bhattacharya, R. Bhattacharya, and Deka, from Indian Institute of Technology (Indian School of Mines), Dhanbad, India.

Third paper explores an interesting idea in designing a digital image processing adder circuit. Fault-tolerance is implemented by triple modular redundancy (TMR) applied only to a selected subset of significant bits. Contributors are Iqbal from Deccan College of Engineering and Technology, Telangana, India, Daimi from Indian Institute of Technology Madras, Tamil Nadu, India, and Chari from GITAM University, Telangana, India.

The fourth paper has a theme of fault-tolerance like the previous paper, though in the context of single event upsets (SEU) occurring in the space applications. Since various reliability schemes are associated with varying performance costs, the scheme for each segment of the system is selected based on the tradeoff between SEU error suppression and performance. Authors are Zhao and Chen from Nanjing University of Aeronautics and Astronautics, China, and Lu from University of Essex Colchester, UK.

Fifth paper develops a machine learning methodology for identifying the sources of electromagnetic interference (EMI). Contributors of this work are Xiao from Lanzhou City University, Lanzhou, China, and Zhu, Zhuang and Yang from Southwest Jiaotong University, Chengdu, China.

Next two papers address hardware security issues.

The sixth paper gives an ingenious design for physical unclonable function (PUF) using CMOS current mirrors and the so-called winner takes all (WTA) neuron cells. Contributors of this work are Mitchell-Moreno and Flores-Verdad from National Institute for Astrophysics, Optics and Electronics (INAOE), Mexico.

The seventh paper develops a deep learning neural network for detecting hardware Trojan from side channel analysis. Authors are Chen, Wang, Huang and Hou from Guilin University of Electronic Technology, Guilin, China.

Finally, we have two papers on software testing, an area we recently included in *JETTA*.

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The eighth paper starts with the premise that not all software instructions have the same capability of producing an observable program error. Machine learning techniques can classify instructions based upon their error producing capability, while separating the class of non-error producing instructions. This classification then helps increase the efficiency of mutation testing. Authors of this work are Asghari and Koochari from Islamic Azad University, Tehran, Iran, and Arasteh from Istinye University, Istanbul, Turkey.

In the ninth paper, the authors prioritize the order of software tests to enhance the reliability of the tested product. They use a variety of machine intelligence algorithms for effective ordering of tests. Contributors of this work are Rajasingh from Anna University, Chennai, India, Kumar from SKR Engineering College, Poonamalle, Chennai, India, and Srinivasan from RMD Engineering College, Kavaraipettai, Tiruvallur District, Tamil Nadu, India.