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Editorial

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The eight articles of this issue focus on reliability against single event upset (SEU), fault diagnosis, hardware security, memory yield and reliability, analog and radio frequency circuit testing, and diagnosis of biochips.

The first paper addresses the problem of errors in approximate digital circuits caused by radiation and electromagnetic interference. The authors use approximate triple modular redundancy (ATMR) and evaluate the reliability of voting schemes by simulation, and by experiment with ion beam radiation. Contributors of this work are Balen, Gonzalez and Butzen from Federal University of Rio Grande do Sul, Porto Alegre, Brazil, Oliveira, da Rosa Jr and Soares from Federal University of Pelotas, Pelotas, Brazil, Schvittz from Federal University of Rio Grande, Rio Grande, Brazil, Added, Macchione, Aguiar and Medina from University of Sao Paulo, Brazil, and Guazzelli from Centro Universitario FEI, Sao Bernardo do Campo, Brazil. This paper extends the researches that authors presented at the 22nd Latin American Test Symposium (LATS) in 2021 and at the IEEE International Symposium on Circuits and Systems (ISCAS) in 2022.

In the second paper, the authors argue that some defects of mixed-signal circuits in advanced technologies may not be accurately represented by the known fault models. Using a decomposition algorithm, they extract features like mean, standard deviation, kurtosis, skewness, and entropy, which are supplied to a deep learning neural network to classify the faults. The authors are Ram from Anna University, University College of Engineering, Dindigul, India, and Cecil Prabhakar from Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai, India.

Next, there are three papers on hardware security, addressing the protection against side channel attacks and hardware Trojans.

The third paper begins by pointing to the role of side-channel analysis (SCA) such as that of power in stealing sensitive information like an encrypted key. Block cypher algorithms, SM4 being one of them, are used to mask the key to protect against SCA. This work discusses higher order masking in SM4. Authors are Shao, B. Wei, Ou, Y. Wei and Wu from Guilin University of Electronic Technology, Guilin, Guangxi, China.

The fourth paper uses XGBoost, a machine learning algorithm, to detect Trojan hardware in the logic level description of a synthesized circuit. Authors are Dhar, Giri and Roy from Indian Institute of Engineering Science and Technology, Shibpur, Howrah, India, and Das from Samsung Research Institute, Noida, India.

The fifth paper begins by showing that machine learning techniques using structural controllability and observability, derived from the SCOAP testability measure, may fail to detect certain types of Trojan hardware. One case where the difficulty arises is an always-on-Trojan. A new detection algorithm then uses a game theoretic approach, SHAP (shapley additive explanations), which helps explain the output of the machine learning model allowing detection of the Trojan. Authors are R. Sharma, G. K. Sharma, Pattanaik and Prashant from ABV-Indian Institute of Information Technology and Management, Gwalior, India.

The sixth paper observes that rapid advances in the technology and applications of NAND flash memories have led to the need for larger number of error correction bits. To efficiently manage the error correcting code (ECC) bits, this work proposes the design of an ECC cache, and demonstrates enhanced reliability and yield for NAND flash memories. The authors are Lu and Tsai from National Taiwan University of Science and Technology, Taipei, Taiwan.

The seventh paper addresses the problem of testing the C-band transmit-receive (TR) modules of a synthetic aperture radar (SAR) system used on an imaging satellite. The paper then describes an architecture and the development of an automatic test system (ATS). The operation and results illustrate high effectiveness derived by the application-specific design of the ATS. Contributors of this work are

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The eighth paper uses the recently proposed microelectrode-dot-array (MEDA) architecture for designing a digital microfluidic biochip (DMFB). Such devices are finding applications in healthcare. Realizing that a single failure in the MEDA dot-array may cause the microfluidic system to fail, this work develops a concurrent fault diagnosis and repair scheme. The research is reported by Zhang from Jiangxi University of Finance and Economics, Nanchang, JiangXi, China.