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BISCC: A Novel Approach to Built In State Consistency Checking For Quick Volume Validation of Mixed-Signal/RF Systems

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Abstract
The increasing integration of mixed-signal systems in System-on-Chips (SoCs) and System-on-Packages (SoPs) has made pre and post-silicon validation more challenging. This is due to the lack of automated design checking algorithms and the inability to control and observe internal circuit nodes in post-silicon. While digital scan chains can provide observability of internal digital circuit states, analog scan chains encounter issues such as signal integrity, bandwidth, and circuit loading. To address these challenges, a new approach based on built-in state consistency checking (BISCC) is proposed in this paper. The BISCC technique enables both pre and post-silicon validation of mixed-signal/RF systems without the need for manual checks. The approach is supported by a design-for-validation (DfV) methodology, which inserts a minimum amount of circuitry into mixed-signal systems to detect and diagnose design bugs. The core idea is to apply two spectrally diverse stimuli to the circuit under test (CUT) in a way that results in the same circuit state (observed voltage/current values at internal or external circuit nodes). By comparing the resulting state values, design bugs can be detected efficiently without manual checks. The proposed BISCC approach does not make assumptions about the nature of the detected bugs and is steered towards detecting the most likely design bugs. The effectiveness of the approach is demonstrated through test cases for both pre and post-silicon design bug detection and diagnosis.

Keywords Electrical validation · System testing · System verification · Analog circuits · State-dpace methods

1 Introduction

The integration of devices in integrated circuits has been made possible by aggressive scaling of technology. While this has allowed for the incorporation of newer features in a single die area, it has also posed significant challenges for testing and validating state-of-the-art SoCs due to the low controllability and observability of internal circuit nodes. The combination of aggressive time-to-market goals and diverse operating modes further complicates pre-silicon validation, which can be computationally intensive. Additionally, electrical aspects such as power and ground bounce, capacitive coupling-induced crosstalk, parasitics in active and passive components, and relevant design non-idealities are challenging to expose in pre-silicon simulation environments. Consequently, design bugs in analog and mixed-signal circuits often appear in the fabricated die, necessitating rigorous post-silicon validation and multiple silicon respins for design debugging.

2 Prior Work

There are three main categories of pre-silicon verification methodologies for analog/mixed signal systems. These are: (i) equivalence checking [15], (ii) model checking [8], and (iii) specification testing through SPICE simulation. However, the use of SPICE simulation for AMS verification is computationally challenging. Current state-of-the-art validation techniques utilizing equivalence and model checking have their drawbacks. Firstly, assertions for

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checking design accuracy need to be handcrafted, requiring input from experienced analog designers. Secondly, only simple properties and specifications of AMS circuits and systems can be handled. Fault isolation and diagnosis are also not addressed satisfactorily by these methods and require manual simulation. Moreover, these pre-silicon verification techniques are not easily adaptable to mixed-signal/RF post-silicon validation.

Scan chains are a popular method for providing state observability and controllability in digital design, aiding in post-silicon validation and circuit debugging. However, the analog scan standard IEEE 1149.1/1149.4 [9, 20] has limited application in testing analog/RF IP blocks in SoCs. An alternative current-based analog scan chain was proposed in [18, 19], and analog scan methods relying on voltage to frequency or voltage to delay conversion [22] are not suitable for testing AMS circuits at-speed. To address this, the authors in [23] proposes an analog DFT technique using supply voltage ramp-up. However, all scan-based test methods face difficulties in testing AMS circuits and systems at-speed, where design bugs are most likely to occur.

On the other hand, model-driven validation techniques have been proposed for analog/RF post-silicon validation in [2, 3], and model learning-based diagnosis in [4]. However, complex design bugs, especially electrical bugs arising from coupling and ground bounce, are challenging to simulate.

In terms of test stimulus generation, digital test generation-driven validation has been researched [14, 17], but there is limited work in the mixed-signal/RF domain. The authors in [10, 13], propose the use of diverse programs with the same functionality to detect design bugs in various hardware components (processor cores, uncore components and accelerators). A hardware design bug is flagged if there are any discrepancies in the outcomes of two program streams that are functionally equivalent, at designated checkpoints. This method does not assume anything about the nature of the bugs and can uncover a broad range of design bugs based on the diversity of the test programs used.

3 Proposed Approach

Validation can be broadly classified into two types a) Functional and b) Electrical. Functional validation is aimed at high level coverages (System/Firmware/Software level) while electrical validation is for ensuring circuit level operation at various PVT corners. As RF/Mixed signal/analog circuits are more susceptible to PVT variations, it calls for extensive electrical validation effort. Moreover RF/mixed signal/analog circuits are sensitive to minute manufacturing variation, so electrical validation requires volume level validation and manufacturing test to ensure correct operation and screen faulty parts respectively. Functional validation requires few parts to prove the functional operation. In this work, we have addressed the huge effort needed to perform the electrical validation and proposed BISCC to accelerate electrical validation of RF/mixed signal/analog circuits

A preliminary version of the proposed approach was published as a short paper in DATE 2017 [5] and in [1]. In this work we have explained the approach in detail with additional pre-silicon simulation results and post-silicon measurement data.

Our proposed approach involves using a reference model of an AMS system to create spectrally diverse test stimulus for the system or module being tested. This method is similar to the work done in reference [10], where program diversity is based on the instruction set architecture (ISA) of the processor being debugged (reference model). The diverse stimuli are designed to take the circuit under test from a known initial state to the same final state, which is measured by the voltage/current values at specific circuit nodes. The final states reached by the two different stimuli, applied in sequence, are acquired using track-and-hold circuitry (as shown in Fig. 1), and the comparison results are scanned out using digital scan chains. By checking for consistency between the final states reached by the diverse test stimuli, we can detect design bugs quickly and with high coverage (as shown in Fig. 1). Similar to reference [10], we do not make any assumptions about the nature of the design bugs detected, and models for hard design bugs are developed only after they are detected with considerable debugging and bug modeling efforts.

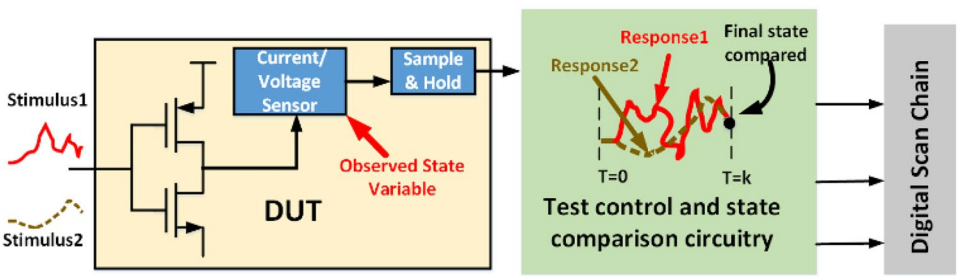


Fig. 1 State Consistency Checking Based Validation of Mixed-Signal/RF Systems

The main contributions of this work are:

1. *The BISCC approach proposed for design debug is a comprehensive methodology that can be utilized for pre and post-silicon validation of AMS/RF systems, and is applicable at various stages of the design process.*
2. *Unlike conventional approaches that rely on manually generated assertions in the AMS domain, which are error-prone, the BISCC design validation approach can automatically identify design bugs, without the need for such assertions. It can even identify bugs whose effects are unknown prior to circuit debugging.*
3. *The BISCC approach uses short test sequences that require very low-test application time, thereby generating a small volume of test data. In post-silicon validation, the data can be scanned out using existing digital scan chains in SoCs. The tests are generated using either existing digital processors on-chip or minimal amounts of compact digital stimulus generation logic, resulting in low hardware overhead.*
4. *The BISCC methodology requires minimal on-chip hardware for post-silicon debug, in contrast to other analog/RF DFT techniques* [9, 14, 18, 19] *that use full ADCs with attendant signal routing and fidelity issues. The minimal hardware consists of track-and-hold and voltage/current comparison circuitry. Additionally, the use of multiple voltage and current test points enables the localization of design bugs to specific design modules, thus facilitating system debug.*

Figure 2 shows how BISCC can be leveraged at different steps of chip design from architectural design to production sign off. In this work, we have restricted ourselves to time domain models and analysis. BISCC can be used to perform equivalence checking (sign-off) between behavioral models and corresponding netlist designs. Similarly, comparing results between architectural simulation (behavioral model) and post layout result, post layout sign off decisions can be facilitated. After silicon fabrication, BISCC can be used to debug and validate manufactured silicon against architectural specifications. RF/analog/Mixed-Signal electrical validation is specification based. For example, High speed IO interfaces (PCIe, USB, CXL) are electrically validated against Bit Error Rate (BER) and Margin (timing and voltage) specifications. Specification based test and validation either need expensive test equipment or/and it takes a long time using internal DFT. None of them is feasible for lab level volume validation (to cover process, voltage, temperature, dynamic range) and high-volume manufacturing testing (to screen parts before shipping to customer). BISCC based validation is well suited for both types of volume validation and test. While BISCC is designed without assertions and its implementation does not require circuit knowledge, a correlation study between the proposed BISCC DFT and ATE measurement values may be necessary for post-silicon validation and manufacturing testing. This study can help increase confidence in the reliability of the testing process and potentially eliminate the need for specification-based testing.

The rest of the paper is organized as follows: Sect. 4 describes the principles of analog state consistency checking and associated debugging. DFX infrastructure placement algorithms are discussed in Sect. 5. Rapid stimulus generation algorithms are explained in Sect. 5.1. Two example circuits are used to validate the proposed methodology in Sect. 6. Analog signal capture and comparison-based design-for-testability (DFT) circuit designs are explained in Sect. 7. Pre and Post Silicon experimental results are discussed in Sect. 8 and 9 respectively. BISCC accuracy is described in Sect. 8. Future work and conclusions are given in Sect. 9.1.

4 Debugging using Analog State Consistency Checking

A. State Transition Representation

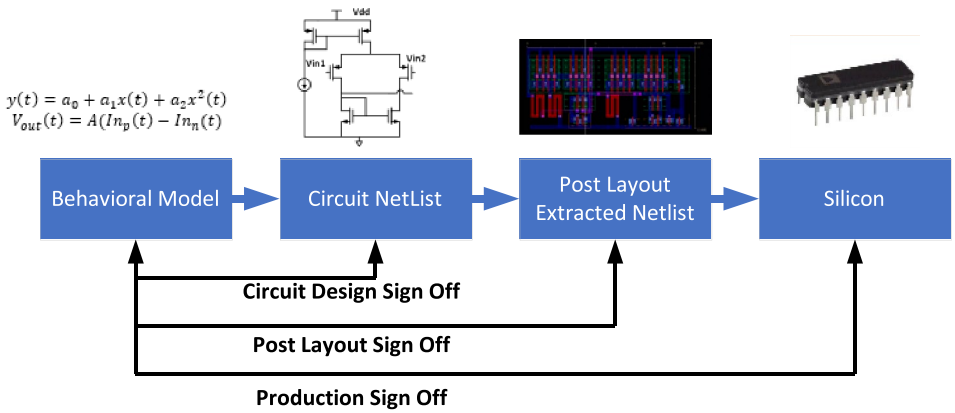


Fig. 2 BISCC Usage

Table 1 Formal Definitions of State Variable and State Consistency

	Definition
State Variable (SV)	*Any observed node voltage or branch current is a state variable.* $SV \in \mathbb{R}$ *and* $R_{i1} < SV_i < R_{i2}$ *Where* (R_{i1}, R_{i2}) *is the dynamic range of the observed current/voltage corresponding to state variable i.*
State Consistency	***Temporal Consistency:*** *Two state values* SV_i^1 *and* SV_i^2 *of state variable* SV_i *are consistent with each other if* $\left\|SV_i^1 - SV_i^2\right\| < \epsilon$ *where* ϵ *is comparator offset voltage* ***Spatial Consistency:*** *Two state values* SV_i^1 *and* SV_j^1 *of state variables* SV_i *and* SV_j *are consistent with each other if* $\left\|SV_i^1 - SV_j^1\right\| < \epsilon$ *where* ϵ *is comparator offset voltage*

Table 1. gives definitions of state variables and state consistency. Energy reservoirs such as capacitors and inductors in circuits cause circuit response to depend on prior capacitor voltages and inductor currents and hence, exhibit memory effects. Hence, RF/analog circuits can be modeled as state machines with future states dependent on the current circuit state and external circuit inputs. The number of possible states is infinite as analog currents/voltages can take any value within the dynamic range of signals at internal circuit nodes and outputs. Here, any branch current or node voltage can be thought of as a state variable of the system. If we imagine a finite resolution analog-to-digital converter associated with each state variable, then the state variable values assume discrete levels given by the assumed resolution of the analog-to-digital converter. The combined state of the circuits is the concatenation of the state variable values seen at all the observed node voltages and branch currents. Exciting the above state machine with an input stimulus, takes the state machine from one state to another through various intermediate states. We say that two models (implementations) of a given circuit or system are *behaviorally equivalent* if both models produce the same final circuit state in response to an arbitrary input starting from the same (arbitrary) initial circuit state.

The BISCC validation approach rests on the premise that two *different* input stimuli that take a model of the circuit from a prescribed starting state of the model to the *same* final model state must also take a behaviorally equivalent (different) model of the circuit from the same starting state to the same final state. Conversely, if the final states of the said models (implementations) under the two input stimuli are not the same, then state transitions behaviors of the two model are also not the same, proving that the two models are behaviorally inconsistent with each other. In practice, when comparing the final states of the two models, a calibrated threshold is used such as when comparing the response of a behavioral model to that obtained from a netlist.

B. State Consistency Checking Approach

Type I Test (Temporal State Consistency Checking) Our approach involves crafting a piecewise linear stimulus of duration T over a time grid of spacing δ and N grid points where $T = N\delta$ (as shown in Fig. 3). After applying stimulus

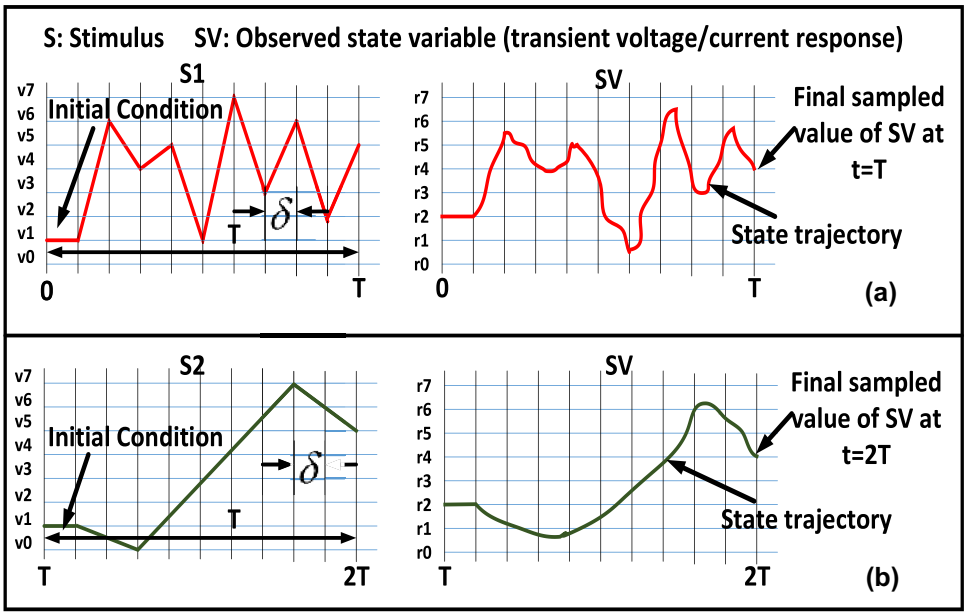


Fig. 3 Temporal State Consistency

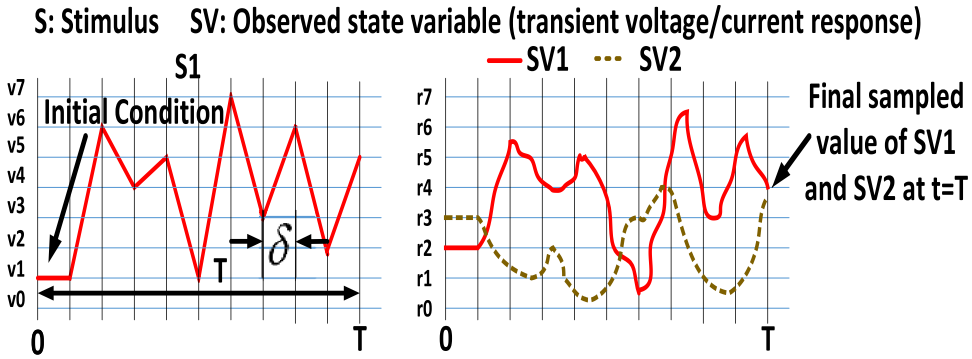


Fig. 4 Spatial Consistency Checking

S1 and sampling the final value of the state variable SV at time t=T using a sample and hold (S/H) circuit, a different stimulus S2 is applied to the device under test (DUT) from t=T to t=2T with the same initial condition as S1. At t=2T, the final value of SV in response to S2 is acquired using an S/H circuit. The sampled values of SV at t=T and t=2T in response to S1 and S2 respectively are then compared. If they are consistent (consistency definition is given in Table 1) then a logic "0" is generated by the error triggering circuit (as shown in Fig. 4), otherwise a logic "1" is generated.

The main concept behind our temporal state consistency checking approach is to design diverse stimuli S1 and S2 that exercise the analog/RF circuit through different state trajectories, while resulting in consistent final states sampled at t=T and t=2T. This hypothesis suggests that an arbitrary design bug or fault is unlikely to affect the state trajectories of SV in response to S1 and S2 identically, resulting in inconsistent final state values.

Type II Test (Spatial State Consistency Checking) Type II tests are utilized to verify consistency among state variables at the same sampling moment. This is in contrast to a Type I test, which examines state consistency of a state variable between two distinct sampling instants. To produce the stimulus, two state variables are observed to be consistent (as defined in Table 1) for the nominal circuit at sampling instant t=T, as demonstrated in Fig. 4. It is important to note that the observed state variable pair may have differing dynamic ranges, necessitating appropriate level shifting and gain compression prior to comparison. In certain cases, such as gain compression and DC offset, the defective circuit may exhibit state consistency under Type I stimuli testing. To identify these faults, we introduce a Type II test, which also examines consistency across state variables.

5 Automatic Test Pattern Generation

The test stimulus used to stimulate the devices in this study is a PWL wave with a finite duration, as illustrated in Figs. 5 and 6. Assuming that the input stimulus has a dynamic range of [0 to V] volts and a duration of T seconds, T is equally divided into time intervals separated by δt seconds. To create the desired PWL wave at time instants $t_0, t_1, t_2 \ldots \ldots t_k$ we require amplitude values of $v_0, v_1, v_2 \ldots v_k$. The generation of test stimuli for type I (temporal state consistency checking) and type II (spatial state consistency checking) tests is explained below:

5.1 Stimuli Generation for Type I Test

In order to conduct a type I test, two distinct stimuli are required that take the circuit to the same final state through different state trajectories. The first step involves generating two stimuli, S1 and S2, with a length of l using a random process (as illustrated in Eq. 1).

$$\begin{aligned} S1 &= \left[v_{11}, v_{12}, \ldots \ldots \ldots v_{1l}\right]^T \\ S2 &= \left[v_{21}, v_{22}, \ldots \ldots \ldots v_{2l}\right]^T \end{aligned} \tag{1}$$

The entropies and dissimilarities of these stimuli are checked using standard deviation and distance correlation, respectively. The distance correlation for two vectors (X,

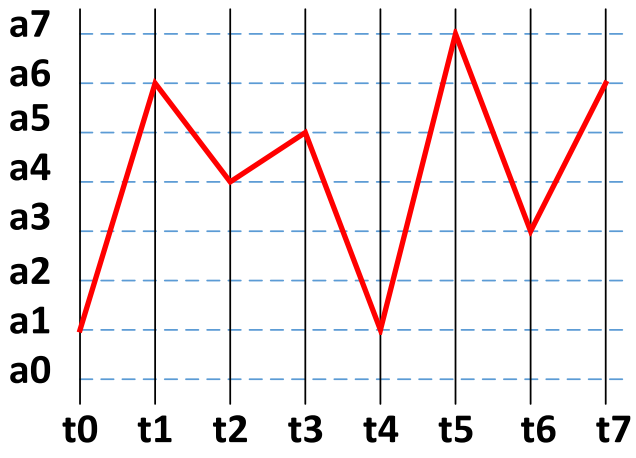


Fig. 5 Transient Test Stimulus

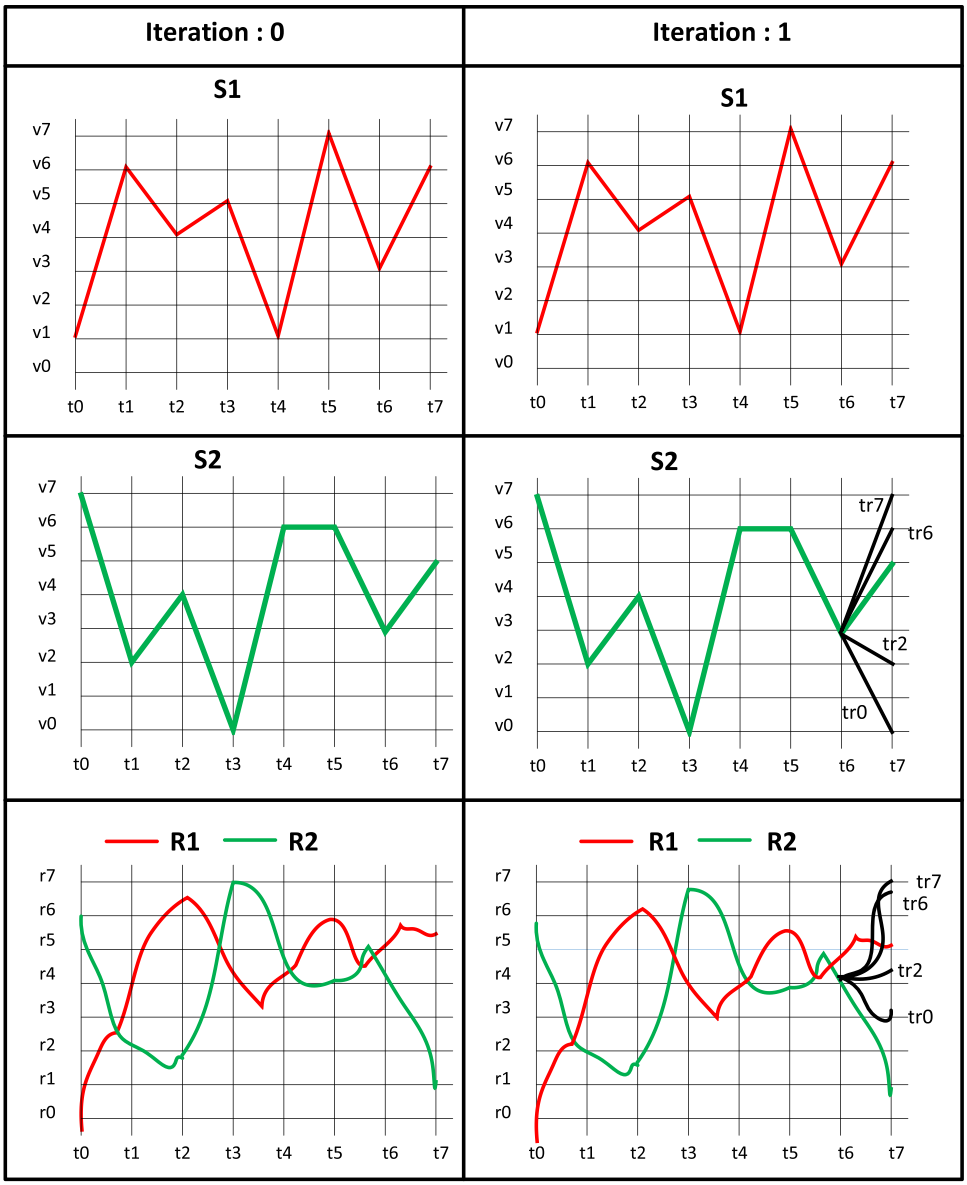


Fig. 6 Type I (Temporal) Stimuli Generation

Y), represented by the samples $(X_i, Y_i)i = 1 \ldots .n$, is given by Eq. (2).

$$dcor(X, Y) = \frac{dcov(X, Y)}{\sqrt{dvar(X) * dvar(Y)}} \tag{2}$$

A more detailed explanation of Eq. (2) can be found in [21]. The entropy check ensures that the signals are diverse in terms of time-frequency, while the dissimilarity check ensures that the two stimuli are distinct from each other. The system is then simulated with stimuli S1 and S2, and corresponding responses R1 and R2 are recorded. The goal of stimulus generation is to match the end responses, R1(l) and R2(l), as closely as possible.

S1 is held constant, and S2 is modified in steps from one end (S2(l), S2(l-1) … up to S2(l-m)). Eq. (3) demonstrates how the S2(l) value is replaced with all possible new values, resulting in a new stimuli set $S2_{new}$. For each new stimuli in $S2_{new,}$ the system is simulated and response set $R2_{new}$ is obtained.

$$\begin{aligned} S2_{New} = \{ &\left[S2(1)_{old}, S2(2)_{old}, \ldots \ldots S2(l-1)_{old}, S2^1(l)\right]^T, \\ &\left[S2(1)_{old}, S2(2)_{old}, \ldots \ldots S2(l-1)_{old}, S2^2(l)\right]^T, \\ &\left[S2(1)_{old}, S2(2)_{old}, \ldots \ldots S2(l-1)_{old}, S2^q(l)\right]^T \} \end{aligned} \tag{3}$$

$$R2_{new} = \{R2^1, R2^2, \ldots \ldots .R2^q\} \tag{4}$$

The chosen stimulus $S2^j$ is the one that minimizes the absolute difference between R1(l) and $R2^j(l)$). This selection process is repeated for S2(l-1), S2(l-3), and so on until R2(l) matches R1(l) with acceptable precision. The algorithm has been presented for all quantized values of S2(l) for clarity,

but a binary search is actually employed in practice. The procedure for generating stimuli is formally outlined in Table 2.

5.1.1 Stimuli Generation for Type II Test

The type II test employs a similar approach to the type I test, in which stimulus S1 is randomly generated and two responses (state variables) R1 and R2 are captured. To compare the spatial relationship between R1 and R2, they must be adjusted for level and compression/expansion. It is assumed that R1 and R2 have already been adjusted properly. S1 is then modified step-by-step from the rear end (S1(l) , S1(l-1)…up to S1(l-m)) following the algorithm in Table 2.

5.1.2 Stimuli Set Formation

While crafting stimuli for type I and II tests, it is ensured that the two responses match within an acceptable accuracy at the sampling instant. Two responses can match at any voltage/current level within the dynamic range. A fair representation from every corner of the dynamic range is ensured when creating the stimuli set.

5.1.3 Stimuli Length Optimization

To optimize the length of stimuli given a finite memory space for storing test stimuli, there is a trade-off between the number of stimuli that can be stored and the length of the stimuli. Assuming that the stimuli sets SS_1 and SS_2 (shown in Eqs. 5 and 6) are formed according to the earlier algorithms, new stimuli sets SS_1^* and SS_2^* are obtained by truncating the length of each stimulus to half from rear end, and appending an initializing sequence before the stimulus. The process is illustrated in Fig. 7. New response sets RS_1^* and RS_2^* are obtained by stimulating the system with new stimuli set. For each new stimulus, the corresponding response is checked to see if it obeys the previously checked objective. If more than 90% of the stimuli meet the objective, the new time duration is accepted. If the condition is not satisfied by 90% of the stimuli, the stimulus length is cut by a quarter and the process is repeated. A formal algorithm for stimuli duration optimization is shown in Table 3.

Table 2 Type I (Temporal) Stimuli Generation Algorithm

Given: Stimuli duration (T), sampling rate (R), stimuli dynamic range (DR), Entropy Threshold, Dissimilarity Threshold
Stimuli length (l) = T/R
Quantize the dynamic range DR into q number of levels
$V = [v_1, v_2, \ldots \ldots v_q]^T$
Step 1: Randomly sample values from V and generate two stimuli S1 and S2 of length l (as shown in equation 1).
Step 2: Perform the following checks
(i) $\sigma_{S1} > Entropy\ Threshold$
(ii) $\sigma_{S2} > Entropy\ Threshold$
(iii) $dcorr(S1, S2) < Dissimilarity\ Threshold$
If all the checks are passed go to step 3, else revert back to step 1
Step 3: Simulate the system with S1 and S2 and system responses R1 and R2 are captured.
If abs(R1(l) – R2(l)) < Comparator Offset
then end the program
Else go to step 4
Step 4: keep S1 fixed, do a binary search on S2 (l-1) to S2 (l) transition so that *abs(R1(l) – R2(l))* is minimized.
Step 5: (i) Repeat the step 4 for S2 (l-2) to S2 (l-1) transition
(ii) Repeat the step 4 for S2 (l-3) to S2 (l-2) transition
.....
(m) Repeat the step 4 for S2 (l-m+1) to S2 (l-m) Transition
Step 6: If abs(R1(l) – R2(l)) < Comparator Offset
Then accept the stimuli S1 & S2 pair
Else go to step 1

$$Type\ I\ Stimuli\ Set\ SS_1 \{(S1, S2)^1, (S1, S2)^2, \ldots ..(S1, S2)^N\} \tag{5}$$

$$Type\ II\ Stimuli\ Set\ SS_2 : \{S3^1, S3^2 \ldots ..S3^N\} \tag{6}$$

$$Type\ I\ Response\ Set\ RS_1 : \{(R1, R2)^1, (R1, R2)^2, \ldots ..(R1, R2)^N\} \tag{7}$$

$$Type\ II\ Response\ Set\ RS_2 : \{(R3, R4)^1, (R3, R4)^2, \ldots ..(R3, R4)^N\} \tag{8}$$

5.1.4 Stimuli Generation Model

It is apparent from the stimuli generation algorithm that it takes a lot of iterations to craft and optimize the stimuli. It would be computationally prohibitive if we use SPICE level simulation. The repeated circuit simulation is based on extracted booleanized models. In our previous work [1, 3, 6] we have shown the efficacy of using these booleanized models in stimuli generation of RF and mixed signal circuits.

6 Test Vehicles used for Pre-silicon Validation

The RF receiver and sigma delta ADC described in this section serve as test vehicles to confirm the effectiveness of the proposed state consistency checking based validation methodology for mixed signal/RF systems in the pre-silicon stage. The RF quadrature receiver system is designed in the 130nm IBM process, while the Sigma Delta ADC is designed in the 45nm predictive transistor model from NCSU. The quadrature RF receiver system (illustrated in Fig. 8) includes an LNA, power splitter and two RF demodulating mixers, with transistor level circuit designs shown in Figs. 9 and 10. RF and analog circuit components are designed in Cadence Spectre, while the ADC and baseband processing are simulated in Matlab. The LO frequency of the designed receiver is 2.4GHz and the in phase and quadrature phase data rate is 1 MHz.

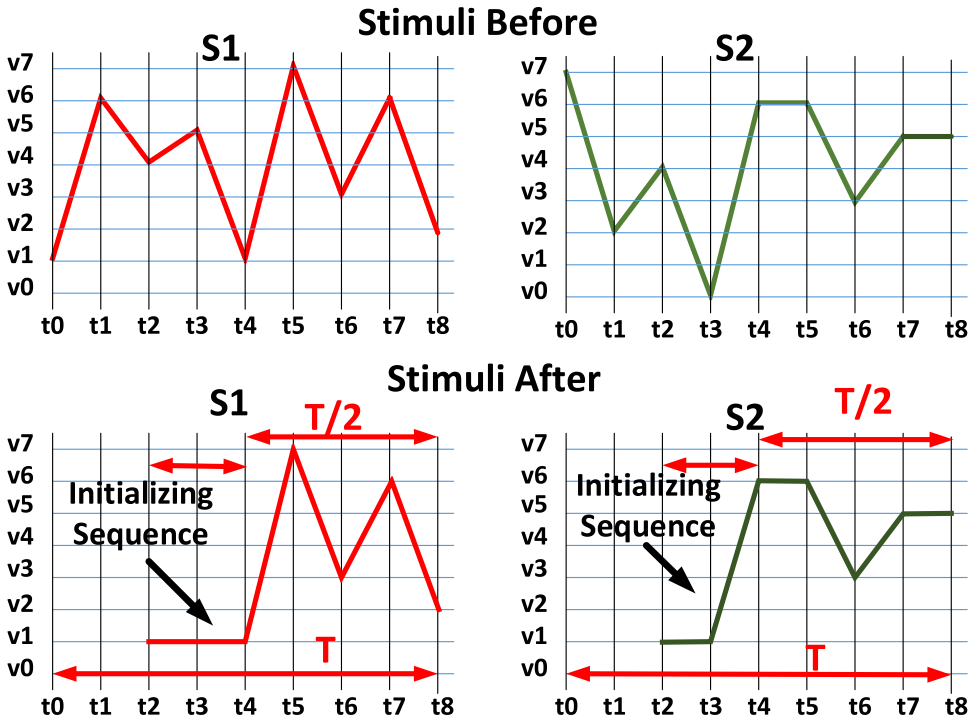


Fig. 7 Stimuli Length Optimization

The second example, Sigma Delta ADC is shown in Figs. 11 and 12, with all the blocks, including sample and hold, opamps, comparator, and D Flip-Flop, designed in Cadence Spectre. The sampling clock and oversample clock frequencies are 1 MHz and 1 GHz, respectively, with an oversampling ratio of 100. Table 4 displays the nominal performance parameters.

Table 3 Stimuli Length Optimization Algorithm

Given: Stimuli duration (T), Stimuli Set SS_1 and SS_2 each of cardinality N
Step 1: Cut every stimulus length to half (T/2) from rear end and append an initializing sequence before it. (See Figure 7)
Stimuli set SS_1^* and SS_2^* are formed from SS_1 and SS_2
Step 2: New response set RS_1^* and RS_2^* are obtained by stimulating the system
Step 3: $SS_1^{**} = \phi$ $SS_2^{**} = \phi$
for i=1 to N
  if $abs(R1^{i*}(l) - R2^{i*}(l)) < Comparator\ Offset$
    $SS_1^{**} = SS_1^{**} \cup \{(S1^*, S2^*)^i\}$

for i=1 to N
  if $abs(R3^{i*}(l) - R4^{i*}(l)) < Comparator\ Offset$
    $SS_2^{**} = SS_2^{**} \cup \{S3^{*i}\}$

Step 4: *if* $|SS_1^{**}| > 0.9N$ && $|SS_2^{**}| > 0.9N$
  // more than 90% stimuli obey the objective even after cutting down to half length
    go to step 1and repeat the process
  Else
    Cut every stimulus length to three quarter (3T/4)from rear end and append an initializing sequence before it. Stimuli set SS_1^* and SS_2^* are formed from SS_1 and SS_2. Go to step 2 and repeat the process.

7 DFX Circuitry

BISCC methodology is built upon internal circuit state monitoring. For RF/Analog circuits, node voltages and branch currents can be thought of state variables of the system.

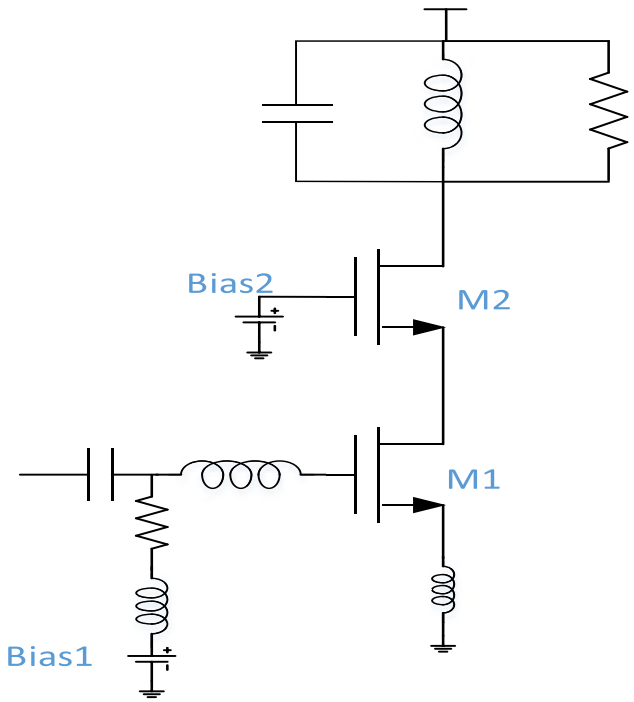


Fig. 8 Cascode LNA

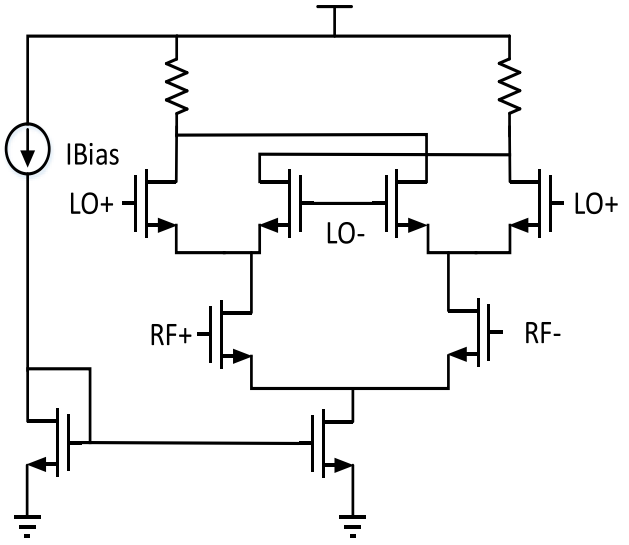


Fig. 9 Gilbert Cell Mixer

We need non-intrusive DFX circuitry to monitor internal voltages and currents, so that the monitoring circuits do not interfere with the actual operation of the circuit. In this section, we describe the DFX circuitry needed to implement BISCC in post silicon stage. The envelope detector is employed in RF transceivers to extract the low frequency characteristics from the modulated voltage signal. On the other hand, in Sigma-Delta ADC, a low pass filter is utilized to capture the low frequency signal. For supply current sensing, a small resistance, R_{sense}, is utilized to convert the supply current to voltage, as illustrated in Fig. 13. Subsequently, amplification and low pass filtering are carried out by the op-amp and low pass filter, respectively.

There are two types of error trigger architectures shown in Figs. 14 and 15 respectively. For temporal architecture (Fig. 14), two stimuli are so designed that they take the circuit to the same state at the sampling instant. These two stimuli are concatenated while applied to DUT. So we need to compare between previously sampled value and present sampled value. A sample & hold circuit is used to hold the previously sampled value. For type II tests, as the comparing signals are coming from two different circuit nodes, no such holding is required.

The error triggering mechanism is shown in Fig. 16. If s1 and s2 are within comparator offset voltage (region t3<t<t4 in Fig. 16) then none of the comparators will trip and no error signal will triggered. If (s1-s2)>comparator offset voltage (region t<t3 in Fig. 16) then comparator 1 will trip and generate an error signal. If (s2-s1)>comparator offset voltage (region t>t4 in Fig. 16) then comparator 2 will trip and generate an error signal.

8 DFX Infrustructure Placement

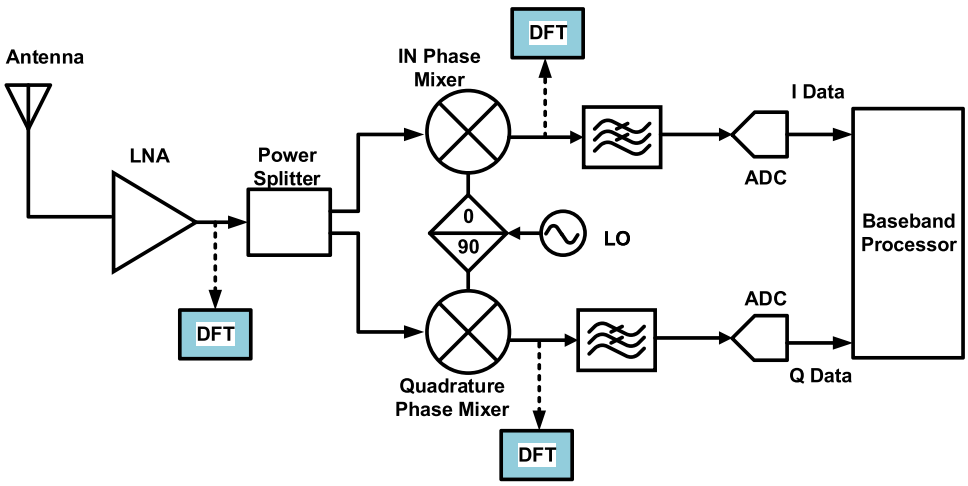
In Sect. 3, we have discussed state consistency checking of state variables. This section will cover the selection of which state variables are needed and how many are required to diagnose a system. All state variables are observable in the pre-silicon stage, while DFX structures must be implemented in the design to observe selected state variables in the post-silicon stage.

During simulation, we select all possible non-intrusive DFX sensor positions within the system and collect sensor data for a long random stimulus. We then identify the sensors that are volatile based on a threshold volatility, which indicates the richness of the sensor's information about the system. As the dynamic ranges of all sensors are not the same, we use a scale-free volatility measure provided in equation (9).

$$volatility = standard\,deviation/mean \tag{9}$$

Assuming the type I test set is SVS1, shown in Eq. 10, we conduct a type II test to check for state consistency

Fig. 10 RF Receiver



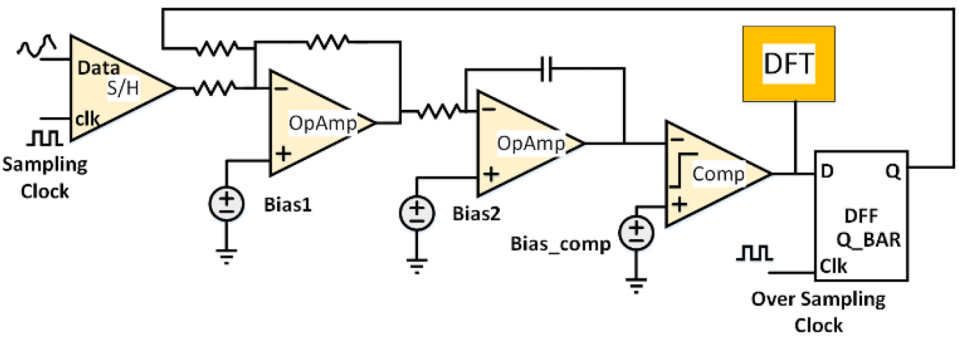


Fig. 11 1st Order Sigma Delta ADC

between a pair of state variables at the same sampling instant. We use the type I test set to create a pairwise variable set, as shown in Eq. 11, and compare the cross-correlation between every pair.

$$SVS1 = \{SV_1, SV_2 \ldots SV_k\} \tag{10}$$

$$\left(SV_i,\ SV_j\right)\ s.t\ i \neq j\ and\ i, j = 1(1)k. \tag{11}$$

In a circuit, the observed state variable pair may be phase-shifted, so we use the Matlab function "xcorr" to enumerate cross-correlation. The maximum shifted cross-correlation serves as a metric to select the state variable pair, and the formal state variable selection algorithm is presented in Table 5. The observed state variables for the SISO RF receiver system (see Fig. 8) are defined in Table 6.

For SISO RF receiver system example, we selected six DFX sensors, and the obtained signatures for a long random stimulus are shown in Fig. 17. The volatility metric of each sensor is presented in Table 7, with sensors placed at positions 1, 2, 3, and 4 deemed acceptable, while sensors 5 and 6 do not provide sufficient information to diagnose the system. State variables 5 and 6 correspond to the bias currents of the In-Phase and Quadrature mixer, respectively, which are biased at high DC current, making their supply currents less sensitive to AC input stimulus. The accepted state variables form the type I test set.

$$Type\ I\ Test\ Set = \{State\ Variable\ 1, 2, 3, 4, 7, 8\} \tag{12}$$

From the type I test set given in Eq. (12), we create a pairwise state variable set and compare the cross-correlation between each pair. The pairwise maximum cross-correlation plot is shown in Fig. 18, and we chose the following pairs $\{1, 4\}, \{2, 4\}, \{1, 2\}, \{4, 6\}$. Similar experiments were conducted for the Delta Sigma ADC, and the defined tests are presented in Table 8.

9 Pre-silicon Simulation Results

Fault models used in this work are random process variation and capacitive/resistive open/short in the netlist. For RF receiver example individual transistor widths, threshold voltages, resistance, capacitance, inductance values and bias voltages all together 30 parameters were randomly varied to create off the nominal circuits. Random capacitive/resistive open/shorts were introduced in the LNA and mixer netlists to create faulty circuits. Similar process variation and open/shorts were introduced in Sigma Delta ADC netlist to create

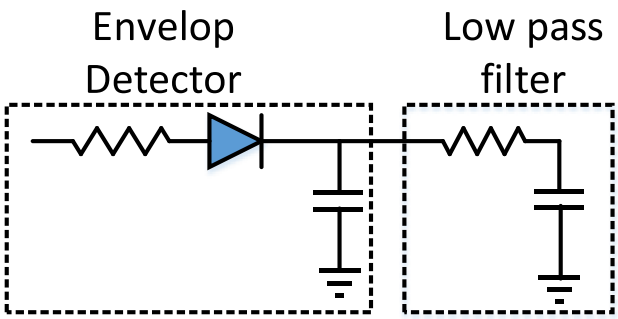


Fig. 12 Low Frequency Voltage Signal Capturing Circuit for RF Receiver

Table 4 Nominal Sigma Delta ADC Specifications

SFDR	THD	ENOB
30.44 dB	-10.31 dBc	4.76

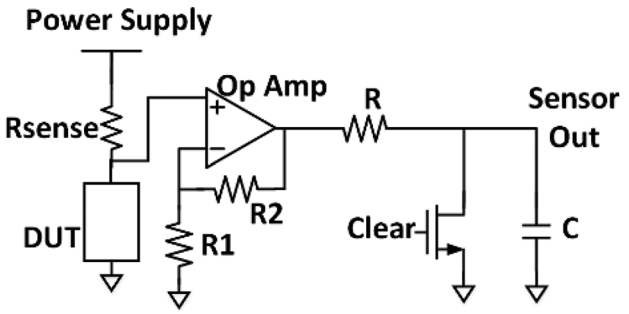


Fig. 13 Supply Current Sensor

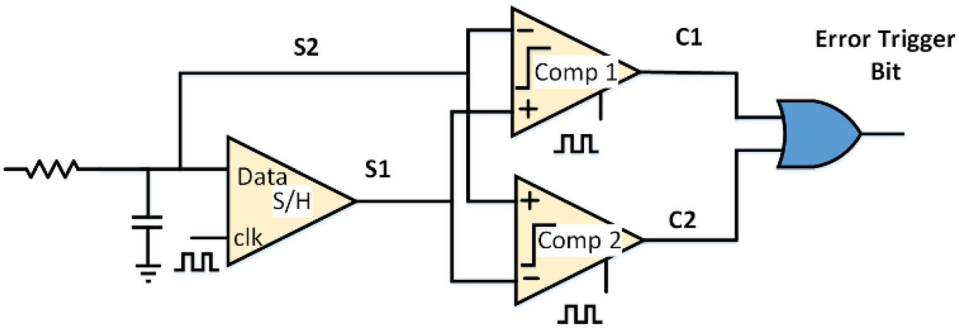


Fig. 14 Temporal Error Trigger DFT Architecture (ComparingSignals from Same Circuit Node at Two Successive Sample Time Instants)

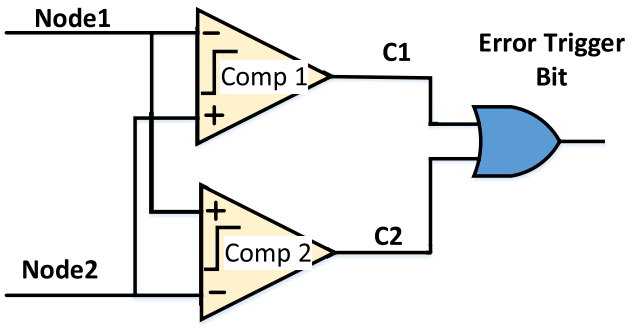


Fig. 15 Spatial Error Trigger DFT Architecture (Comparing Signals from Two Different Circuit Nodes)

off the nominal circuits. In this work, we have used percentage of bits flipped as a metric to quantify error (given in Eq. 13).

$$\%\ bit\ flipped = \frac{Hamming\ Distance\ (R_{exp}, R_{obt})}{length\ of\ R_{exp}} \times 100 \quad (13)$$

R_{exp} : Expected Digital Bit Stream
R_{obt} : Obtained Digital Bit Stream

Table 5 State Variable Selection Algorithm

Given: State Variable Set $SVS = \{SV_1, SV_2, \ldots \ldots SV_m\}$
Objective: Find State Variable Set SVS1 for type I test and SVS2 for type II test
Step 1: Take a long random stimulus and stimulate the system to collect the system response. All state variable values corresponding to the applied random stimulus are acquired.
Step 2: SVS1={}
For i=1 to m
  If volatility(SV_i) > Threshold Volatility
    SVS1 = SVS1 ∪ SV_i
Step 3: $k = |SVS1|$ (cardinality of set SVS1) SVS2={}
For i=1 to k
  For j=1 to k
    If $i \neq j$
      Max_crosscorr=max(xcorr(SVS1(i),SVS1(j)))
      If Max_crosscorrelation > ThresholdCrossCorr
        $SVS2 = SVS2 \cup \{(SVS1(i), SVS1(j))\}$

9.1 Test Case 1: Delta Sigma ADC

Process Varied Circuit Table 9 illustrates an instance of a validation test case for a Sigma Delta ADC. The faulty circuit parameters in this case deviate significantly from the nominal circuit parameters, and are obtained by varying the design and process parameters. The test design includes 400 pairs of stimuli for type I testing and 100 stimuli for type II

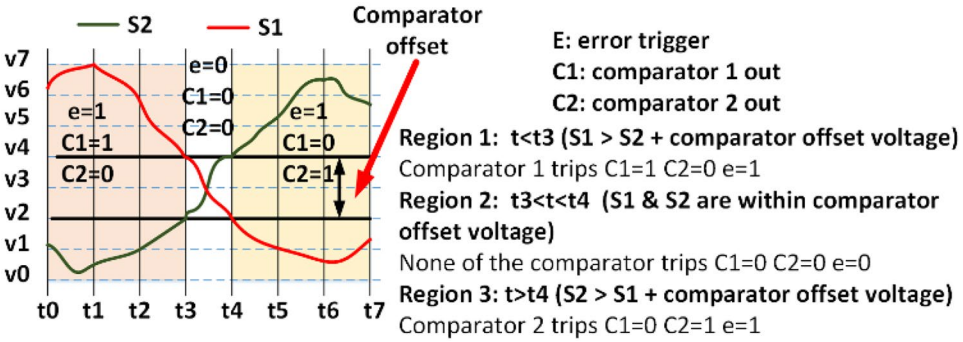


Fig. 16 Error Trigger Operation

Table 6 State Variable Definition for RF Receiver System

State Variable	Definition	Test #
State Variable 1	voltage signature captured by the envelope detector placed at the output of the LNA	Type I Test 1
State Variable 2	voltage signature captured by the envelope detector placed at the output of the In Phase Mixer	Type I Test 2
State Variable 3	voltage signature captured by the envelope detector placed at the output of the Quadrature Phase Mixer	Type I Test 3
State Variable 4	current signature captured from LNA supply current	Type I Test 4
State Variable 5	In Phase input data	X
State Variable 6	Quadrature Phase input data	X
State Variable 7	current signature captured from In Phase Mixer supply current	X
State Variable 8	current signature captured from Quadrature Phase Mixer supply current	X
State Variable pair 1	{State Variable 1, State Variable 4}	Type II Test 1
State Variable pair 2	{State Variable 2, State Variable 4}	Type II Test 2
State Variable pair 3	{State Variable 1, State Variable 2}	Type II Test 3

testing. Simulation result for one of the 400 stimuli is shown in Fig. 19. Output response of the nominal circuit for input 1 and input 2 differ by 1mv, while the difference is 70mv for faulty circuit. For type I and II, 81% and 96% error triggering bits are flipped respectively.

Comparator Bias Voltage Variation Another test example is constructed by varying bias voltage of the comparator used in Sigma Delta ADC. Identical stimuli set as of the previous example is applied in this case and the validation results are shown in Table 10.

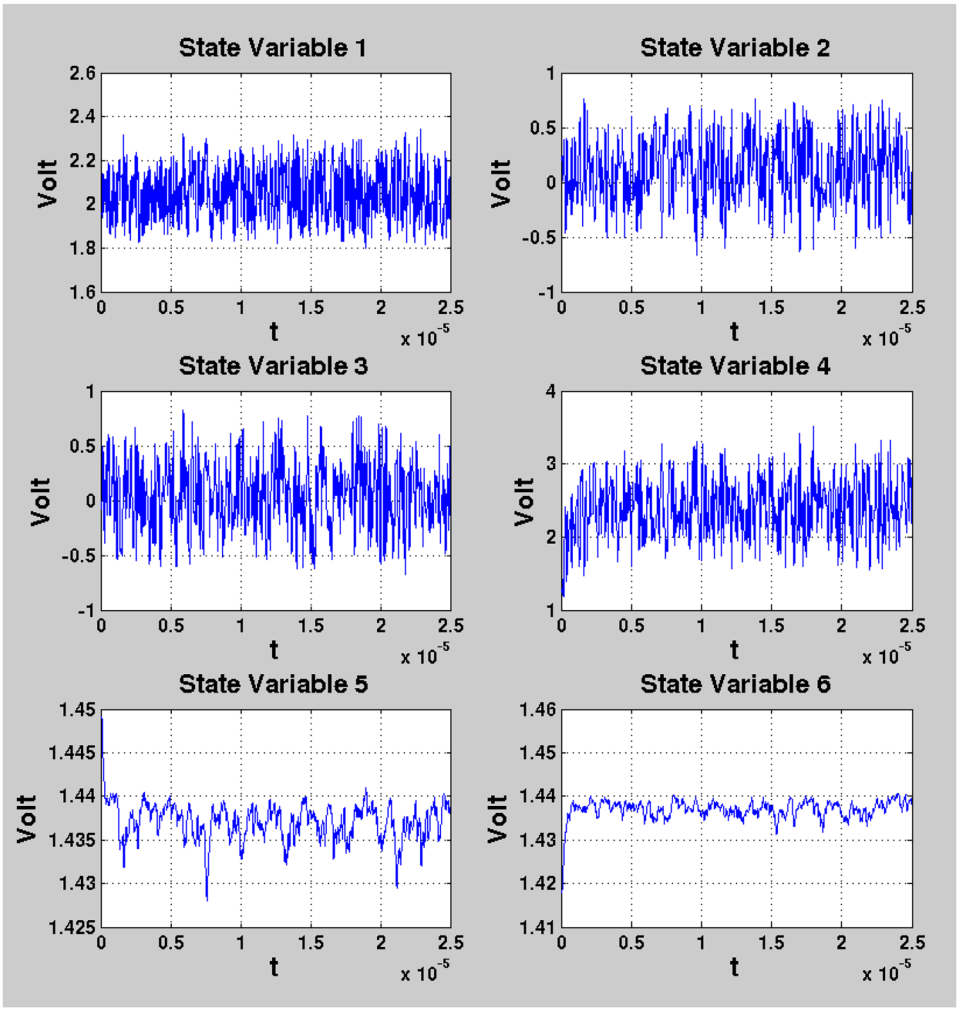


Fig. 17 Observed State Variables for a Random Input Stimulus

Table 7 Volatility of Observed State Variables (RF Receiver System)

	Standard Deviation	Volatility	Accept/Reject
State Variable 1	0.1112	0.0541	√
State Variable 2	0.2784	2.5187	√
State Variable 3	0.2881	6.6280	√
State Variable 4	0.3671	0.1537	√
State Variable 5	0.0021	0.0014	X
State Variable 6	0.0200	0.0014	X

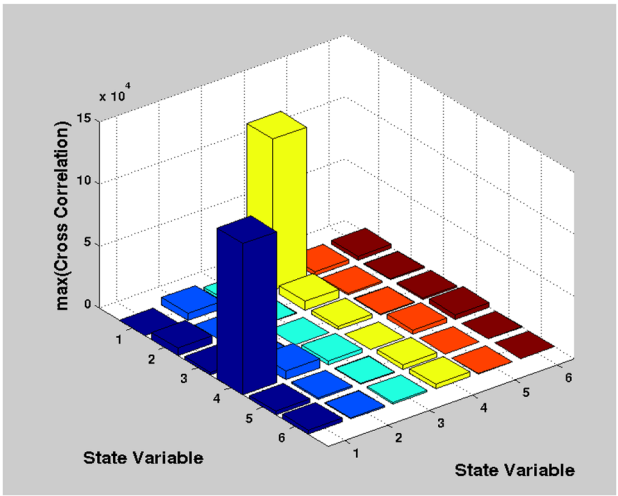


Fig. 18 Pairwise Maximum Cross Correlation among State Variables

9.2 Test Case 2: SISO RF Receiver System

Faulty In-Phase Mixer (Bias Voltage Variation) An example test case is created by altering bias voltage of the In-Phase Mixer (other design and process parameters were not altered). Diagnosis result is shown in Table 11. Although fault isolation is not covered in this work, the diagnostic results shows that the state variables associated with In Phase Mixer causing more bit flips than the others.

DC Offset and Gain Change We devised two sample test cases: (i) incorporating a DC offset in the output of the LNA, and (ii) enhancing the gain of the In-Phase Mixer through modifications to the design parameters. For case i, state variable 1 (capturing LNA output signature) and for case ii, state variable 2 (capturing In Phase Mixer output signature) are plotted in Fig. 20 and in Fig. 21 respectively. Sampled values at t=T_1 and at t=T_2 for the faulty circuits are consistent. While the accuracy of Type I test is low in these two pathological cases, type II tests catch these faults easily (see Table 12). The above observation can be attributed to the fact that DC offset or Gain variation will not show appreciable temporal difference (type I tests) while spatially different signals will show appreciable difference (type II tests).

Table 9 Sigma Delta ADC Validation Test Case (process Varied Circuit)

	Nominal Circuit	Faulty Circuit
Specifications		
SFDR (dB)	30.44	22
THD (dBc)	-10.31	-2
ENOB (Bits)	4.76	3.36
Diagnosis		
Percentage of bits flipped triggering error		
Type I Test 1	0	81.0
Type II Test 1	0	96.0

Temperature Variation Fig. 8 depicts the RF receiver system, which is designed to function between 0 °C and 50 °C. Burn In (high temperature) test is used for detecting infant mortality [11] and low temperature test is useful to uncover reliability issues and transient faults as opposed to catastrophic faults [7, 12]. In two instances, the temperature range exceeded the acceptable limit, and Table 13 displays how the built-in assertion-based diagnosis raises an error flag during validation. The results indicate that all type II tests indicate device malfunction at temperatures of 100 °C and -20 °C, whereas type I test 1 does not detect any errors. Figs. 22 and 23 illustrates the observed state variable 1 for a random signal input applied to the RF receiver system. The captured responses indicate gain compression/enhancement, which varies in amplitude depending on the temperature. As previously explained, if the anomaly observed is solely due to gain compression/enhancement, a type I test would fail.

Manufacturing Production Testing (Binning) The following example shows how BISCC can be used in production testing (binning). Employing the fault model described earlier, we have created 1000 process varied, and 200 capacitive/resistive open/short netlists of the RF Receiver (Fig. 8).

Table 8 State Variable Definition for RF Delta Sigma ADC

State Variable 1	Voltage signal captured by a low pass filter placed at the output of the comparator	Type I Test 1
State Variable 2	Input sampled value at the output of the S/H circuit	X
State Variable Pair 1	{State Variable 1, State Variable 2}	Type II Test 1

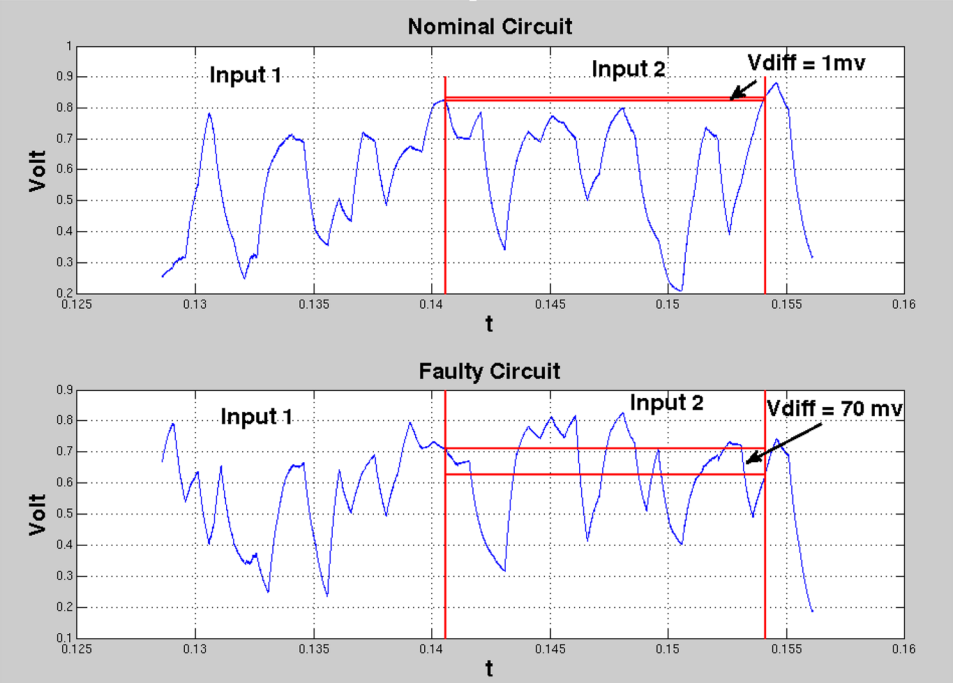


Fig. 19 Simulation Result for a pair of stimuli (Error Triggered in Temporal Architecture)

The type I and II tests described earlier are applied to the population of 1200 devices. Device classification definitions are given in Table 14. Binning test accuracy is shown in Table 15. Misclassification rate is 2.1% (1.8% yield loss and 0.3% Test Escape) and re-test rate is 11%.

Table 10 Sigma Delta ADC Validation Test Case (Comparator Bias Voltage Varied)

Tests	Percentage of bits flipped triggering error		
	Nominal Circuit	Comparator Bias Voltage Reduced by 20 %	Comparator Bias Voltage Reduced by 10 %
Type I Test 1	0	82.7	81.3
Type II Test 1	0	92.6	93.5

10 Post-Silicon Measurement Results

In this section, we will demonstrate the feasibility of BISCC in post-silicon test cases. We have demonstrated BISCC on two RF systems, a MIMO RF Receiver and a RF Transmitter. For RF systems, BISCC does not need expensive high frequency test instrumentation to observe RF signals. For voltage sensing we have used a low cost envelope detector, and in built source current monitor of power supplies is used as current sensor. For Power Amplifier and LNA we have used TI transceiver IC (X35337AZ-CYH3) and the associated load board. We have received and characterized about 500 of these ICs. Out of these 500, one is used as nominal (reference) and the others are used as process-varied instances.

Table 11 Pre-Silicon Validation Results of RF Receiver (In Phase Mixer Bias is Varied)

Tests	Percentage of bits flipped triggering error	
	In Phase Mixer's Bias Voltage Change 5%	In Phase Mixer's Bias Voltage Change 10%
Type I Test 1 (State Variable 1)	5.1	5.3
Type I Test 2 (State Variable 2)	52.1	68.0
Type I Test 3 (State Variable 3)	23.1	30.1
Type I Test 4 (State Variable 4)	4.8	5.0
Type II Test 1 (State Variable pair 1)	12.1	13.3
Type II Test 2 (State Variable pair 2)	14.8	13.8
Type II Test 3 (State Variable pair 3)	46.6	73.3

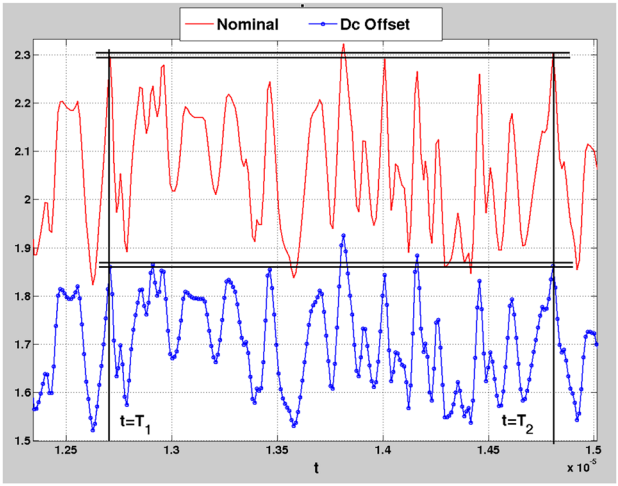


Fig. 20 State Variable 1 (LNA DC offset)

10.1 MIMO RF Receiver

Majority of the electrical post-silicon defects arises from signal coupling, noise coupling and supply voltage variation. A 2x2 MIMO receiver with two chains of RF receiver is used as test vehicle here. As shown in Fig. 24, a coupling fault is introduced by inserting a capacitance between LNA output nodes of the chains. This fault will show up in actual MIMO mode of operation and will corrupt received MIMO data.Conventional RF specification testing (EVM testing) will not be able to catch this defect as EVM testing is done in SISO mode sequentially, the coupling defect will not be activated in SISO mode. The only way to excite this defect in testing is to test the two chains concurrently (required two sets of costly RF test instruments), with different data pattern on each chain.. How BISCC methodology proposed in ths paper catches this defect is shown in Table 16. Here SV1 & SV2 are supply current sensor readings and SV3 & SV4 are envelope detector outputs.

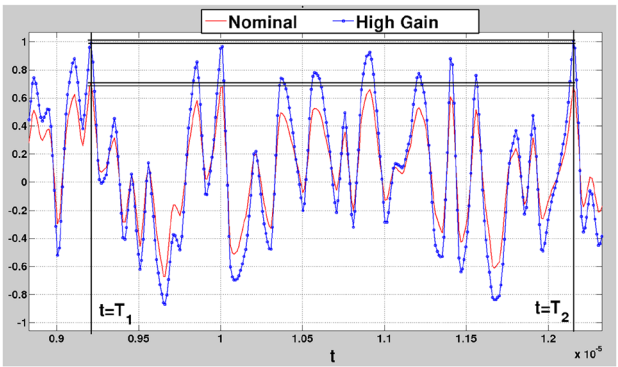


Fig. 21 State Variable 2 (In Phase Mixer Gain Error)

Table 12 Pre Silicon Validation Results of RF Receiver (DC Offset and Gain Error)

Fault	Percentage of bits flipped triggering error	
	DC Offset at LNA	Gain Error at In Phase Mixer
Type I Test 1 (State Variable 1)	11	12
Type I Test 2 (State Variable 2)	83	25
Type I Test 3 (State Variable 3)	80	34
Type I Test 4 (State Variable 4)	13	15
Type II Test 1 (State Variable pair 1)	80	71
Type II Test 2 (State Variable pair 2)	83	68
Type II Test 3 (State Variable pair 3)	90	76

10.2 RF Transmitter

The 2nd post silicon test example, RF Transmitter is shown in Figs. 22 and 25. Here SV1, SV2, SV3 are envelope detector voltages and SV4, SV5 are supply currents. Various test cases (injected faults) are shown in Table 17. BISCC diagnostic accuracies for various tests are shown in Table 18.

10.3 Test Time Reduction

According to reference [16], it takes at least 300ms to conduct EVM testing on a transceiver. In our manufacturing testing of the receiver, we utilized 1000 stimulus pairs for type I testing and 200 stimuli for type II testing. Each stimulus has a duration of 0.5µs, which results in a total test time of 1.1ms (2200*0.5µs). The test time for the RF transmitter is also 0.7ms. It's important to note that EVM testing alone does not offer diagnosis capability. While we did not focus on diagnosis and fault isolation in this work, the methodology we describe is capable of achieving that. We plan to explore diagnosis using state consistency as future work.

Table 13 Post Silicon Validation Results of RF Receiver System at Various Temperatures

System temperature	Percentage of bits flipped triggering error		
	27 °C	100 °C	-20 °C
Type I Test 1 (State Variable 1)	0	1	4
Type I Test 2 (State Variable 2)	0	11	70
Type I Test 3 (State Variable 3)	0	12	67
Type I Test 4 (State Variable 4)	0	1	6
Type II Test 1 (State Variable pair 1)	0	63	75
Type II Test 2 (State Variable pair 2)	0	55	69
Type II Test 3 (State Variable pair 3)	0	66	73

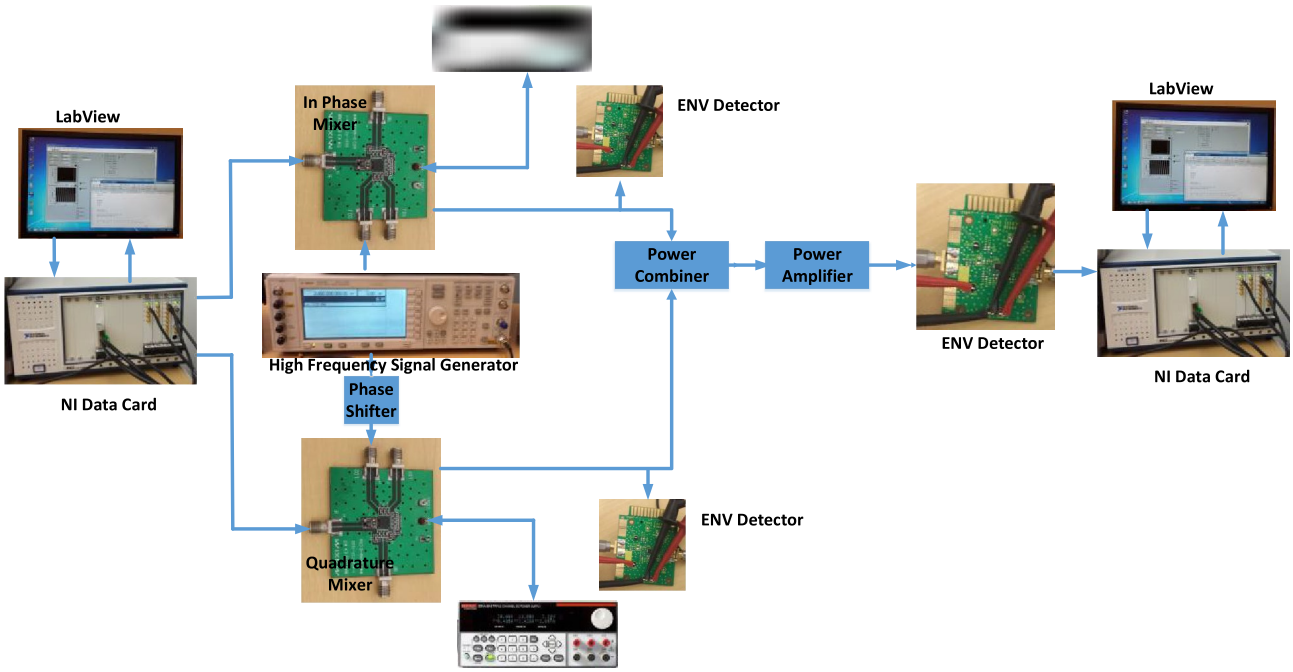


Fig. 22 Hardware test setup (RF Transmitter)

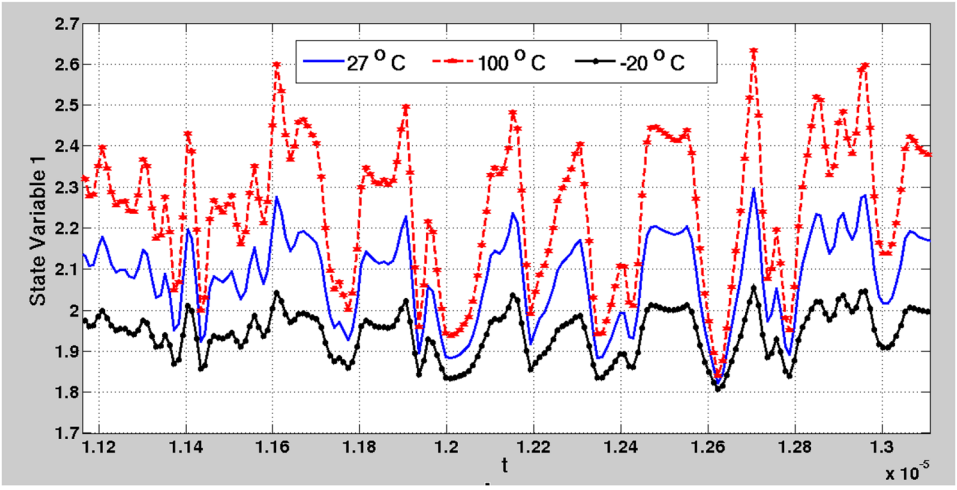


Fig. 23 Captured State Variable 1 for a Random Stimulus

Table 14 Device Classification Definitions for Manufacturing Testing

	Definitions
Good threshold	20% (or less) of error trigger bits are logic "1"
Bad threshold	50% (or more) of error trigger bits are logic "1"
good	A device is good if for all the test the error trigger bits below the good threshold
bad	A device is bad if for any of the tests the error trigger bits above the bad threshold
marginal	A device is marginal if it is neither good nor bad. If a device is classified as marginal, then the test cannot say confidently whether the device is good or bad. It indicates that further conventional testing is required.

Table 15 Manufacturing Test Result for RF Receiver System

	Type I and II Tests
Test escape (%)	0.3
Yield loss (%)	1.8
Re test needed for Marginal devices (%)	11

Table 16 Post-Silicon Validation Results of RF Receiver

	Percentage of bits flipped triggering error
Type I Test 1 (SV2)	89
Type I Test 2 (SV4)	91
Type I Test 3 (SV6)	92

*SV State Variable

11 BISCC Diagnostic Accuracy

In this section BISCC diagnostic accuracy parameters will be discussed.

11.1 Comparator Precision

In post silicon stage, BISCC methodology depends on internal comparator precision. Diagnostic capacity of BISCC increases with precision of the comparator. In pre-silicon stage, although the precision can be infinite (simulation accuracy), still a finite precision (guard band) is imposed to avoid misclassification. However, in the post silicon stage, the comparator circuit design includes a threshold voltage limitation that serves as a guard against tolerable process variation and noise. It is important to note that no two circuits will respond identically in the post silicon stage, therefore a tolerance limit for analog/ RF circuit must be considered, which is dependent on the specific circuit and technology being used. The minimum value of the comparator threshold voltage is circuit-related rather than DFT-related. On the other hand, the maximum value of the comparator threshold voltage is DFT-related. Fig. 26 shows that SV2 and SV3 become ineffective after a threshold voltage of 10mv, while Sv1 remains effective up to a threshold voltage of 50mv.A study of comparator precision vs BISCC diagnostic accuracy for the above example (Post Silicon RF Transmitter example) is shown in Fig. 26.

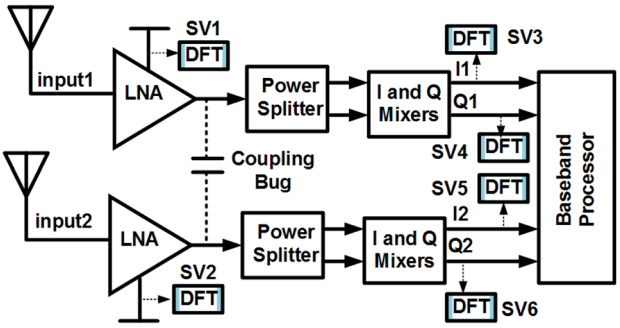


Fig. 24 2x2 MIMO Receiver

11.2 Effects of Sampling Clock Jitter

Given that the proposed validation methodology is a self-checking scheme, which ensures state consistency within the circuit/system across time and space, some may question how sampling clock jitter could impact its performance. To address this concern, we conducted simulations (detailed in Table 19 and Table 20) to assess the efficacy of the proposed

Fig. 25 RF Transmitter

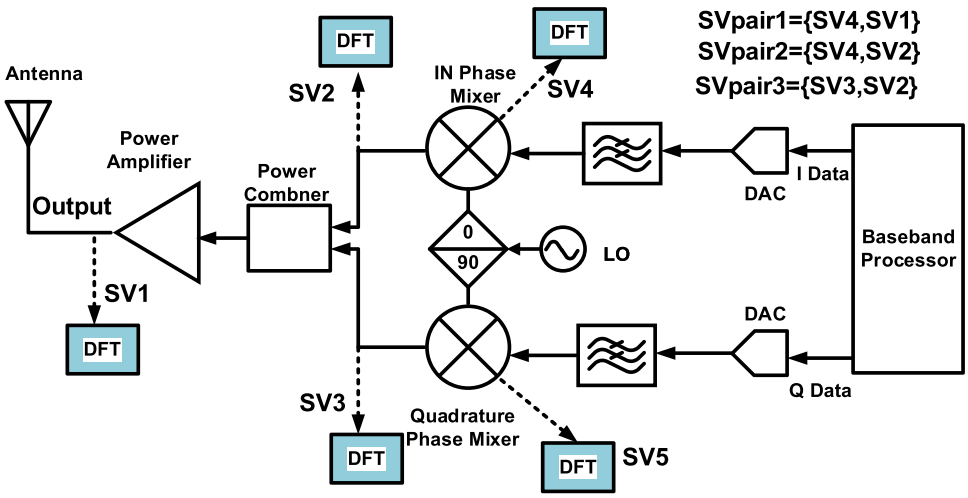


Table 17 Test Cases of the RF Transmitter

Test Case #	Description
Test Case 1	Phase shift introduced in quadrature mixer's LO (10°)
Test Case 2	Voltage droop in In Phase Mixer's BIAS circuitry
Test Case 3	Process Varied PA having phase error

Table 18 Post-Silicon Validation Results of RF Transmitter (*SV: State Variable)

Test Case #		Percentage of bits flipped triggering error (comparator threshold 10mv)
Test Case 1	Type I Test 1 (SV1)	93
	Type I Test 2 (SV2)	39
	Type I Test 3 (SV3)	0.3
Test Case 2	Type I Test 1 (SV1)	87
	Type I Test 2 (SV2)	29
	Type I Test 3 (SV3)	20
Test Case 3	Type I Test 1 (SV1)	93
	Type I Test 2 (SV2)	0
	Type I Test 3 (SV3)	0.3

Table 19 Effect of Random Clock Jitter on Nominal Circuit's (RF Receiver) State Reachability for Type I Test

Random Clock Jitter (ns)	Error Trigger (%)		
	Type I		
	State Variable 1	State Variable 2	State Variable 3
0	0	0	0
1	1.6	1.7	1.6
2	2	2.1	2.2

methodology when subjected to random clock jitter. Specifically, we employed 1000 stimuli pairs for type I testing and 200 stimuli for type II testing, using a sampling clock frequency of 10MHz (with a sampling clock period of 100ns). Our results indicate that, for type I testing, the average error trigger rate is 1.65% for 1ns random jitter and 2.1% for 2ns random jitter.

Table 20 Effect of Random Clock Jitter on Nominal Circuit's (RF Receiver) State Reachability for Type II Test

Random Clock Jitter (ns)	Error Trigger (%)		
	Type II		
	State Variable pair 1	State Variable pair 2	State Variable pair 3
0	0	0	0
1	0	0	2.5
2	1.9	2.6	2.0

12 Conclusion and Future Work

The authors have demonstrated a novel low cost, quick to implement volume validation DFX technique for embedded RF/analog/mixed-signal systems. Observability is a major issue in embedded RF/analog/mixed-signal system validation. It will become even more challenging when various chiplets are connected inside package. We need embedded on chip DFX capability to test and validate these systems. In this paper the authors demonstrated a built in self-validate methodology for RF/analog/mixed-signal systems with on chip signature capturing and temporal and spatial signature comparing infrastructure. The proposed BISCC technique can immensely accelerate long time consuming electrical volume validation. Although anomaly detection technique proposed in this work can be further extended to fault isolation or finding the root cause of system electrical failure, fault isolation is left for future developments of the presented research work. Vdd ramping technique proposed in [19] for mixed-signal/

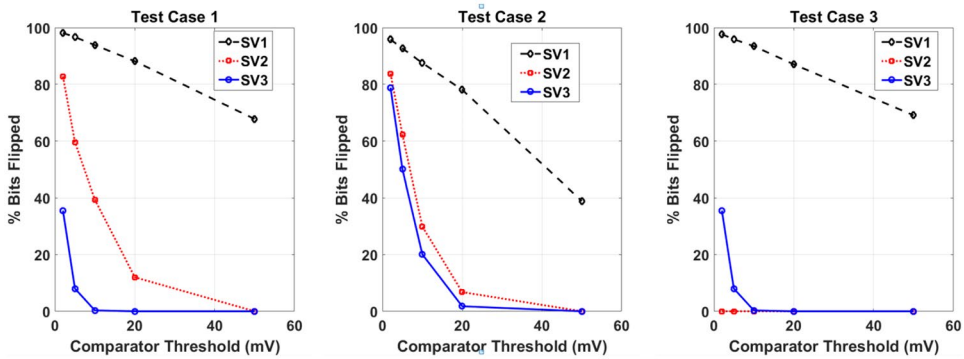


Fig. 26 Comparator Threshold Voltage Vs Diagnostic Accuracy

RF validation is an orthogonal approach to the proposed BISCC scheme of this work. In future, the authors would like to integrate Vdd ramping into the proposed scheme.

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Data Availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of Interest Author Abhijit Chatterjee had received funding for this research from the following sources NSF under Grants CNS 1441754, ECCS 1407542 and by SRC under GRC Task 2555.001. The authors have no relevant financial or non-financial interests to disclose. The authors have no competing interests to declare that are relevant to the content of this article. All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript. The authors have no financial or proprietary interests in any material discussed in this article.

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