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Low Overhead and High Stability Radiation-Hardened Latch for Double/Triple Node Upsets

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Abstract

To tolerate Double Nodes Upset (DNU) and Triple Nodes Upset (TNU), we propose the DNU Tolerant Latch (DNUL) and TNU Tolerant Latch (TNUL) with low overhead and high stability. Both DNUL and TNUL are composed of the looped Input-Split C-Elements (ISCs) and the C-Elements (CEs) at the output level. Based on the robust blocking ability of the ISCs, the simultaneous upset of all inputs of the CE can be blocked. DNUL and TNUL have low overhead with fewer transistors by utilizing the clock-gating and high-speed path technique. Exhaustive HSPICE simulation shows that, in contrast to previous DNU tolerant latches, DNUL is optimal in terms of delay, power consumption and product of delay and power (PDP), but is suboptimal in terms of area overhead. Compared with all alternative structures, TNUL is the best in terms of delay and PDP. Compared to other TNU tolerant latches, TNUL achieves a suboptimal power consumption and area overhead. Variation analysis shows that DNUL and TNUL are insensitive to variations of process, voltage and temperature (PVT).

Keywords Single Event Upset · Double Nodes Upset · Triple Nodes Upset · C-Element · Radiation hardened

1 Introduction

With the scaling of the integrated circuits, the feature size of transistors has entered the nano-scale. The supply voltage and node capacitance are decreasing, causing a constant decrease in the critical charge of the internal nodes [14]. When the energetic particles hit the sensitive regions of the device, charges are deposited on their trajectory of movement. These deposited charges will be collected by source/drain during drift and diffusion. When the collected charge exceeds the critical charge of the node, the logic value of the node will be upset [9]. When the effect occurs in sequential logic, such as latches and flip-flops, it is called Single Event Upset (SEU). If the SEU occurs and causes the logic value of a single node of the storage module to upset, it is called a Single Node Upset (SNU). Due to the decrease in feature sizes, the distance between the internal nodes continually decreases. Because of the effect of charge sharing, the deposited charges may be simultaneously collected by two or more internal nodes [7, 24]. This causes the Double Nodes Upset (DNU) or Multiple Nodes Upset (MNU) [21]. In particular, the aerospace is littered with high energy particles such as protons, neutrons, α particles and γ Rays, which increases the probability of SNU and MNU for space applications [3, 6]. Prior research shows that DNU and MNU

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have become the most dominant factors inducing soft errors in sequential elements [10]. Radiation Hardened By Design (RHBD) is suitable for mitigating SNU/MNU and can effectively harden circuits to provide high reliability. In addition, there are device-level and system-level hardened methods, such as Radiation Hardened By Process (RHBP) and Error Correction Codes (ECC) [5].

In this paper, we propose a low overhead DNU tolerant latch (DNUL). Based on the robust blocking ability of Input-Split C-Elements (ISCs) [11], six ISCs are connected into a large subtle feedback loop. And specific three internal nodes feed the Triple-input C-Element (TCE) to provide the output. DNUL achieves complete tolerance of DNU. We also propose a low overhead TNU tolerant latch (TNUL), as an extension of DNUL. The number of ISCs in the feedback loop is increased to eight. And specific four internal nodes feed the two-level CEs to provide the output. TNUL achieves complete tolerance of DNU. The proposed latches utilize a high-speed path technique to reduce the propagation delay. The introduction of clocked ISCs and clocked C-Elements can effectively reduce the power consumption. Extensive HSPICE simulation shows that the proposed latches achieve advantages in terms of delay, power consumption, PDP and area overhead. Variation analysis shows that the proposed latches are insensitive to process, voltage and temperature (PVT) variations.

The rest of the paper is organized as follows: Section 2 describes the previous hardened latches; Section 3 introduces the circuit schematic, working principle and fault-tolerant principle of DNUL and TNUL; Section 4 evaluates the hardened performance, overhead and sensitivity to variation; Section 5 summarizes this paper.

2 The Previous Hardened Latch Designs

Figure 1 shows the basic elements which have been commonly used in previous hardened latches. Figure 1a is the C-Element (CE) [13]. Figure 1b is the clocked CE. Figure 1c is the ISC, ISC is the abbreviation of Input-Split C-Element. Because compared with the C-Element, ISC is equivalent to separating one input of C-Element into two inputs. Therefore, it is defined as Input-Split C-Element (ISC) [11]. Figure 1d is the clocked ISC. Figure 1e is the TCE. As we can see from Fig. 1a, when two inputs of the CE are the same, the output is reverse to the input. The output temporarily holds the previous logic value when the CE has two different inputs. In the same way, the TCE has the same property, i.e., the output temporarily holds the previous logic value when the inputs are different.

Under the premise that the number of transistors is the same as for CE, the ISC not only has the ability like the CE to block SNU, but also has the effective ability to block DNU. When the logic values of the three inputs are the same, the ISC works normally. When the inputs CPN = 000, Q = 1. After DNU occurs at the inputs of ISC, the logic value of the CPN may be upset to 110, 101 or 011. According to the structure of ISC, Q upsets to 0 if and only if the CPN is upset to 101. Similarly, when CPN = 111, Q upsets if and only if CPN is upset to 001. In addition, if CPN is upset in either case, Q will be in the "hold" state. So, the DNU tolerance rate of ISC is 2/3. Next we will briefly introduce the previous hardened latches.

DONUT [4] in Fig. 2a is a DNU tolerant latch. DONUT can be seen as a combination of 4 Dual Interlocked storage Cells (DICE) [2], and uses the SNU tolerance of DICE

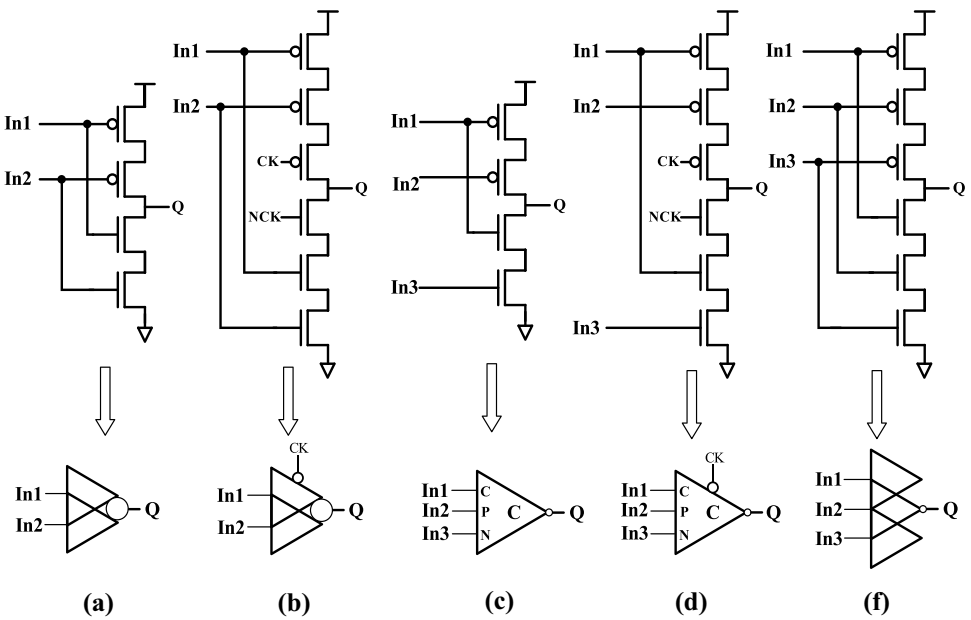


Fig. 1 Basic elements. **a** CE, **b** Clocked CE, **c** ISC, **d** Clocked ISC, **e** TCE

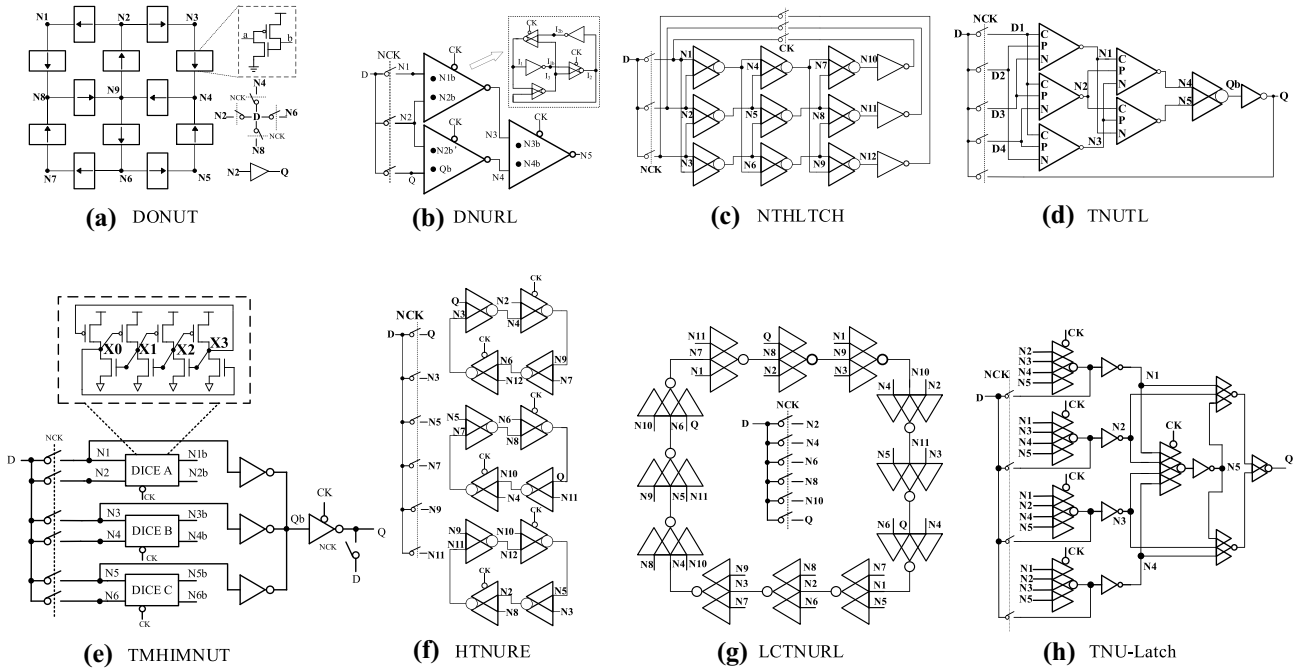


Fig. 2 Schematics of the previous hardened latches. **a** DONUT, **b** DNURL, **c** NTHLTCH, **d** TNUTL, **e** TMHIMNUT, **f** HTNURE, **g** LCTNURL and **h** TNU-Latch

to realize the tolerance of DNU. DICE consists of 4 cross coupled elements. PMOS and NMOS of the same cross coupled elements are controlled by signals from two different nodes. When the input signal changes, there will be a delay between the control signals of PMOS and NMOS for the same cross coupled element, resulting in short-circuit current and increased circuit power consumption. Similar to DICE, DONUT uses 12 cross coupled elements, which also has short-circuited current and generates short-circuit power consumption. Therefore, the power consumption of DONUT is relatively large. As a one-level buffer is added between input and output, the delay is also large.

DNURL [20] in Fig. 2b is a DNU tolerant latch. Each SNU-Resilient Cell can realize SNU tolerance. DNURL utilizes three SNU-Resilient Cells interconnecting to form a redundant interlocked structure, achieving complete tolerance of DNU. DNURL utilizes a high-speed path, so the delay is small. However, DNURL has more transistors than the proposed DNUL, so the power consumption and area are relatively large.

NTHLTCH [8] in Fig. 2c is a DNU tolerant latch. NTHLTCH utilizes nine C-Elements to constitute 3×3 array, filtering the wrong logic value level by level, achieving complete DNU tolerance. NTHLTCH does not use a high-speed path, so the delay is large. NTHLTCH has more transistors than DNUL, so its power consumption is greater than DNUL.

TNUTL [11] in Fig. 2d is a TNU tolerant latch. Based on the blocking ability of the ISC and CE, TNUTL realizes TNU tolerance through three-level filtering of upset. However, there is no feedback loop in TNUTL, so the node logic value is not stable. TNUTL utilizes a high-speed path, and the number of transistors is very small, so the delay and power consumption are very low.

HTNURE [19] in Fig. 2e is a TNU tolerant latch. Based on the tolerance of CE loop to SNU, HTNURE combines three C-Element loops to realize TNU tolerance. HTNURE utilizes a high-speed path and clock-gating, so the delay and power consumption are low. However, HTNURE has 8 more transistors than TNUL.

TMHIMNUT [22] in Fig. 2f is a TNU tolerant latch. Based on the tolerance of DICE to SNU, TMHIMNUT utilizes three DICEs and " wired-AND " selector at the output to realize TNU tolerance. TMHIMNUT utilizes a high-speed path, so the delay is low. TMHIMNUT utilizes three DICEs, so there is the problem of short-circuit current mentioned above. Therefore, power consumption of TMHIMNUT is high.

LCTNURL [23] in Fig. 2g is a TNU tolerant latch. Based on the powerful blocking ability of Triple-input C-Element, LCTNURL connects 12 Triple-input C-Elements into a loop, and realizes TNU tolerance through the blocking of upset level by level. LCTNURL utilizes high-speed path, so the delay is low. LCTNURL has a large number of transistors

and does not utilize clock-gating, so the power consumption is large.

TNU-Latch [18] in Fig. 2h is a TNU tolerant latch. TNU-Latch utilizes a large number of transistor stacks. Based on the strong blocking ability of clocked quadruple-input C-Element, TNU-Latch attains TNU tolerance. TNU-Latch does not utilize a high-speed path. In the transparent mode, the path from input to output is long, so the delay is very high. The number of TNU-Latch transistors is large, so the power consumption is high.

3 Proposed Hardened Latch Design

3.1 Circuit Structure and Working Principles of DNUL

Figure 3 shows the schematic of the proposed DNUL, which consists of four transmission gates ($TG_0 \sim TG_3$), six ISCs ($ISC_0 \sim ISC_5$) and a TCE. With six internal nodes ($N_0 \sim N_5$), the feedback loop of DNUL connects as follows: The In1 (C) of ISC_i connects to N_i, In2 (P) connects to N_{i+4}, In3 (N) connects to N_{i+2}, and output connects to C of ISC_{i+1} (i = 0, 1, 2, 3, 4, 5). It should be noted that the numerical operations of subscript are all senary addition operations, represented by "*mod6*". For example, $(3 + 4)_{mod6} = 1$. D, Q, CK, and NCK are the input, output, clock signal, and complementary clock signal, respectively.

Figure 4 shows the layout of the proposed DNUL design. When CK = 1 and NCK = 0, DNUL works in the transparent mode. $TG_0 \sim TG_3$ turn on. D propagates to Q only through one-level transmission gate (TG_3), which can greatly reduce delay. ISC_1, ISC_3 and ISC_5 turn off, which can reduce power consumption. D propagates to internal nodes N_0, N_2 and N_4 through TG_0, TG_1 and TG_2, respectively. Then N_1, N_3 and N_5 are driven by ISC_0, ISC_2 and ISC_4, respectively.

When CK = 0 and NCK = 1, DNUL works in the hold mode. $TG_0 \sim TG_3$ turn off. ISC_1, ISC_3 and ISC_5 turn on. The signal holds in the feedback loop. The N_1, N_3, and N_5 nodes propagate to output Q through TCE.

3.2 Fault Tolerance Principle of DNUL

The following is the fault-tolerance analysis of DNUL to SNU and DNU. Before analysis, it is assumed that $N_0 = N_2 = N_4 = 0$, $N_1 = N_3 = N_5 = 1$ and Q = 0 in the hold mode. In Figs. 5 and 9, the red lightning symbol in the simulation waveform indicates that a double exponential current source [12] is used to perform fault injection at this position. We adopt the double exponential model for fault injection, and the fault injection node is added with the following current sources:

$$I(t) = \frac{Q}{(\tau_2 - \tau_1)}(e^{-t/\tau_2} - e^{-t/\tau_1}) \quad (1)$$

Compared with the early single exponential current source model, the double exponential current source model can more accurately describe the process of rapid rise and slow decline of leakage current after a particle incident. Therefore, it is suitable and accurate for simulating fault injection. Q is the injected charge of the fault injection node.

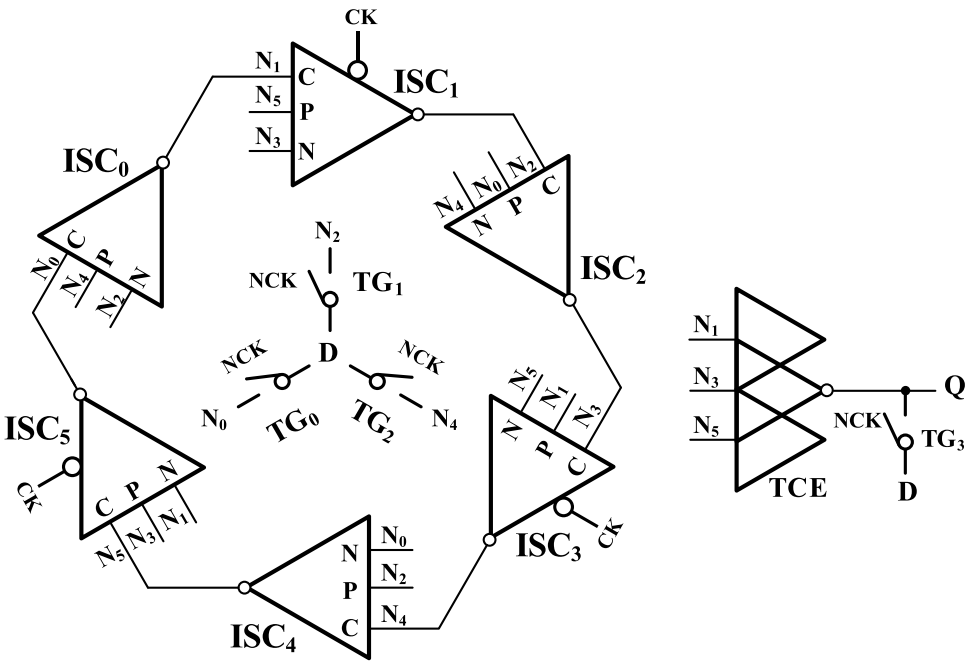


Fig. 3 Proposed hardened latch DNUL

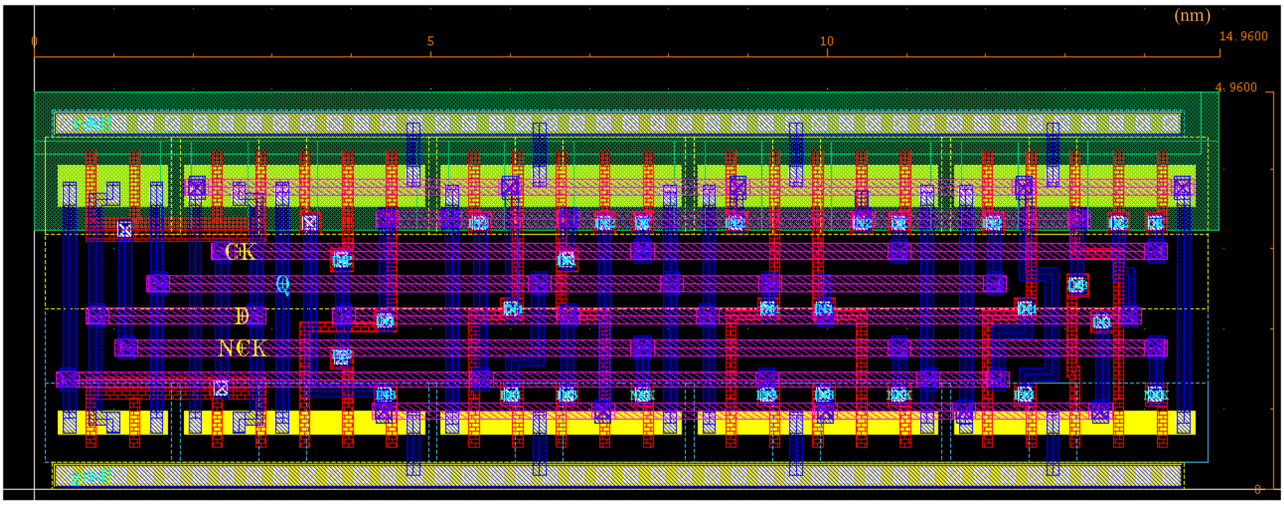


Fig. 4 Layout of the proposed DNUL design

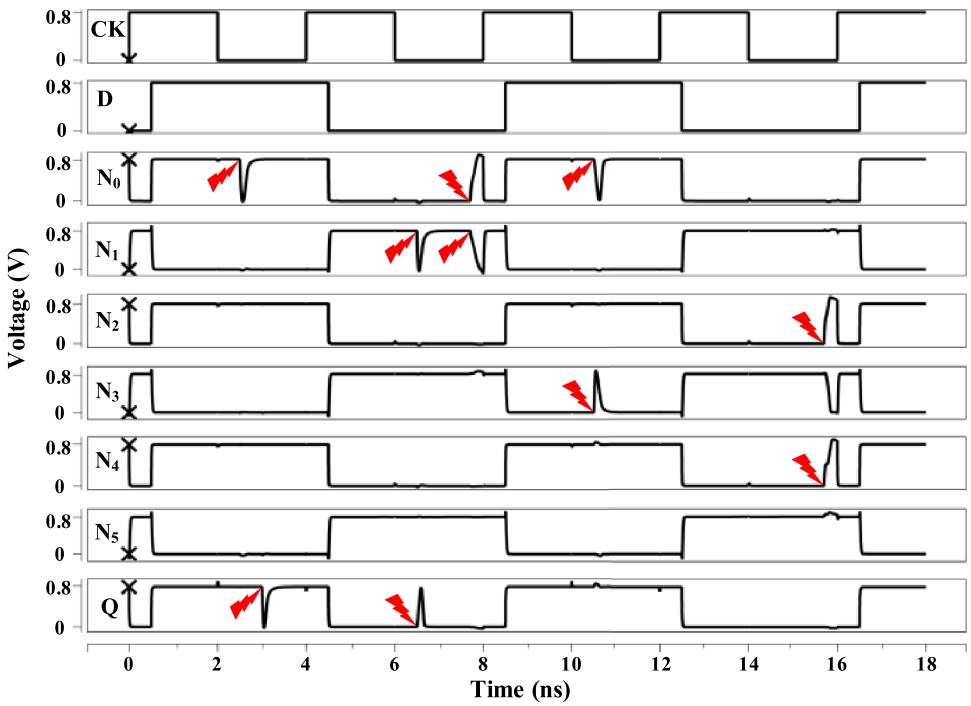
"t" is the simulation time for fault injection. "τ_1" is the ion trajectory establishment constant, which is set to 50 ps in the simulation. "τ_2" is the charge accumulation time constant, which is set to 164 ps in the simulation [12, 15, 17].

SNU1 *SNU occurs at an internal node.* Because of the symmetry of DNUL, we can take upset at N_0 as an example. When upset occurs at N_0, it will not propagate to other internal nodes because of the blocking ability of ISC_0, ISC_2 and ISC_4. N_1, N_3 and N_5 quickly recover N_0 to the correct logic value. As shown in Fig. 5, when fault injection is performed at N_0 at 2.5 ns, N_0 can recover quickly.

SNU2 *SNU occurs at output node Q.* The internal nodes will not be affected. So N_1, N_3 and N_5 quickly recover Q to the correct logic value by TCE. As shown in Fig. 5, fault injection is performed at Q at 3 ns.

DNUL has six internal nodes and one output node. Therefore, there are totally $C_7^2 = 21$ cases for DNU. We will discuss and classify in three situations.

Fig. 5 Fault injection of DNUL



DNU1 *DNU occurs at internal nodes, and the two upset nodes are exactly two inputs of the same ISC.* We discuss the worst case for this situation, such as $< N_2, N_4 >$. N_2 and N_4 upset from 0 to 1 at the same time. Because of the blocking ability of ISC, the output of ISC_0 and ISC_4 is unchanged. The output of ISC_2 (N_3) is upset from 1 to 0. The outputs of both ISC_1 and ISC_3 are in "hold", so N_2 and N_4 hold the wrong logic value. But Q does not suffer an upset due to the protection of TCE. Hence, DNUL can completely tolerate the DNU of this situation. Fault injection is performed at $< N_2, N_4 >$ at 15.7 ns in Fig. 5. It can be seen that the latch tolerates this kind of DNU. This situation totals $2 \times C_3^2 = 6$ cases.

DNU2 *DNU occurs at internal nodes, but the two upset nodes are not two inputs of the same ISC.* We discuss the worst case for this situation, such as $< N_0, N_1 >$. N_0 is upset from 0 to 1 and N_1 is upset from 1 to 0. Therefore, the outputs of both ISC_0 and ISC_5 are in "hold", i.e., N_0 and N_1 cannot recover to the correct logic values. But other internal nodes are not affected, so Q holds the correct logic value because of the filtering of TCE. Hence, DNUL can completely tolerate the DNU of this situation. As shown in Fig. 5, the fault injections are performed at $< N_0, N_1 >$ and $< N_0, N_3 >$ at 7.6 ns and 10.5 ns, respectively. It can be seen that the latch tolerates this kind of DNU. This situation totals $C_3^1 \times C_3^1 = 9$ cases.

DNU3 *DNU occurs at one internal node and the output Q at the same time.* Taking $< N_1, Q >$ as an example, after N_1 is upset, it recovers to the correct logic value by ISC_0. Q also recovers to the correct logic value by TCE. Hence, DNUL can achieve complete tolerance and also self-recovery to the DNU of this situation. Fault injection is performed at $< N_1, Q >$ at 6.5 ns in Fig. 5. It can be seen that the latch tolerates this kind of DNU. This situation totals $C_6^1 = 6$ cases.

In summary, three situations of DNU contain $6 + 9 + 6 = 21$ sub-cases, i.e., it covers all DNU cases. The above proves that DNUL can completely tolerate DNU. DNUL is a blocking latch. When the data is stored for a long time and DNU occurs, the output may be in the high impedance state. There will be leakage current which makes the logic value unstable. In order to ensure the correct output logic value, we can add a keeper to the output to drive the output. DNUL_keeper is shown in Fig. 6. For very low-frequency applications, we can use DNUL_keeper. For current mainstream chips, the operating frequency is generally hundreds of megahertz so that DNUL can be fully competent.

3.3 Circuit Structure and Working Principles of TNUL

Figure 7 shows the schematics of TNUL. Compared to DNUL, the feedback loop of TNUL adds two ISCs. The number of internal nodes also increases to eight ($N_0 \sim N_7$). To tolerate TNU, the output level of TNUL uses two-level CEs (C_0, C_1 and C_2). The output level nodes include X_0, X_1 and Q.

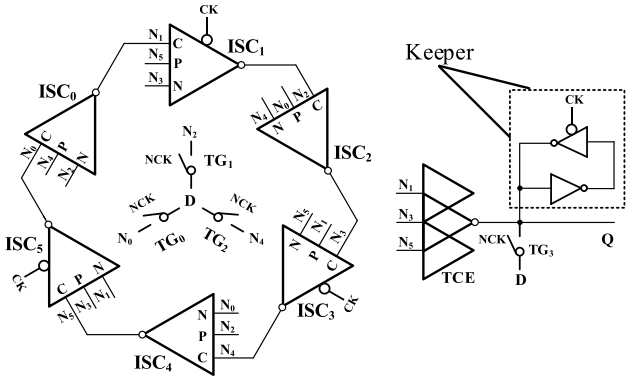


Fig. 6 The schematic of the DNUL_keeper

Figure 8 shows the layout of the proposed DNUL design. The feedback loop of TNUL connects in this way: The In1 (C) of ISC_i connects to node N_i, In2 (P) connects to N_{i+6}, In3 (N) connects to N_{i+4}, and output connects to C of ISC_{i+1} (i = 0, 1, 2, 3, 4, 5, 6, 7). Similarly, the numerical operations of subscript are all octonary addition operations, represented by "*mod8*". TNUL works the same way as DNUL whether in the transparent mode or hold mode, so no additional analysis is performed.

3.4 Fault Tolerance Principle of TNUL

Since the fault tolerance principle of TNUL to SNU and DNU is the same as DNUL, we no longer analyze them. Figure 9 shows the fault injection of SNU and DNU: At N_2 at 2.5 ns; At X_0 at 3 ns; At Q at 3.5 ns; At $< N_0, N_1 >$ at 6.5 ns; At $< N_0, Q >$ at 10.5 ns.

There are $C_{11}^3 = 165$ TNU cases, which are classified into the following four situations for analysis:

TNU1 *TNU only occurs at the feedback loop.* The worst cases of this situation can result in some nodes not recovering to the correct logic value. Taking $< N_0, N_2, N_3 >$ as an example, N_0 and N_2 are upset from 0 to 1, and N_3 is upset from 1 to 0. X_0 suffers an upset from 1 to 0 by C_0. Therefore, the outputs of both ISC_2 and ISC_7 are in "hold", so N_3 and N_0 hold the wrong logic value. X_0 also holds the wrong logical value by C_0. But under the filtering of the CEs of the output level, Q is not affected. Anyway, TNUL can completely tolerate TNU in this situation. As shown in Fig. 9, the fault injection is performed at $< N_0, N_2, N_3 >$ and $< N_1, N_3, N_5 >$ at 7.7 ns and 11.5 ns, respectively. It can be seen that the latch tolerates this kind of TNU. This situation totals $C_8^3 = 56$ cases.

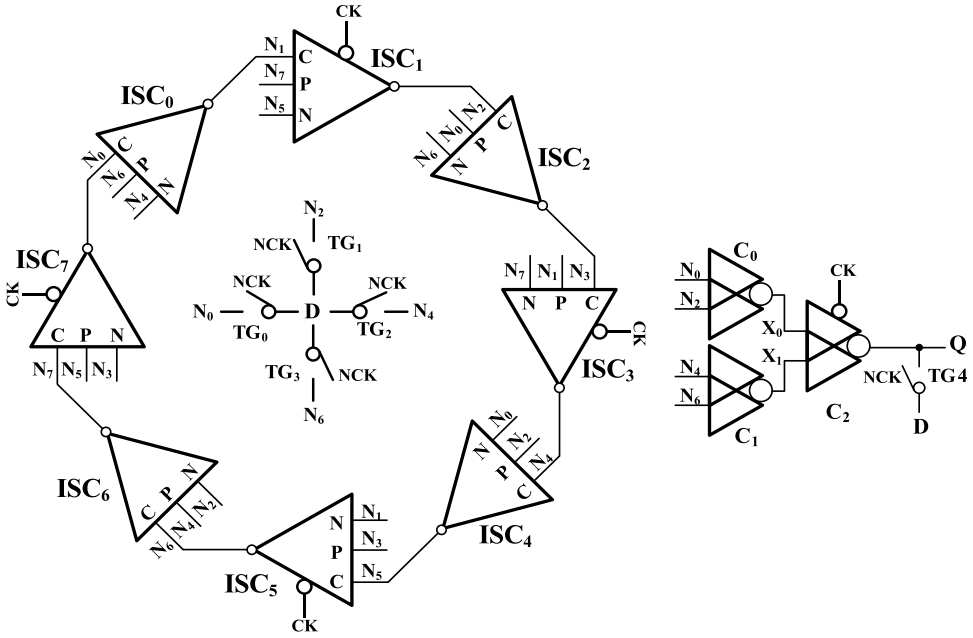


Fig. 7 Proposed hardened latch TNUL

TNU2 *Two upset nodes are at the feedback loop and one upset node is at the output level.* Discussing the worst case, i.e., $< N_1, N_6, X_1 >$, N_1 and X_1 are upset from 1 to 0, and N_6 is upset from 0 to 1. Therefore, the outputs of both ISC_0 and ISC_5 are in "hold", so N_1 and N_6 hold the wrong logic value. X_1 also holds the wrong logical value by C_1. But under the filtering of the C_2 of the output level, Q is not affected. In a word, TNUL can completely tolerate TNU in this situation. As shown in Fig. 9, the fault injection is performed at $< N_1, N_6, X_1 >$ at 15.5 ns. It can be seen that the latch tolerates this kind of TNU. This situation totals $C_8^2 \times C_3^1 = 84$ cases.

TNU3 *One upset node is at the feedback loop and two upset nodes are at the output level.* Known from the above analysis, single node upset at the feedback loop can achieve self-recovery, and then refresh the logic value of the output level nodes to achieve TNU self-recovery of this situation. As shown in Fig. 9, fault injection is performed at $< N_0, X_0, Q >$ at 18.5 ns. It can be seen that the latch tolerates this kind of TNU. This situation totals $C_8^1 \times C_3^2 = 24$ cases.

TNU4 *TNU only occurs at the output level, i.e., X_0, X_1 and Q upset at the same time.* The nodes at the feedback loop will not be affected. So X_0, X_1 and Q quickly recover to the correct logic value by C_0, C_1 and C_2, respectively. As shown in Fig. 9, fault injection is performed at $< X_0, X_1, Q >$ at 19.5 ns. This situation totals one case.

Four situations contain 56 + 84 + 24 + 1 = 165 subcases, i.e., it covers all TNU cases. The above proves that TNUL is completely tolerant to TNU. Like DNUL_keeper,

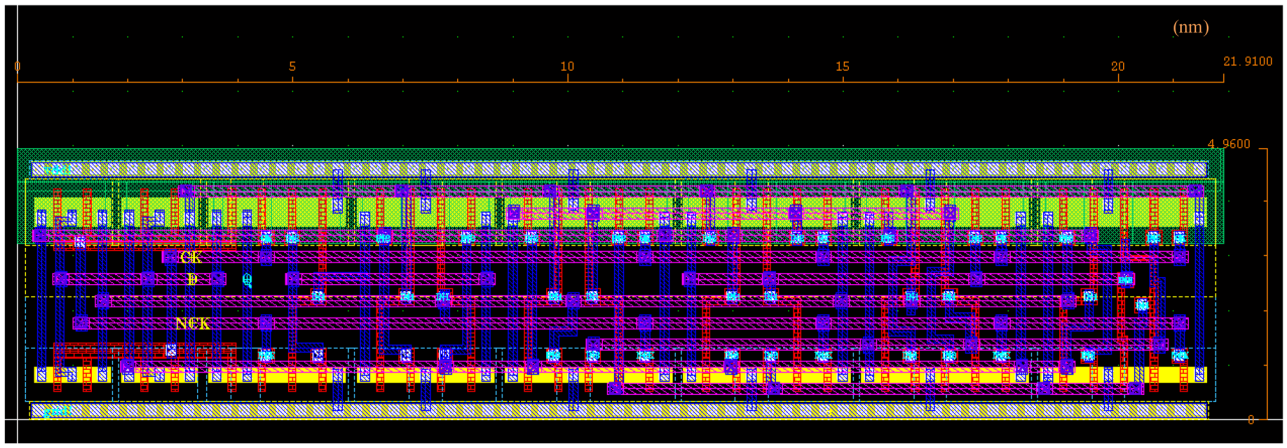


Fig. 8 Layout of the proposed TNUL design

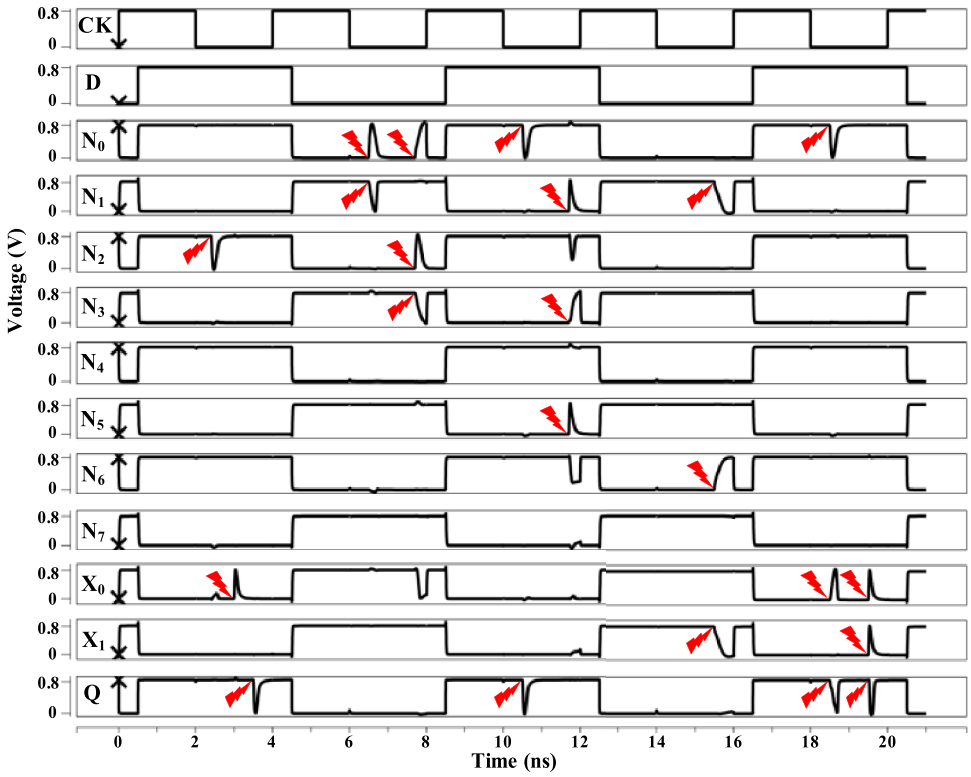


Fig. 9 Fault injection of TNUL

TNUL can also add keeper to the output to keep the output logic is correct. For mainstream applications, TNUL is fully competent.

4 Evaluation and Comparison

This part evaluates and compares the proposed latches with previous hardened latches, in terms of hardened performance, overhead and sensitivity to variation.

4.1 The Comparison of Hardened Performance and Overhead

To ensure fairness, the simulation conditions are the same for the proposed latches and the compared latches. The simulation software used is HSPICE. Simulation conditions are set as 22 nm CMOS process, 0.8 V supply voltage, 25 °C temperature and 250 MHz clock frequency.

Under the premise of ensuring that the circuit can work properly, the PMOS transistor has W/L = 88/22 nm while the NMOS transistor has W/L = 44/22 nm. Table 1 shows the comparison in terms of hardened performance and overhead. The second to fourth columns represent the hardened performance, which indicates whether the SNU, DNU and TNU are fully tolerated, respectively. "√" means that the latch can tolerate, "×" means that the latch cannot tolerate. It can be seen from Table 1 that the comparison latches DONUT, DNURL, NTHLTCH and the proposed DNUL can tolerate SNU and DNU; the comparison latches TNUTL, HTNURE, TMHIMNUT, LCTNURL, TNU-Latch and the proposed TNUL can fully tolerate SNU, DNU and TNU. The following is the comparison of the critical charge of each latch, and Q_{crit} is the critical charge. For fairness of comparison, the critical charge is the injected charge when the node happens to have full swing. For DNU tolerant latch, Q_{crit} represents the minimum charge required to upset the two internal nodes at the same time; For TNU tolerant latch, Q_{crit} represents the minimum charge required to upset the three internal nodes at the same time. However, these upsets will be tolerated by the hardening latch, and the output of the latch will not be affected.

The Delay refers to the propagation delay, that is, the D-Q delay. Power denotes the average power consumption of the latch within 20 ns [16]. The Area designation corresponds to the silicon area extracted from layout comparisons. T_{setup} is the setup time. For the input of the latches, T_{setup} is the minimum setup time before the CLK high level disappears. T_{setup} is equivalent to the time required to establish stable logic values for all internal nodes and output Q in transparent mode [8]. The smaller the setup time, the faster the latch responds to the input change, which means the better the latch performance.

Table 1 Comparison of performance and overhead of latches

Latch	SNU	DNU	TNU	Q_{crit} / fC	Delay / ps	Power / µw	PDP / aJ	10^{-3} × Area / µm^2	T_{setup} / ps
DONUT [4]	√	√	×	5.45	24.06	1.19	28.63	60.70	28.12
DNURL [20]	√	√	×	3.76	3.02	0.92	2.78	111.29	59.05
NTHLTCH [8]	√	√	×	4.42	12.39	0.76	9.42	97.81	62.63
DNUL (proposed)	√	√	×	4.05	2.30	0.28	0.64	74.20	22.03
TNUTL [11]	√	√	√	1.68	7.42	0.32	2.37	63.24	47.79
HTNURE [19]	√	√	√	3.93	2.88	0.44	1.27	126.49	19.23
TMHIMNUT [22]	√	√	√	3.98	1.54	0.84	1.29	112.44	7.96
LCTNURL [23]	√	√	√	3.50	4.84	0.83	4.02	147.58	57.69
TNU-Latch [18]	√	√	√	6.45	92.61	0.85	78.72	144.06	95.32
TNUL (proposed)	√	√	√	4.50	1.52	0.39	0.59	108.92	21.07

In order to compare the latch performance comprehensively, we introduce PDP. Formula (2) shows the calculation of PDP.

$$PDP = Delay \times Power \tag{2}$$

Compared with the latches with the same hardened performance (DONUT, DNURL and NTHLTCH), the delay, power consumption, PDP and the setup time of the DNUL are optimal, the area overhead of DNUL is suboptimal. The delay and PDP of TNUL are optimal in the comparison with all compared latches. Compared with the latches with the same hardened performance (TNUTL, HTNURE, TMHIMNUT, LCTNURL and TNU-Latch), the delay and PDP of the TNUL are optimal, and the critical charge, power consumption and area overhead are suboptimal. The proposed TNUL is better than TNUTL, LCTNURL and TNU-Latch, and worse than HTNURE and TMHIMNUT in terms of the setup time.

4.2 PVT Variation Analysis

With advances in IC process, latches become more sensitive to variations of PVT [1]. Based on the stable working characteristics of ISC and CE, the proposed latches are insensitive to variations of PVT. As shown in Figs. 10 and 11, for comparing the stability of each latch, variation analysis is performed for the proposed latches as well as for the DNU and TNU tolerant latches.

As shown in Fig. 10, Monte Carlo simulations based on 500 samples were performed by sweeping the gate length using a ±10% Gaussian distribution with variation at the ±3σ level and the gate oxide using a ±10% Gaussian distribution with variation at the ±3σ level. Figure 10a is the comparison scatter diagram of delay variation between the proposed DNUL and the DNU tolerant latches after Monte Carlo simulation; Fig. 10b is the comparison scatter diagram of power consumption variation between DNUL and the DNU tolerant latches after Monte Carlo simulation; Fig. 10c is the comparison scatter diagram of delay variation between TNUL and the TNU tolerant latches after Monte Carlo simulation; Fig. 10d is the comparison scatter diagram of power consumption between the proposed TNUL and the TNU tolerant latches after Monte Carlo simulation. The abscissa represents 500 simulation times. In order to facilitate the observation of data variation, the comparison diagrams of the proposed latches and the comparison latches are displayed independently.

Figure 10a shows the variation of the delay of the DNU tolerant latches with the variation of process. Figure 10b shows the variation of the power consumption of the DNU tolerant latches with the variation of process. Figure 10c shows the variation of the delay of the TNU tolerant latches with the variation of process. Figure 10d shows the variation of the power consumption of the TNU tolerant latches with the variation of process. The scatter plots of the proposed latches are very concentrated. The more concentrated the scatter distribution, the lower the sensitivity of the latch to process variations. The results show that the proposed latches have very low sensitivity to process variation.

Figure 11 is the voltage and temperature variation analysis. Figure 11a shows the variation of delay at different voltages; Fig. 11b shows the variation of power consumption at different voltages; Fig. 11c shows the variation of delay at different temperatures; Fig. 11d shows the variation of power consumption at different temperatures. In Fig. 11a and c, because of the large delay of TNU-Latch, the delay of TNU-Latch uses the right longitudinal axis, and the other latches use the left longitudinal axis. As we can see from Fig. 11, the variations of delay and power consumption of DNUL and TNUL are low.

These validate the high stability of the proposed DNUL and TNUL.

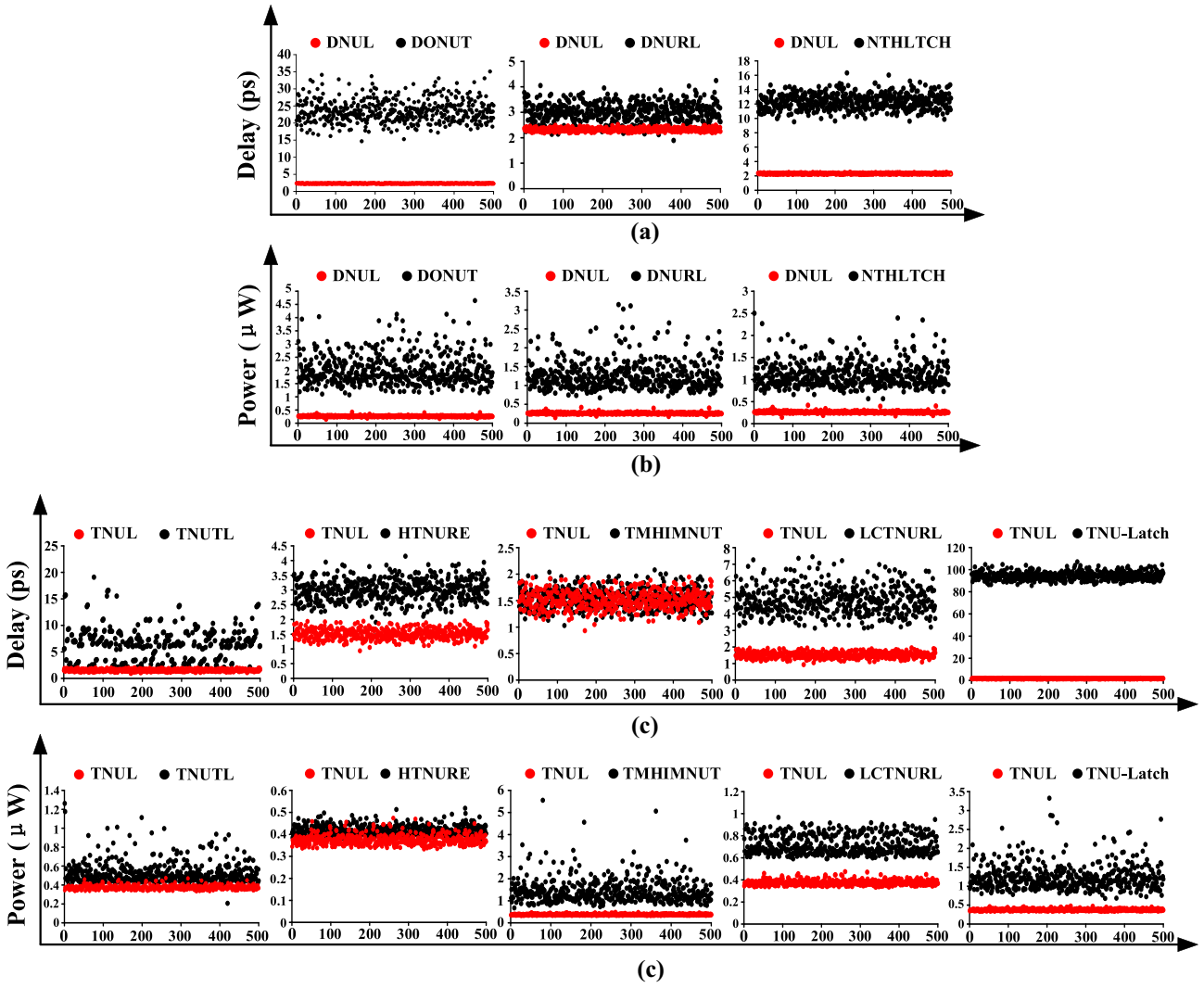


Fig. 10 Monte Carlo simulations. **a** The variation of delay of the DNU tolerant latches with the variation of process, **b** The variation of power consumption of the DNU tolerant latches with the variation of process, **c** The variation of delay of the TNU tolerant latches with the variation of process, **d** The variation of power consumption of the TNU tolerant latches with the variation of process

5 Conclusion

For the increasing problems of DNU and TNU, this paper proposes DNUL and TNUL, respectively. Based on the robust blocking property of the ISC, we use a subtle interconnection way and connect the ISCs into a large feedback loop to maintain the logic value. Then, the CEs at the output level filter the wrong logic value, so that DNUL and TNUL can effectively tolerate DNU and TNU, respectively. Through the introduction of clock-gating and high-speed path technique, DNUL and TNUL attain very low overhead. At the same time, Monte Carlo simulations and Voltage and Temperature Variation analysis show that the proposed latches are insensitive to variations of PVT and have high stability.

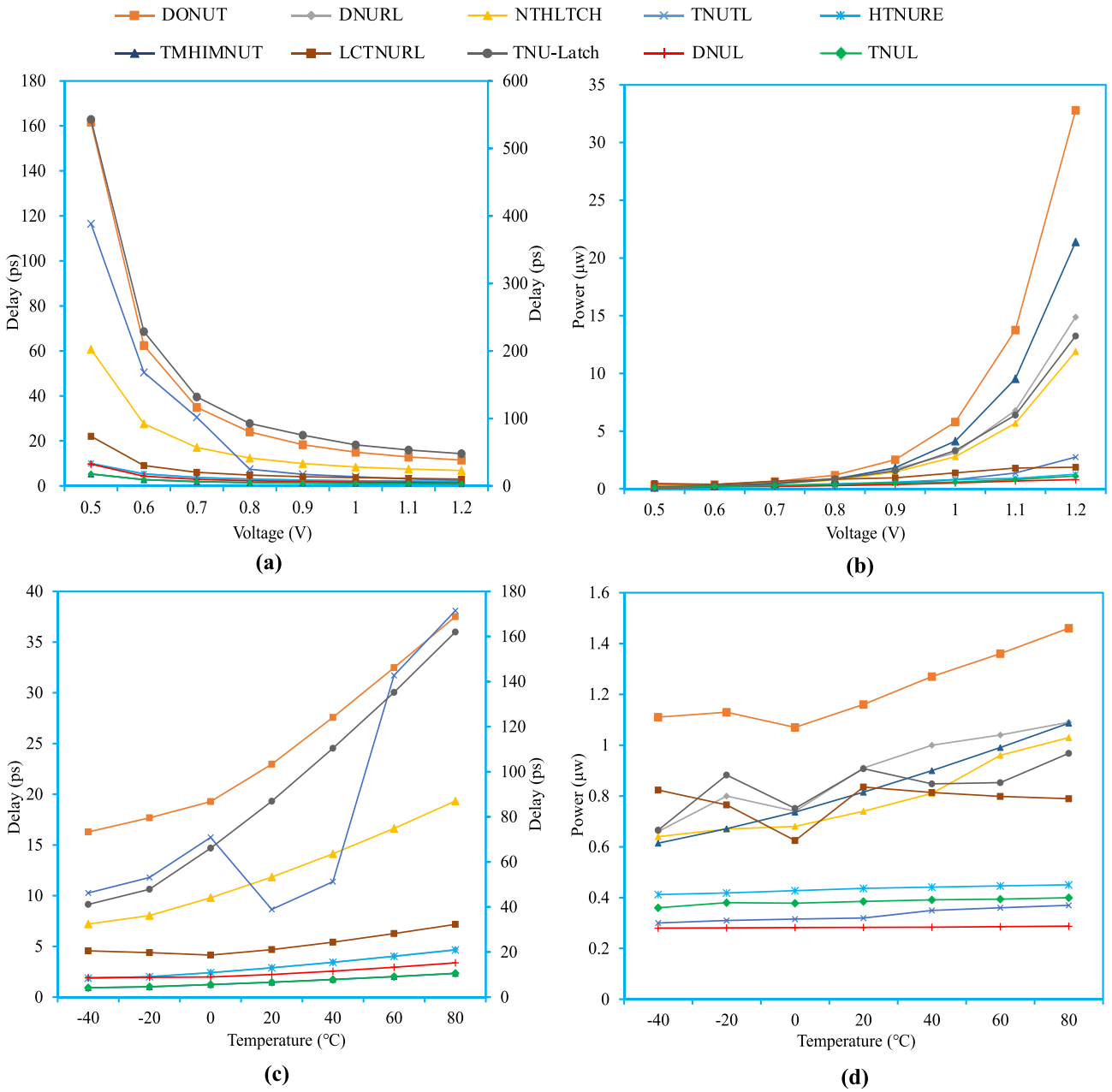


Fig. 11 Voltage and Temperature Variations analysis. **a** The variation of delay at different voltages, **b** The variation of power consumption at different voltages, **c** The variation of delay at different temperatures, **d** The variation of power consumption at different temperatures

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Data Availability The datasets generated and analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflicts of Interests The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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