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Investigation of Single Event Effects in a Resistive RAM Memory Array by Coupling TCAD and SPICE Simulations

K. Coulié[1] · H. Aziza[1] · W. Rahajandraibe[1]

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Abstract
Resistive Random Access Memory (RRAM) are attractive candidates to overcome power, cost and integration density limitations of conventional memories. They are emerging non-volatile memories, based on resistive switching mechanisms. Due to their intrinsic structure, RRAMs technology is known to exhibit very good tolerance to radiation. In this context, this paper proposes to investigate Single Event Effects in RRAM arrays, for particles with different characteristics: a 0.6 MeV Alpha and a 1.47 MeV Aluminum. The decoding circuitry of the memory array, including bit line and source line drivers is targeted. Currents shapes generated by Alpha and Aluminum particles are obtained from TCAD simulations to propose realistic SPICE simulations. Worst cases scenarios are studied in order to point out the most sensitive configurations able to induce Single Event Effects (SEE).

Keywords OxRAM · RRAM · SEE · SPICE simulation

1 Introduction

Due to their appealing performances Resistive RAM (RRAM) [2, 3, 7, 9] are promising candidates to reach the ITRS requirements for non-volatile memories. Indeed, compared to conventional floating gate technologies, they gather fast write/read operations, low power consumption, CMOS compatibility and high endurance. Note that in literature, the acronym RRAM is often used to refer to both Oxide Random Access Memory (OxRAM) and Conductive-Bridging Random Access Memory (CBRAM). OxRAM technology will be considered in this paper. Due to their intrinsic structure, RRAMs are known to exhibit very good tolerance to radiation [21]. From the late 90 s, radiation effects are recognized as a reliability concern to account for. This is particularly true for memory devices where the transient current generated by impinging particles can induce a SEU (Single Event Upset). Thus, it is mandatory to evaluate the hardness of RRAMs against radiations. Several studies exist about RRAM sensitivity to radiation effects [5, 19, 21, 32–34], but available works often address dose effects in the resistive switching element. Alternatively, RRAMs elementary cells based on hafnium oxide have demonstrated a tolerance against various kinds of radiations [6, 16, 23, 28, 35, 37]. In OxRAM memories, MIM (Metal-Insulator-Metal) structure is used as a single-bit memory cell, while the semiconductor transistor subsystem enables performing all the peripheral operations (input/output, coding/decoding, line driving, and sense amplification). In the complementary study presented in this paper, as in previous investigations [10, 12], the case of an ion crossing the MIM (Metal-Insulator-Metal) structure of an OxRAM cell is not considered. However, if only Single Event Effects (SEE) are considered (no combined effects with dose), and accounting for the insulator thickness and the probability of occurrence of SEEs, we can expect that the impact of a particle event in the MIM structure should be low on the global SER [4, 21].

In previous studies [10, 12], we focused on SEE in the close proximity of the OxRAM cell (i.e., selection transistors). The simulations were performed for a specific

Responsible Editor: L. M. B. Poehls

✉ K. Coulié
karine.coulie@im2np.fr

H. Aziza
hassen.aziza@im2np.fr

W. Rahajandraibe
wenceslas.rahajandraibe@im2np.fr

[1] IM2NP-UMR CNRS 7334, Aix-Marseille University, IM2NP, IMT Technopôle de Château – Gombert, Marseille Cedex 20 13451, France

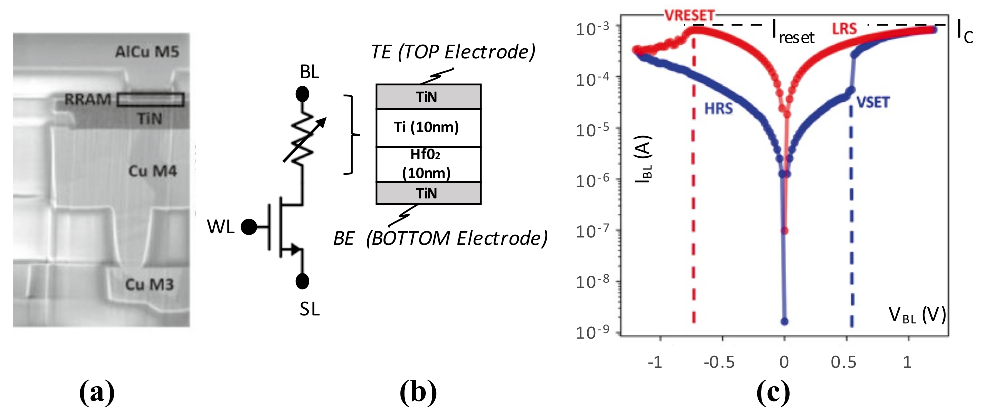

Fig. 1 **a** TEM cross-section of an OxRAM device **b** symbol view of a 1 T-1R cell **c** OxRAM I-V characteristic in log scale [22]

structure corresponding to the worst case in regards to single event radiation effects. Despite this, the studied OxRAM cell has exhibited low sensitivity to SEE. In these papers, it was shown that the only configurations able to induce effects were simultaneous impacts in a NMOS and a PMOS transistors, one being connected to the Bottom Electrode (BE) node and the other to the Top Electrode (TE) node of the OxRAM cell. Depending on the considered technology and on the memory array, the distance between two sensitive transistors can vary from tens to hundreds of microns. So, only a particle crossing the structure, could have a significant impact on the OxRAM array behavior. Then, the worst structure would correspond to 3D stacking, where NMOS and PMOS transistors could be physically close [24]. This architecture is used in order to improve integration density and scalability in emerging technologies. As a conclusion, the occurrence of a particle crossing simultaneously a NMOS and a PMOS should be low but possible.

The remainder of this paper is organized as follows. Section 2 presents the OxRAM technology. In Section 3, the simulations conditions and strategies are detailed. Section 4 presents systematic simulation results, using simplified TCAD conditions and shows the effect of SEE at different injection points. In the last part of this section, the worst-case configuration is considered combined with TCAD simulations to generate realistic transient currents. Finally, Section 5 concludes this paper.

2 RRAM Technology

An OxRAM memory cell consists of two metallic electrodes that sandwich a thin dielectric layer serving as a permanent storage medium (Fig. 1a). Its resistance may be switched between ‘0’ and ‘1’ states. The OxRAM Metal-Insulator-Metal (MIM) structure can be easily integrated in the Back-End Of Line (BEOL) on top of the CMOS subsystem [5, 6, 32–34]. Oxide-based resistive random-access memory (so-called OxRAM) elements present a lot of interesting features like high integration density, high-speed operations (write/erase/read) and satisfactory reliability performances in terms of retention and cycling. Figure 1b shows the basic 1 T-1R memory cell, where one MOS transistor is connected in series with an OxRAM cell. Figure 1c presents a typical 1 T-1R OxRAM I-V characteristic in logarithmic scale. Based on the I-V curve, the memory cell operation can be seen as follows: after an initial electro-FORMING (FMG) step [18], the memory element can be reversibly switched between the Low Resistance

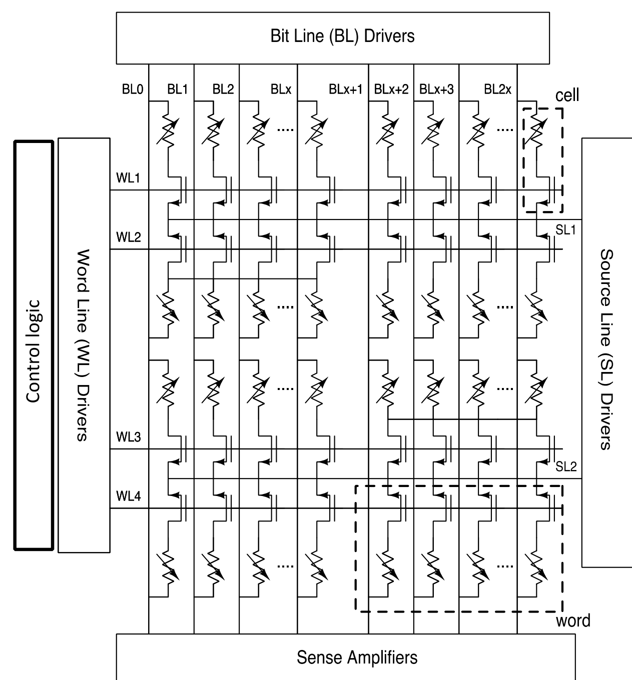

Fig. 2 Elementary memory array architecture used for simulations

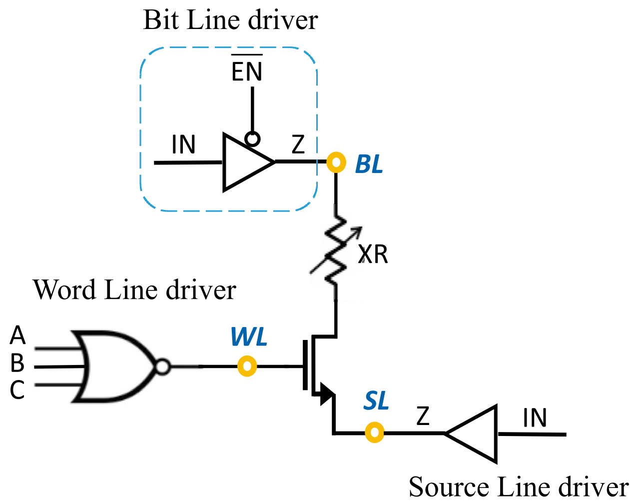

Fig. 3 Schematic diagram of one memory point and its peripheral circuit

State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance is changed by applying specific biases across the 1 T-1R cell, *i.e.*, V_{SET} to switch to LRS and V_{RST} to switch to HRS. In the 1 T-1R configuration, the transistor controls the amount of current flowing

Table 1 Operating voltage levels (H:2.5 V, HV:3.3 V, L:0 V)

	FMG	RST	SET	READ	STBY
BL	HV	L	H	HI	HI
SL	L	H	L	H	L
WL	H	H	H	H	H/L

HI High Impedance level

through the cell according to its gate voltage bias. The maximum current allowed by the select transistor is called the compliance current and is referred to as I_C in Fig. 1c. I_C controls the LRS resistance value in the SET state as well as the maximal RESET (RST) current I_{reset}.

Figure 2 presents the OxRAM array, studied in this work, which is composed of a word line driver to select the active row (WL_X), a bit line driver to select the active bit lines (BL_X) during a FORM/SET and READ operations, and a source line driver to select a specific source line (SL_X) during RST. Sense amplifiers are used to convert the cell current into a logical value at the circuit output during a READ operation. Memory cells are usually grouped into 8, 16 or 32 bits to form a memory word (dashed line). During the READ operations, the sense amplifier compares the cell current to a strictly controlled reference current.

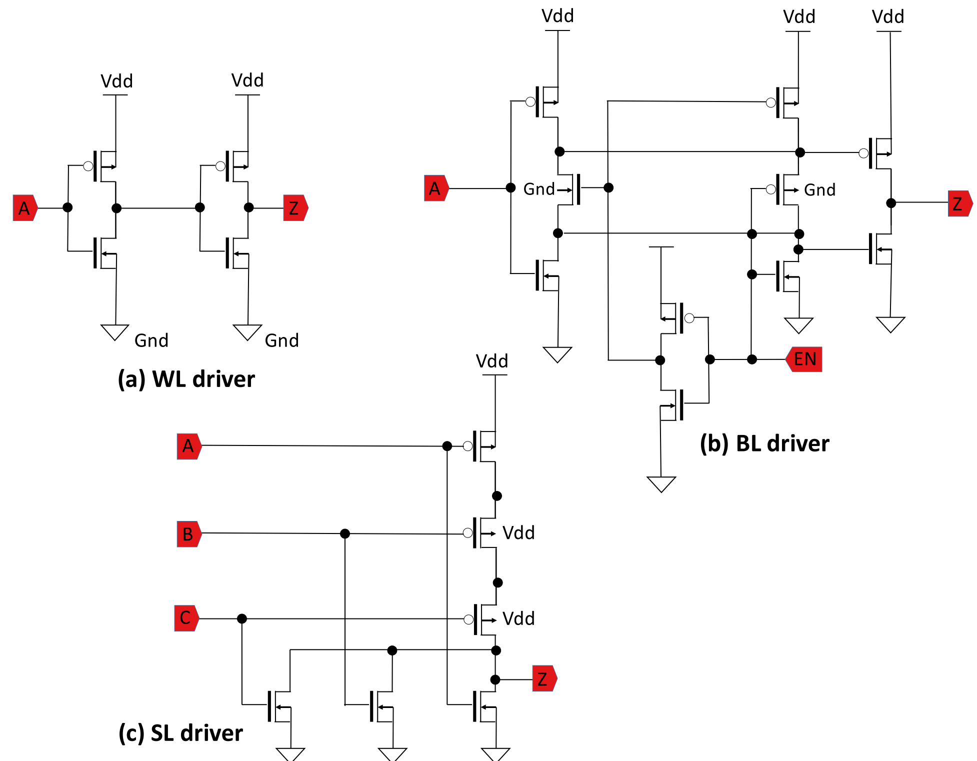

Fig. 4 Structure of WL, BL and SL drivers

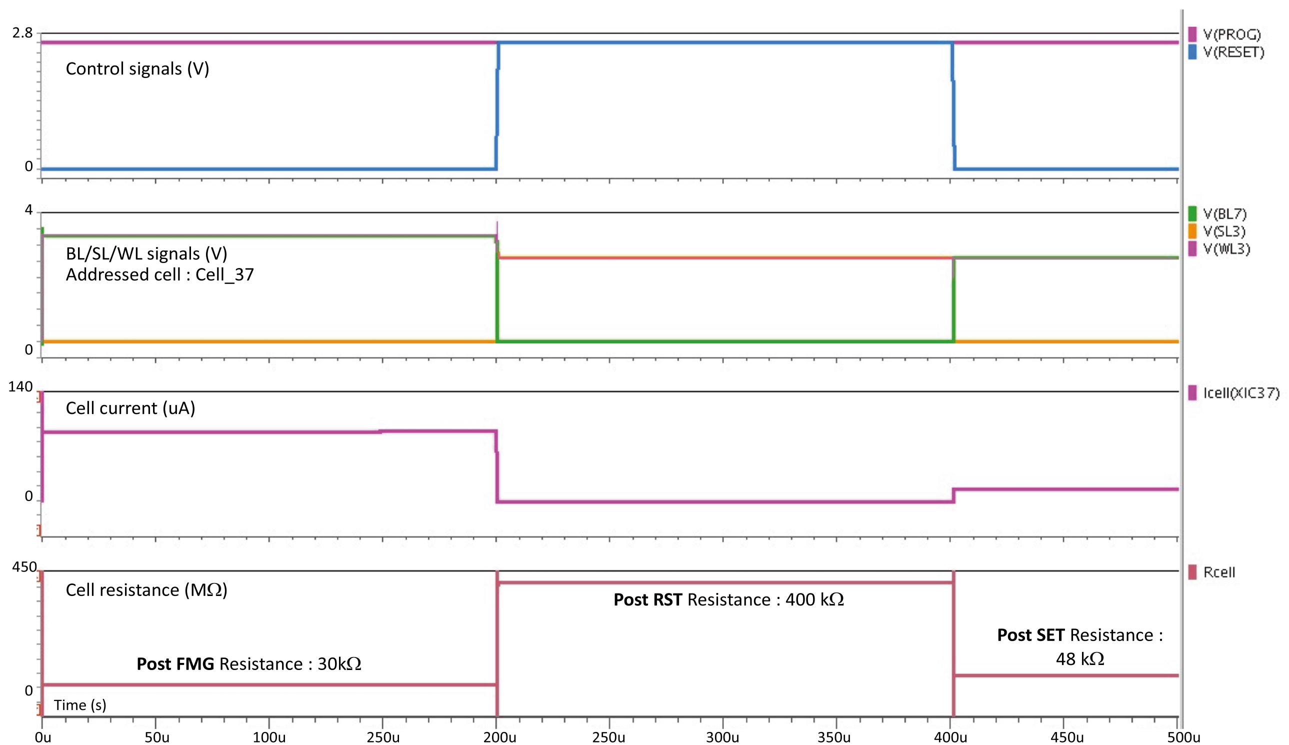

Fig. 5 Transient simulation results after FMG, RST and SET operations

3 SEE Simulation Setup in the OxRAM Array

3.1 The Current Injection Strategy

We implemented the memory array presented in Fig. 2 using a 0.13 µm High Voltage CMOS technology offering a 3.3 V supply voltage. This technology was targeted because both, measurements and model calibration, were available for the 130 nm technology. Moreover, transistors withstanding high voltages are available in the 130 nm technology. The latter are required during the FORMING operation achieved at 3.3 V. To verify the operation of our design scheme, SPICE simulations are performed using the *Eldo* simulator. Various methodologies have been developed in the past to get reliable results about SEE sensitivity using SPICE simulations [15, 20, 27, 29]. Using this kind of simulation decreases considerably the simulation time. Indeed, SPICE simulations run at least 100 times faster than TCAD simulations. It allows a very quick analysis even if the accuracy is limited for the study of radiations effects [13, 14]. It is particularly convenient when mixed-mode simulation is used to simulate the peripheral circuits at SPICE level and the impacted cell at TCAD level [11, 17].

This study considers only the configurations able to induce a change of the cell state. Hence, the investigation focuses on the peripheral circuit of one memory point (X_R) of the array, depicted in Fig. 3. Note that X_R models the OxRAM cell, which is considered as a variable resistance with a value R_{cell}. A compact OxRAM model [8] calibrated on measurements is used. The model accurately reproduces the switching mechanisms of OxRAM cells. It is used along with a 130 nm High Voltage technology from ST-Microelectronics. The peripheral circuits are three logic

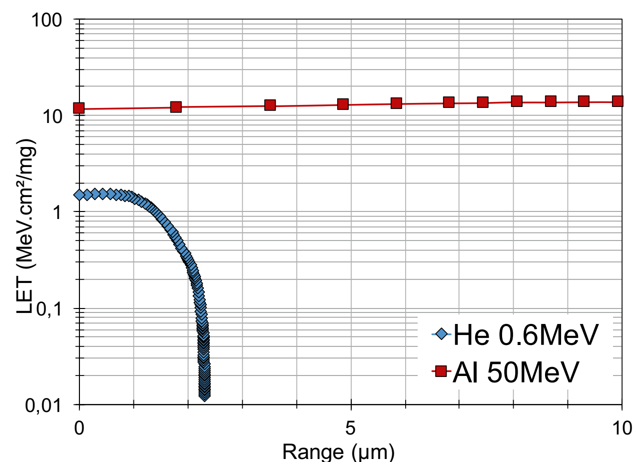

Fig. 6 LET variation extracted from SRIM tables [36], versus range, in the Silicon for Alpha and Aluminum particles

Fig. 7 Currents generated by Alpha and Aluminum particles in two different configurations: horizontal (hor.) and diagonal (diag.)

gates, involved in the memory configuration, namely the bit line (BL), the word line (WL) and the source line (SL) drivers. So, the variation of the BL, SL and WL voltages could impact the OxRAM cell resistance and could have an influence on the cell state. In order to better understand the electrical mechanisms managing the bias voltage of each terminal (BL, WL and SL), the transistor level schematic of each CMOS driver is depicted in Fig. 4(a–c).

The impact of the particle strike is studied on the steady-state of the transistors directly involved to program the RRAM value. There are five possible states: RST (reset), SET, READ, WRITE, STBY (standby). Table 1 presents typical voltage levels applied to the memory cells during FMG, RST, SET, READ and STBY operations. These voltage levels are provided by the Bit Line drivers (BL), the Source Line drivers (SL) and the Word Line (WL) drivers of Fig. 4.

Transient simulation results are presented in Fig. 5 considering the voltage levels presented in Table 1. One cell of the memory is addressed (Cell_37) by activating WL3, BL7 and SL3. The cell current I_{cell} (XIC37) and the final cell resistance (R_{cell}) are extracted after FMG (~ 30 kΩ), RST (~ 400 kΩ) and SET (~ 48 kΩ) operations.

SEE is evaluated by injecting and simulating current sources using the electrical simulator. Current sources, reflecting SEE, are injected at specific nodes of the memory array presented in Fig. 3. The current value is negative when

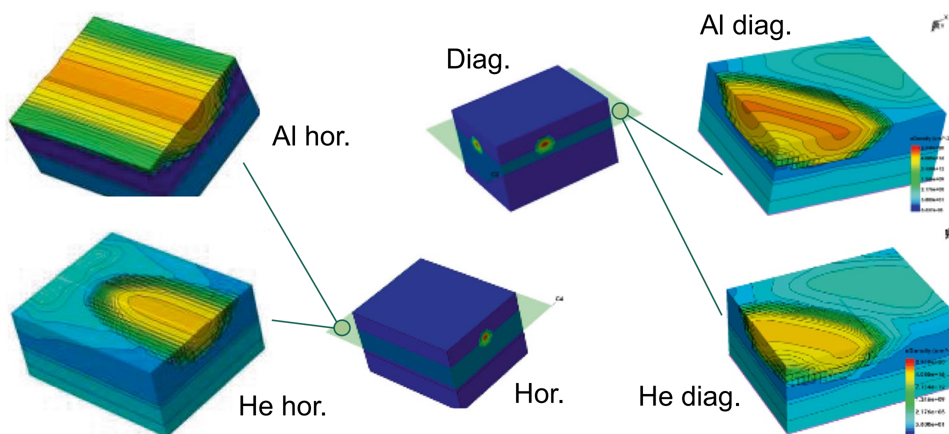

Fig. 8 Electron density in the silicon volume for the four studied configurations; Alpha and Aluminum particles in two different configurations: horizontal (hor.) and diagonal (diag.)

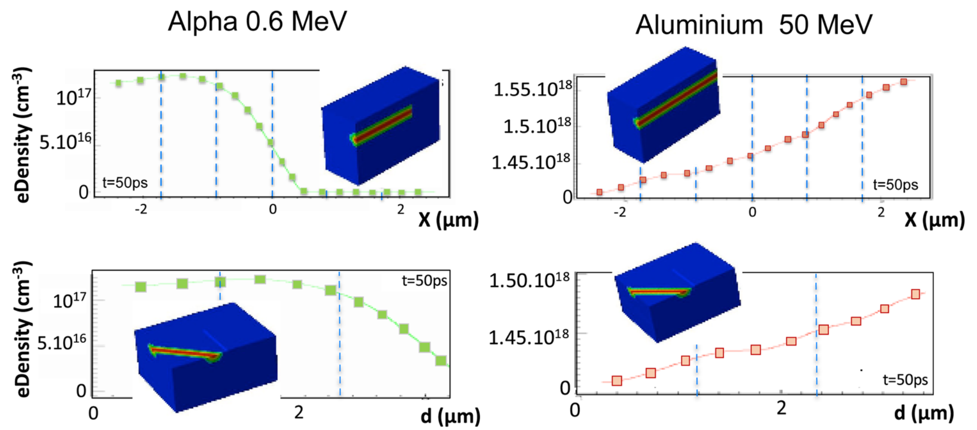

Fig. 9 Variation of the electron density along the track for the four studied configurations; Alpha and Aluminum particles in two different configurations: horizontal (hor.) and diagonal (diag.)

a NMOS transistor is struck and positive when a PMOS transistor is struck. The goal is to determine which configuration causes logical failures and which one does not, but causes an important shift of OxRAM resistances. To evaluate the impact of each source on the memory circuit, the simulation process is automated. Currents are injected sequentially and the circuit responses are automatically extracted.

3.2 Simulation of the Ion at Device Level

The current source comes from the realistic simulation of a particle crossing a silicon volume using TCAD device simulation tools (Synopsis © [31]). The effect of the ion strike is simulated using the *Heavy Ion* module of Synopsis, considering an electron-hole pair column centered on the ion track axis. The Linear Energy Transfer is defined as the energy lost by the particle, by unit of length and varies along the track depending on the initial energy of the particles [1]. An actual variation of the LET was integrated in our simulations (Fig. 6), based on the value given by SRIM tables [36]. SRIM is a collection of software packages which calculate many features of the transport of ions in matter.

Two very different particles were studied: an Alpha ion and an Aluminum ion. Alpha is a particle generated with a low initial energy and exhibiting a low LET. Its maximum LET, for the considered case is 1.53 MeV.cm^2/mg. The simulated Alpha particle is supposed to cross the device with an initial energy of 0.6 MeV, which corresponds to a range of 2.3 µm in the silicon volume. It corresponds to the end of an Alpha particle path of 1.47 MeV, generated by the initial interaction of a thermal neutron with boron-10 (Alpha contamination). The Aluminum is generated with an initial energy of 50 MeV, almost one hundred times higher than the Alpha particle one, and its maximum LET is 13.9 MeV.cm^2/mg, about ten times higher than the Alpha particle one. The Aluminum range in Silicon, corresponding to 50 MeV, is 18.43 µm. It could be produced by the interaction of fast protons with silicon [25].

Two geometries are simulated for the two considered ions: crossing horizontally (hor.) or diagonally (diag.) the silicon volume. The associated currents are presented in Fig. 7. Al hor. corresponds to a total deposited charge of 723fC, Al diag. to 398fC, He hor. to 44fC and He diag. to 43fC. The electron density in the silicon volume is presented in Fig. 8 and the variation of the electron density along the track is presented in Fig. 9.

4 SEE in the OxRRAM Array

4.1 Fault Simulation Strategy

As shown in [10, 12], the only configurations able to induce effects in the OxRAM were simultaneous impacts in a NMOS and a PMOS transistors, one being connected to the Bottom.

Electrode node and the other to the Top Electrode node of the OxRAM cell. These electrodes correspond respectively to the BL node and to the WL or SL nodes. The schematic diagram of the simulated memory point is presented in Fig. 4, where only the transistors directly connected to the memory nodes are shown. We can state that each terminal (BL, WL and SL) are faced with PMOS and NMOS transistors that are used to set the proper operating voltages, according to the chosen configuration, as summarized in Table 1.

Particle strike is supposed to cause a transient error on the nominal value of the bias voltage at each node (BL, WL and SL) directly connected to the OxRAM. These specific nodes

Table 2 Particle strike impact

	FMG	RST	SET	READ	STBY
Impact	NO	NO	NO	NO	**YES**

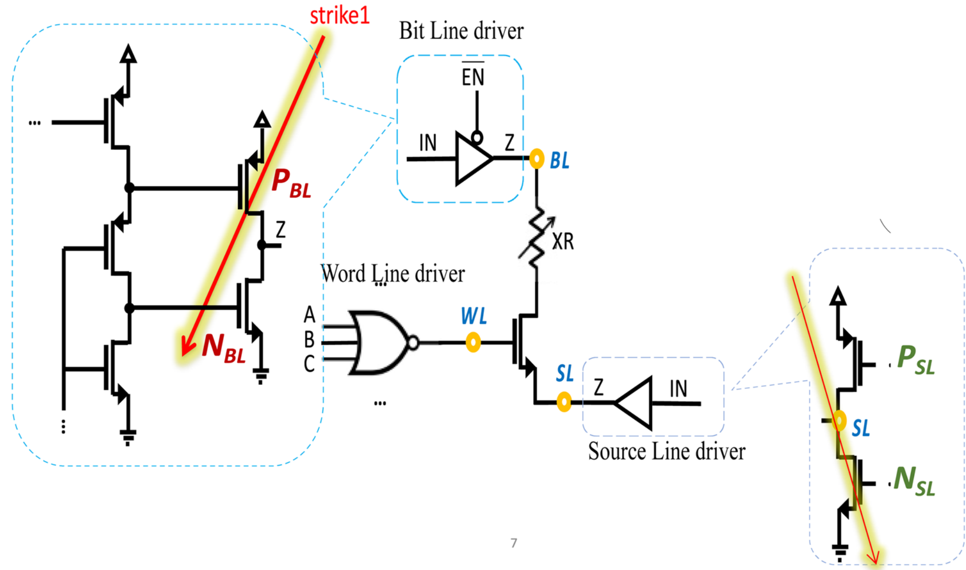

Fig. 10 Schematic diagram of one memory cell and its peripheral circuit at the transistor level

are considered as sensitive nodes regarding fault simulation due to particle crossing. Current spikes resulting from particle strikes are injected at these sensitive nodes and the state of each memory cell of the array is evaluated. Among possible states, the standby operation is the longest state in terms of duration when considering OxRAM used in microcontroller dedicated to the IoT market, although this state can last less time for some specific application as neuromorphic [26]. Then, we can assume that the probability for a radiation event to occur during standby is the highest. Moreover, based on the considered memory array architecture, the only operating stage subject to SEE errors, leading to resistance drift is the STBY stage (Table 2). A particle crossing the structure during the other states will not impact the RRAM operation. In STBY configuration, the electrical values of the RRAM terminals (BL, SL and WL) are respectively high impedance (HI), low (L) and high or Low (H/L).

To well understand the STBY configuration, we simulated the electrical operation of each driver (Fig. 4). Figure 11 focuses on the BL driver with HI value. The BL driver is in

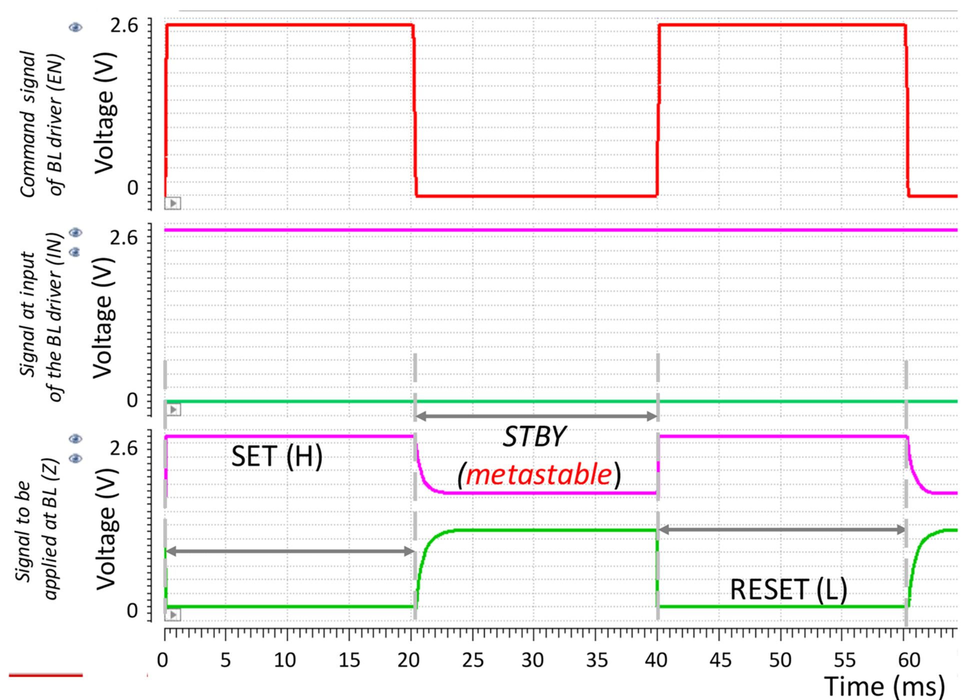

Fig. 11 Electrical value simulated at the output of the BL driver (BL node)

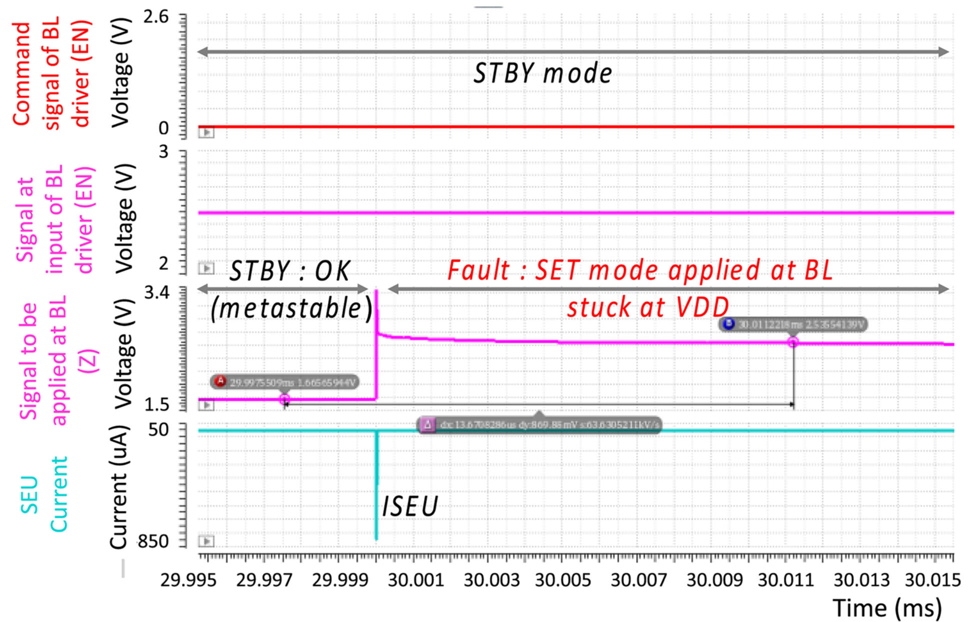

Fig. 12 Simulation of SEU strike on the BL driver (passgate)

fact a CMOS tri-state gate. When the EN terminal is set, the gate is *on* and the output voltage at the terminal Z (BL) is the same as the input one (IN). From an electrical point of view, these values correspond to VDD = 2.5 V (H) or GND = 0 V (L). However, when the gate is *off*, the voltage value at Z terminal is around VDD/2 depending on the voltage value at the input. This value corresponds to a metastable state (HI). This configuration is associated with the STBY state. Figure 12. shows the impact of a particle striking the peripheral transistor N_{BL} of Fig. 10, during the STBY mode. This is done by injecting a very short current pic (I_{SEU}) at the Z node of the BL driver. We can see in Fig. 12 that the voltage value at node Z switches to VDD, what could lead to a fault on the memory configuration.

Several scenarios are possible depending on the path and the energy of the particle. In the rest of the paper, we will focus only on the particles striking the peripheral transistors BL (P_{BL}; N_{BL}) and SL (P_{SL}; N_{SL}) of Fig. 10. Indeed, as previously assessed, these transistors act directly on the potential difference between the memory terminals.

4.2 Worst Cases Scenarios Simulation

The worst-case scenarios are related to a particle strike impacting both the Bit Line (BL) voltages and Source Line (SL) voltages in STBY mode. Thus, extensive simulations are performed to assess the robustness of the memory array versus particles striking at these specific locations. Two configurations are studied. The first one considers a memory cell at LRS (Low Resistance State: 48 kΩ). The second one considers a memory cell at HRS (High Resistance State: 400 kΩ).

Figure 14 shows the impact of a particle (at 50 µs) on a HRS cell in STBY mode. The simultaneous impact of the particle on BL and SL nodes induces a voltage difference across the cell of the memory array connected to the impacted drivers. Then, a programming current through the cell is triggered and a change of the cell resistance from HRS (368 kΩ) to LRS (51 kΩ) is detected. This event is named

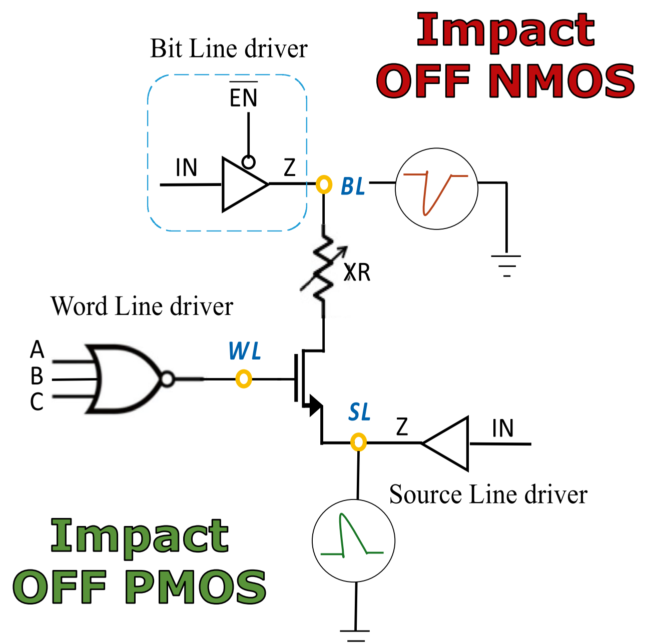

Fig. 13 Schematic diagram of one memory cell and its peripheral circuit at the transistor level including an example of NMOS and PMOS current sources configuration

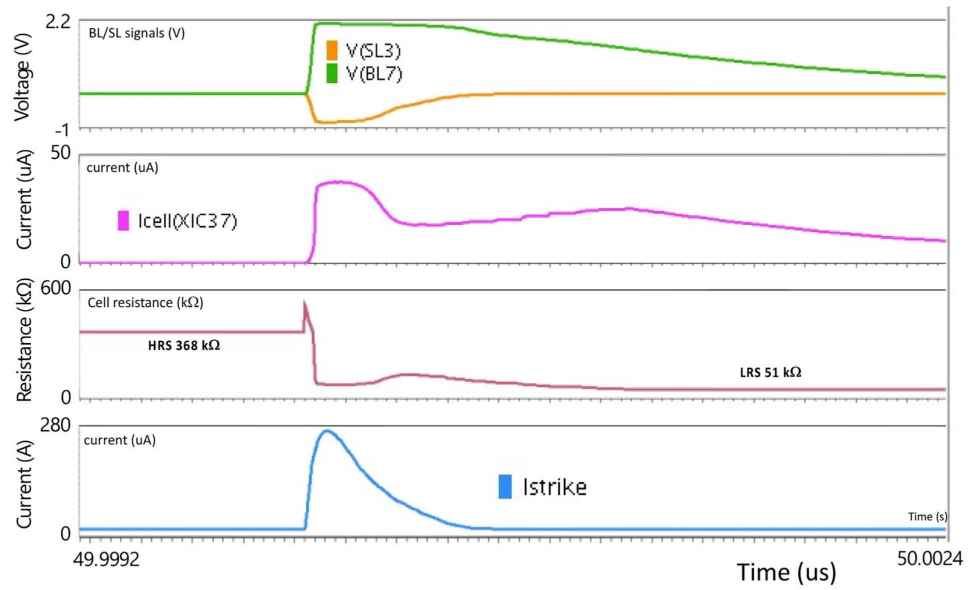

Fig. 14 Transient simulation results for a particle *Al hor*. striking a cell in HRS state

Single Event Upset (SEU) as the memory state is switched with respect to the OxRAM nominal values. For each simulated configuration in this work, a PMOS is simultaneously impacted with a NMOS. Then a negative current is injected when a NMOS is supposed to be struck, and a positive current for a PMOS (Fig. 13).

Figure 15 shows the impact of the Al hor. particle on a LRS cell (47 kΩ) in STBY mode. In this configuration, a shift of memory cell resistance towards lower LRS levels (26 kΩ) is observed. This resistance shift improves the LRS. However, going deeper in the LRS state can lead to programming issues during the next RESET operation. Indeed, if the LRS resistance value is too low, resetting the cell to HRS can be difficult or even impossible [18]. Then a stuck at fault will occur. It is worth noting that stuck bits are bits that return faulty values more than once after read operations.

Table 3 summarizes the particle impacts on the cell resistance when the cell is in an initial HRS or LRS state. Resistance shift, compared to the resistance nominal value before the strike, and radiative event (SEU or stuck-at-fault) are captured and presented. The analysis was conducted for the different current sources correlated with Alpha and

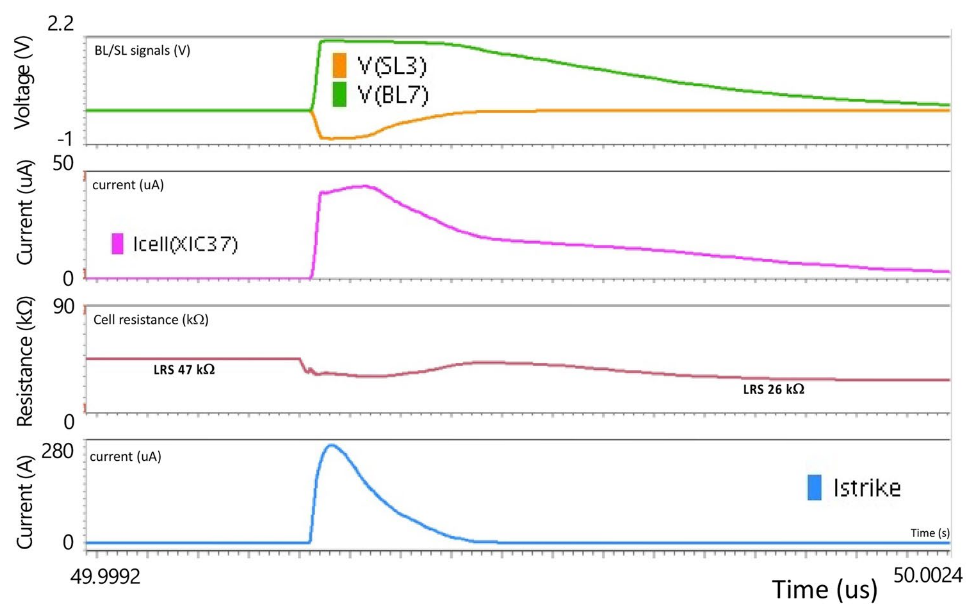

Fig. 15 Transient simulation results for a particle *Al hor*. striking a cell in a LRS state

Table 3 Worst case scenarios results in STBY mode

	State	Negative current	Positive current	Resistance shift (%)	Effect
He diag.	HRS	BL	SL	-80	SEU
He hor.	HRS	BL	SL	-80	SEU
Al diag.	HRS	BL	SL	-85	SEU
Al hor.	HRS	BL	SL	-86	SEU
He diag.	LRS	BL	SL	-28	Stuck?
He hor.	LRS	BL	SL	-28	Stuck?
Al diag.	LRS	BL	SL	-39	Stuck
Al hor.	LRS	BL	SL	-45	Stuck
He diag.	HRS	SL	BL	0	NO
He hor.	HRS	SL	BL	0	NO
Al diag.	HRS	SL	BL	0	NO
Al hor.	HRS	SL	BL	0	NO
He diag.	LRS	SL	BL	-28	Stuck?
He hor.	LRS	SL	BL	-28	Stuck?
Al diag.	LRS	SL	BL	-39	Stuck
Al hor.	LRS	SL	BL	-45	Stuck

Aluminum particles and presented in Section 3. From this table, we can conclude that the SEU will mostly occurs in the HRS state and for a particle striking simultaneously a NMOS connected to the BL node and a PMOS connected to the SL node. The opposite configuration does not induce errors but resistance shifts. Concerning the initially LRS state, for each configuration the LRS state is reinforced, potentially leading to stuck-at-faults depending on the value of the resistance shift (*Stuck?*). The resistance shift is then related to the injected current and the occurrence of stuck-at-faults would depend on the threshold of the

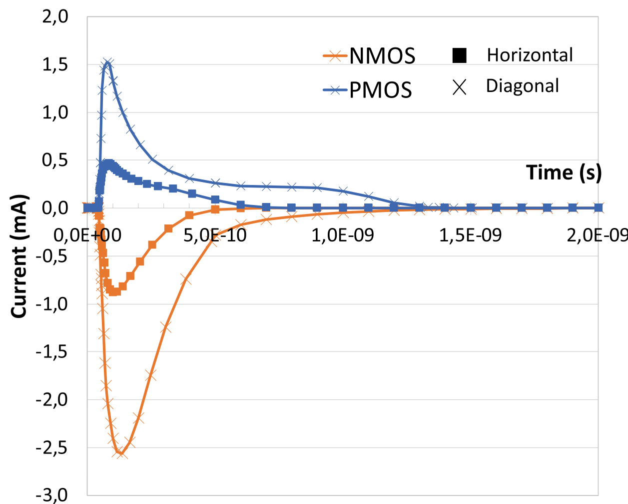

Fig. 16 Currents generated by an Aluminum ion crossing horizontally a NMOS and a PMOS (cross) or by an Aluminum ion crossing diagonally a NMOS and a PMOS (square)

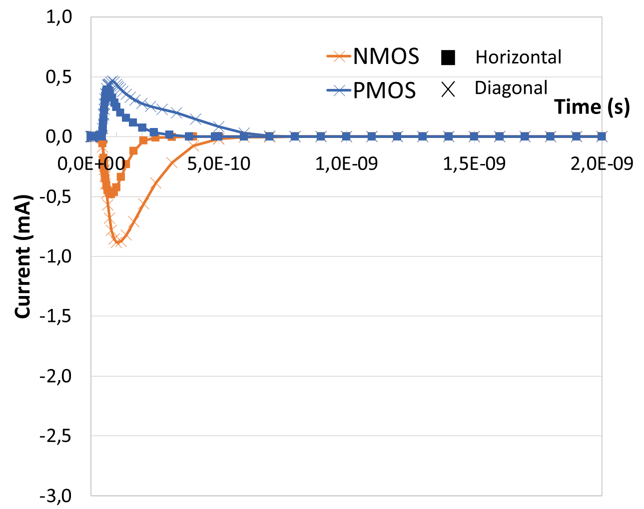

Fig. 17 Currents generated by an Alpha crossing horizontally a NMOS and a PMOS (cross) or by an Alpha crossing diagonally a NMOS and a PMOS (square)

RRAM cell. The resistance shift seems to be linked to the peak value of the generated currents. From Table 3, we can note that the resistance shift is 28% for the Alpha particles, 39% for the Aluminum in the diagonal configuration and 45% for the Aluminum in the horizontal configuration. This clearly follows the trend of the current peaks presented in Fig. 7. This peak is linked to the deposited energy. Then the stuck-at-fault occurrence would depend on the energy deposited by the particle in the sensitive transistors surrounding the RRAM.

4.3 More Realistic Approach of the SEE Study

The approach proposed in Section 3.2 is based on the simulation of the ions in a P-Substrate. The injected current is considered to be the same for an impact in a PMOS or in a NMOS. In this first approach, the only difference was the sign of the current: negative for a stroke NMOS or positive for a stroke PMOS. We decided to focus on a more realistic generation and simulation of the impact of a striking particle by simulating the particle impact in the sensitive zone of the NMOS and in the sensitive zone of the PMOS. The dimensions of the transistors are extracted from the layouts of the standard cells of the 130 nm High Voltage CMOS technology considered in this study. The obtained currents are presented in Figs. 16 and 17. The total charge deposited for each configuration is reported on Table 4.

The worst cases selected in Section 4 have been studied by injecting the new currents. The results are reported in

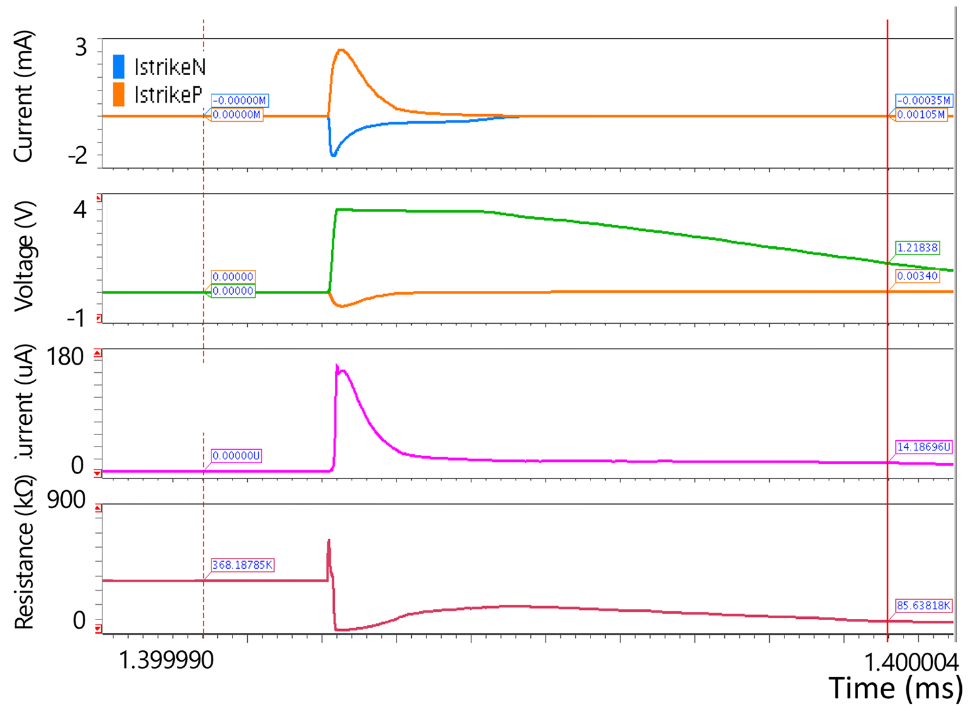

Fig. 18 Transient simulation results for a particle *Al hor.* striking a cell in a HRS state

Table 5. The only configuration inducing a SEU is Al Hor. which corresponds to the highest deposited charge (Table 4) and the highest currents (Fig. 18). This result is due to a more realistic simulation of the current in the PMOS. In Section 4, we considered that the current generated in the PMOS was the same as the one generated in the NMOS. It induced an overestimation of the SEU count. With this new approach, only the worst configuration, corresponding to an aluminum ion crossing horizontally a NMOS and a PMOS transistors, is able to change the state of the RRAM. The results of the transient simulation are shown in Fig. 17. The resistance shift from high to low resistance state is visible on the last graph. The initial resistance is 368 kΩ and the final value is 85 kΩ.

Note that the initially LRS Al Hor. case, exhibits a particular behavior. The resistance shift is 153% because it goes from 30kΩ to 76kΩ (Fig. 19). The high resistance state is about 300kΩ. In Fig. 19, the resistance variation is visible in the last graph. This variation is not high enough to be considered as a SEU, however another set of currents may have induced a SEU. This behavior was not observed when the injected currents were exactly the same with only the sign as difference. The shape of the current, or the delay between both current peaks may explain this phenomenon [10].

Table 4 Deposited charge

	NMOS Qdep (fC)	PMOS Qdep (fC)
Al Hor	725	422
Al Diago	173	119
He Hor	44	36
He Diago	19	16

Table 5 Particle strike impact considering NMOS and PMOS

	State	NMOS current	PMOS Current	Resistance shift (%)	Effect
He diag.	HRS	BL	SL	0	NO
He hor.	HRS	BL	SL	0	NO
Al diag.	HRS	BL	SL	0	NO
Al hor.	HRS	BL	SL	77	SEU
He diag.	LRS	BL	SL	0	NO
He hor.	LRS	BL	SL	2	NO
Al diag.	LRS	BL	SL	1	NO
Al hor.	LRS	BL	SL	1	NO
He diag.	HRS	SL	BL	0	NO
He hor.	HRS	SL	BL	0	NO
Al diag.	HRS	SL	BL	0	NO
Al hor.	HRS	SL	BL	0	NO
He diag.	LRS	SL	BL	0	NO
He hor.	LRS	SL	BL	4	NO
Al diag.	LRS	SL	BL	17	NO
Al hor.	LRS	SL	BL	153	SEU?

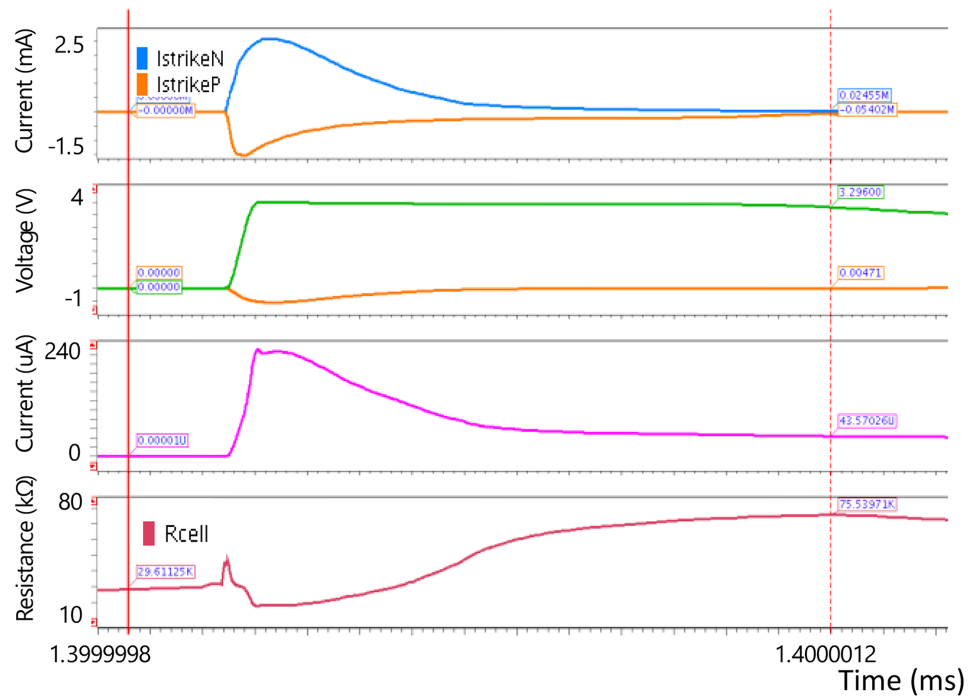

Fig. 19 Transient simulation results for a particle *Al hor*. striking a cell in a LRS state

5 Conclusion

This paper provides a complementary analysis of Single Event Effect in a OxRAM cell. As it was shown in [10, 12], some specific configurations can induce effects in this kind of device, particularly when striking simultaneously a NMOS and a PMOS transistors, in standby operation. The configurations simulated here confirm that SEU could occur in RRAM cells for some specific topologies. This is the case if a NMOS connected to BL node is close enough to the PMOS connected to the SL node to be crossed by a single particle, when initially at HRS. By avoiding this topology, SEU could be reduced. Thus, as shown in [10, 12], the worst structure would correspond to physically close NMOS and PMOS transistors i.e. 3D stacking. This architecture is used in order to improve integration density and scalability in emerging technologies.

Other configurations, related to the LRS, can induce stuck-at-fault which could be more difficult to address than SEU because the cell then remains permanently in LRS. However, stuck-at-fault are not suspected when more realistic simulations are performed. Then, stuck-at-fault would need more specific simulations focused on the OxRAM itself, in order to simulate the physical phenomena involved in OxRAM switching. Indeed, circuit simulation is not able to accurately account for the kinetic of the elementary cell.

Finally, the study was performed on a 130 nm technology. At the transistor level, downscaling should induce a shrinking of the drain/source junctions and should make them closer. As transistors for smaller technology nodes are known to be more sensitive to ionizing particles, the SEE rate should increase [30]. Thus, we plan to investigate shrinking effects in next papers by changing standby voltage state while keeping the power consumption low at the OxRAM memory array level. Moreover, at the memory matrix level, the shrunk transistors should be closer [21], facilitating the crossing of a single particle through several sensitive transistors and making the scenario studied in this paper more probable. The final error rate will also depend on the radiative environment: species of particle, initial energy, LET versus range, particle flux; collided material: silicon, HfO_2, TiN, etc.; the memory geometry and the topology.

Data Availability Statements Only supporting data related to electrode outputs could be available from the corresponding author, upon reasonable request.

Declarations

Conflicts of Interests The authors have no relevant financial or non-financial interests to disclose.

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Karine Coulié received her BS and MS degrees in 1997 and 1999, and her PhD in Microelectronics in 2002 at the University of Montpellier. She is currently Associate Professor with the Aix-Marseille University, Institute of Materials, Microelectronics and Nanosciences of Provence – IM2NP (France). Her research interests include Single Event Effects modeling in memories and memories based circuit reliability.

Hassen Aziza received his B.S. and M.S. degrees (Electrical Engineering) in 1998 and 2001, both from the University of Marseille, France. Aziza received his Ph.D. degree (Electrical Engineering) in 2004 from the University of Marseille, France. In 2005, he joined the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP), Marseille, France, where he is currently associate professor. His research interests focus on Non Volatile Memory (EEPROM and Flash) design and test as well as emerging memories (ReRam).

Wenceslas Rahajandraibe received the B.Sc. degree in electrical and electronics engineering from Nice Sophia-Antipolis University, France, in 1997. He obtained the M.Sc. and the Ph.D. degree in microelectronics from Montpellier University of Science, France, in 1999 and in 2002 respectively. He worked on the new generation of Bandgap reference circuits and contributed to design methodologies for very low current standard circuits at STMicroelectronics. Since 2003, he joined the Microelectronics department of the Institute of Materials, Microelectronics and Nanoscience of Aix-Marseille University (IM2NP), Marseille, where he is currently a Full Professor. His research interests are focused on the area of ultra-low power integrated circuit design for smart sensor interface (Electro Mechanical & Chemical sensors) as well as analog and RF circuits for wireless communications.