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Editorial

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Professor Seiji Kajihara, who passed away recently, had been serving on JETTA editorial board for over two decades. We will deeply miss him. I am grateful to our editor, Professor Xiaoqing Wen, a colleague of Professor Kajihara, for providing the details in the following paragraph.

I am deeply saddened to report to you that Professor Seiji Kajihara, Vice President of Kyushu Institute of Technology (KIT), a veteran in the LSI test research community, and above all, a dear friend of all of us, passed away at the age of 58 on May 16, 2023 after a long fight with coma induced by myocardial infarction. Seiji's funeral was held from 13:00–14:00 (JST) on May 20, 2023, in Iizuka, Japan. The president of Kyushu Institute of Technology (representing KIT), Dr. Yasuo Sato (representing co-researchers), and I (representing friends) delivered condolence speeches. Deputy Prime Minister of Japan and the Mayor of Iizuka City also sent their condolence messages. Seiji's wife, two kids, parents, two brothers and their families, together with a large number of his former colleagues, students, and friends, attended the funeral to remember his profound love for his family, his research, and his friends around the world. After the funeral ceremony, the funeral coach carrying Seiji drove around the KIT Iizuka campus, allowing Seiji a last glimpse of his beloved workplace of 30 years. May Seiji rest peacefully in heaven.

This issue contains articles on automotive testing, single event upset, radiation hardening, analog and RF testing, bridging faults, software testing, hardware security, and system-on-chip (SoC) test.

The first paper discusses automotive testing. The testing is done at the software level. Tests are functional and aim to cover aspects like safety and security, legal requirement or certification, and the function itself. Authors are Jooß from CARIAD SE, Mönsheim, Germany, and Schramm from University of Duisburg-Essen, Duisburg, Germany.

Resistive random-access memory (RRAM) is an emerging technology with potential benefits of reduced power and area, and higher levels of integration. The second paper examines single event effects (SEE) in RRAM caused by ionized particles. Investigators are Coulié, Aziza, and Rahajandraibe from Aix-Marseille University, Institute of Materials, Microelectronics and Nanosciences of Provence (IM2NP), Marseille, France.

Single event upset (SEU) in semiconductor circuits caused by radiation has been receiving much attention. The third paper advances beyond the single node upset and develops double and triple node upset tolerant latches. New latch designs are shown to be superior to the existing ones in terms of lower power delay product (PDP), and reduced sensitivity to process, voltage and temperature (PVT) variations. Authors are Huang, Wang, Ma, Liang, Ouyang, and Yan from Hefei University of Technology, Hefei, China.

The fourth paper points to the difficulties of validating the analog and RF portions of a mixed-signal system where digital parts rely on scan chains. It proposes the application of two carefully selected analog test signals applied through inserted hardware that allows the necessary observability into the analog and RF parts. This innovative approach, referred to as built-in state consistency checking (BISCC), is presented by Deyati, Muldrey and Chatterjee from Georgia Institute of Technology, Atlanta, GA, USA.

The fifth paper addresses concurrent testing that refers to detection of faults during normal functional operation of the circuit. It presents a logic-level analysis to identify fault identification transitions (FI-transitions) that can detect feedback as well as non-feedback type of bridging faults. The author, Biswal from IIIT, Bhagalpur, Bihar, India, also proposes reduction of hardware used to connect the circuit under test and automatic test equipment.

What does forest optimization have to do with software testing? The sixth paper tells us just that. To find the so-called mutation tests, a program is represented by control flow graph (CFG). As we know graphs can contain patterns referred to as trees and forests. The described method attempts to find the most bug prone paths in the CFG for

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the purpose of testing. The paper is contributed by Arasteh from Istinye University, Istanbul, Turkey, Gharehchopogh from Islamic Azad University, Urmia, Iran, Gunes from Dogus University, Istanbul, Turkey, Kiani from Fatih Sultan Mehmet Vakif University, Istanbul, Turkey, and Torkamanian-Afshar from Nisantasi University, Istanbul, Turkey.

The seventh paper focuses on Trojan detection, an important problem in hardware security. A meta-heuristic Pareto-based multi-objective optimization algorithm is used to find compact and effective tests for detecting Trojans. If that sounds complicated, then read on. The paper explains the details demonstrating how the algorithm works for combinational Trojans and even holds future promise for detecting sequential Trojans. Reporting the work are Rathor from PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India, D. Singh from National Institute of Technology, Raipur, India, and S. Singh and Sajwan from Bennett University, Greater Noida, India.

The final paper follows an unconventional path to testing cost reduction for multi-core system-on-chip (SoC). The authors argue that in a multi-core SoC for certain cores the absolute accuracy may not be paramount. Therefore, the fault coverage can be compromised, judiciously, of course, depending upon the functional requirements. They name this incomplete testing, which allows them to reduce test access time, test power, and test data volume, thereby saving on testing cost. The authors are Singh and Deka from Indian Institute of Technology, Guwahati, Assam, India, and Biswas from Indian Institute of Technology, Bhilai, Chhattisgarh, India.