Journal of Electronic Testing (2023) 39:1–2
https://doi.org/10.1007/s10836-023-06052-z

Editorial

Vishwani D. Agrawal[1]

Received: 13 February 2023 / Accepted: 13 February 2023 / Published online: 17 February 2023

We begin 2023 by wishing well to our readers. As reported in my last editorial, the journal seems to have almost recovered from the pandemic related slowdown of previous years.

We welcome three new editors to the Editorial Board of *JETTA*. Professor Bahman Arasteh is with the Software Engineering Department, Istinye University, Istanbul, Turkey. He has contributed to search-based software testing, software dependability, fault injection-based test, and software maintenance. Dr. Ujjwal Guin is with the Department of Electrical and Computer Engineering, Auburn University. Auburn, AL, USA. His expertise includes hardware security and trust, supply chain security, cybersecurity, and VLSI design and test. Professor Yashwant K. Malaiya is with the Computer Science Department, Colorado State University, Fort Collins, CO, USA. He has contributed to fault modeling, reliability, testing, quantitative security risk evaluation, and social history and demography. Biographies of the new editors appear in this issue following this editorial.

Leaving the Editorial Board at the end of 2022 is Professor Mark Tehranipoor. He has served on the Board since 2008 and decided to step down owing to the responsibilities he recently assumed at the University of Florida. He introduced hardware security to *JETTA*. This is an area that has seen significant growth in recent years.

Peer reviewing is an essential part of *JETTA*'s paper selection process. We thank our reviewers of 2022, whose names appear in this issue, for their contribution to the journal and to the profession.

This issue has eight articles covering the topics of network-on-chip (NoC), fault modeling, analog and radio frequency (RF) circuit testing, software testing, microfluidic chip testing, printed circuit board (PCB) faults, and self-healing circuits.

The first article is a survey of photonic network-on-chip (PNoC). These networks help to reduce the communication delay and loss in long interconnects. The paper summarizes basic design and test concepts and outlines loss parameters, routing algorithms, and topological factors, citing relevant references. Authors are Asadi from Ghiaseddin Jamshid Kashani University, Qazvin, Iran, Zia from Shah Abdul Latif University, Kharipur, Sindh, Pakistan, Al-Khafaji from Al-Mustaqbal University College, Babil, Iraq, and Mohamadian from Islamic Azad University, Ilkhchi, Iran.

The second paper gives a machine learning (ML) solution for the small delay fault (SDF) detection problem of resistive opens. Such defects may not cause a failure of timing specification but still present a reliability challenge. The method uses tests at multiple voltages and frequencies to examine the latent faults. Authors are Najafi-Haghi and Wunderlich from University of Stuttgart, Stuttgart, Germany. They first presented this work at the 22nd *IEEE Latin American Test Symposium* (LATS), Punta del Este, Uruguay, October 27–29, 2021.

Next, two papers deal with analog and radio frequency circuits.

The third paper develops an alternate test, also known as indirect measurement (IM), procedure for low noise amplifier (LNA). Sensors are placed close to circuit components to monitor process parameters. These sensors use machine intelligence (MI) and work in two phases, namely, training and calibration. Contributors of this work are Xiao, Diao, Qiao, Liu, He and Guo from Xiamen University, Fujian, China.

The fourth paper explores multi-site testing of analog and mixed-signal devices. This differs from the case of digital circuits where signals are binary. For analog signals, testing must deal with site-to-site variations among devices that pass the test. This investigation aims to find the maximum variation between sites, referred to as issue sites. Authors are Bruce, Farayola, and Chen from Iowa State University, Ames, IA, USA, and Chaganti, Sheikh, and Ravi from Texas Instruments, WW Hardware R&D - Connectivity Business Unit.

The fifth paper focuses on software testing. It provides a method for creating activity diagrams (AD) that are used for

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, 36,849, AuburnAlabama, USA

generating test scenarios. Total test activity on logical paths and compactness of test set are some of the quality criteria used. Authors are Du, Zhang, Chen, and Zhou from Xi'an Jiaotong University, Shaanxi, China.

The sixth paper presents a test method for digital microfluidic biochip (DMFB). It proposes simultaneously actuating more than one electrode to detect multiple faults together, thereby reducing the test time. The method allows online as well as offline DMFB testing. Authors are Ghosh from Institute of Engineering and Management, Kolkata, India, and Roy and Giri from Indian Institute of Engineering Science and Technology, Shibpur, India.

The seventh paper analyzes bend-related failures in printed circuit board (PCB) interconnects. It is found that a route with acute-angle, e.g., 45-degrees, bend is more likely to fail over a shorter time as compared with a straight interconnect or even one with 90-degree angle. Also, the failure tends to occur at the bend. Investigators reporting this work are Elliot and Brown from University of Southern Queensland, Queensland, Australia.

The eighth paper addresses fault tolerance through self-healing or evolutionary hardware (EHW). Taking the example of a virtual reconfigurable (VRC) adder, the paper develops a reconfigurable architecture on an FPGA and experiments with various evolutionary algorithms for error recovery. The investigation leads into a self-healing algorithm called chromosome reconstruction that reduces the healing time and hardware needs. The authors are Sakali and Mahammad Sk from Indian Institute of Information Technology, Manufacturing and Design, Chennai, India.