PREFACE

The modern electronic testing has a *forty* year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students.

Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device technology, circuit design, and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signal subsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits.

We have written this textbook for an undergraduate "foundations" course on electronic testing. Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course.

With equal tenacity, we address the needs of three other groups of readers. The first group consists of engineers who, upon graduation, engage in any kind of electronic hardware design, testing, or manufacturing project. Parts I and III emphasize the needs of a design-oriented project and Parts I and II those of a test-oriented project. The second group consists of students of a VLSI design course who have not taken a course on testing. Parts I and III focus on their needs. The third group, consisting of post-graduate and research students, will find a complete coverage of topics with pointers to references where advanced material was omitted for a lack of space. Figure 1.6 shows several ways to read this book.

At the 1999 *International Test Conference* during a panel discussion titled, "Increasing Test Coverage in a VLSI Design Course," a panelist from the microelectronics industry gave the wish-list as: test economics, classical semiconductor defects, simple test pattern coverage, structured design for testability techniques (scan, boundary scan, BIST) for system-on-a-chip design, automatic test equipment (constraints and costs), and selected advanced topics (I_{DDQ} and delay faults.) We kept that list in mind while writing the book and we hope the teachers of VLSI design and electronic testing courses will too.

We are all too familiar with incompleteness of software debugging and hardware design verification. No "formal" method was used to verify the material in this book either. Despite all efforts to remove errors, we cannot guarantee that the readers will not find them. We will greatly appreciate the generosity of our readers if they inform us about any errors. We will make such findings available to all readers through our websites until the publisher gives us an opportunity to make corrections, with due acknowledgment to those who have pointed them out.

We have taught a course on testing at Rutgers University for the past ten years. Interaction with the students in the course and our master's and doctoral students had the greatest influence on our understanding of the subject. We would like to thank them. Special mention should be made of the class of Spring 2000, which used the draft and pointed out corrections and improvements. We are indebted to colleagues at Bell Labs and Rutgers for their advice and counsel. The enthusiasm and support of the world-wide test professionals was exceptional. A partial list of those we thank includes: Miron Abramovici, Prathima Agrawal, Mark Barber, Dilip Bhavsar, Shawn Blanton, Amy Bushnell, Tapan Chakraborty, Srimat Chakradhar, Xinghao Chen, Dochan C. Choi, Rick Chruscial, Don Denburg, José de Sousa, Shaun Erickson, David Fessler, Hideo Fujiwara, Paul Glick, John Hayes, Michael Hsiao, James Jacob, Neil Kelly, Bill Kish, Kozo Kinoshita, Ken Lanier, Yuhai Ma, Pinaki Mazumder, Cliff Miller, Karen Panetta, Janusz Rajski, Elizabeth Rudnick, Manoj Sachdev, Kewal Saluja, Sharad Seth, and Lakshman Yagati. We thank our publisher Carl Harris for always encouraging us to proceed ahead and for being patient through schedule slips. We are thankful for the support of Al Aho, Dennis Ritchie, and Tom Szymanski, research managers at Bell Labs, and David Daut and Jim Flanagan of Rutgers University. We also wish to thank the LTX Corporation, the Advantest Corporation, Samsung Electronics Company, Ltd., IBM, and Lucent Technologies for their cooperation in providing data for this book. In describing technical contributions we have tried our best to cite correctly. From those who find their work incorrectly cited, we beg forgiveness because such errors, caused by our ignorance, were unintentional.

We have corrected errors from the previous printings. Students of our class at Rutgers, X. Liu, S. Sheng and L. Zhang (Spring 2001), and L. N. Balasubramanian, R. Modi and J. Nelson (Spring 2002), deserve thanks for pointing them out. Readers gratefully acknowledged include M. Balster and G. Robinson of Credence, K. Chakraborty of Agere Systems, Y. Kim of University of Wisconsin, and T. Pham of Alchemy Semiconductor, Inc. Lectures (*powerpoint slides*) based on this book are available at our websites and teachers can request a solution manual by e-mail.

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