straints and costs), and selected advanced topics (I_{DDQ} and delay faults.) We kept that list in mind while writing the book and we hope the teachers of VLSI design and electronic testing courses will too.

We are all too familiar with incompleteness of software debugging and hardware design verification. No "formal" method was used to verify the material in this book either. Despite all efforts to remove errors, we cannot guarantee that the readers will not find them. We will greatly appreciate the generosity of our readers if they inform us about any errors. We will make such findings available to all readers through our websites until the publisher gives us an opportunity to make corrections, with due acknowledgment to those who have pointed them out.

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