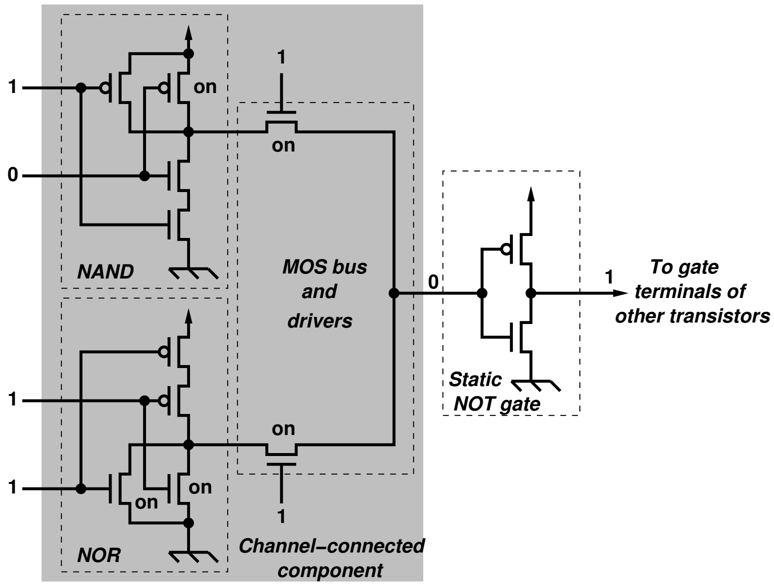

Figure 5.6: An example showing the necessity of transistor-level modeling.

no current is drawn from the supply (neglecting the quiescent or leakage current, I_{DDQ}.) In this specific configuration, the transistor implementation, called a static CMOS gate, can be modeled as an ideal Boolean gate of NAND type. Similar static designs of NOR and NOT gates are also used. The following example shows that not every CMOS structure can be mapped onto a Boolean gate.

Example 5.6 *Necessity of transistor-level models: Consider the MOS circuit of Figure 5.6. The outputs of the NAND and NOR gates are connected to a bus via two nMOS driver transistors. In a normal operation of the circuit, it is usually intended that only one driver will be turned on. However, due to signal delays, it is possible that both drivers are momentarily turned on. They may also be turned on due to design errors. These errors can be detected by simulation provided the modeling is correct. For the signal values shown in Figure 5.6, there is a conducting path formed by transistors shown as "on." If we assume that all devices have the same on-resistance, then because of the two parallel transistors in the NOR gate the output to ground resistance will be lower than the* V_{DD} *to output resistance. Depending on the threshold voltage of transistors in the NOT gate, the output of the MOS bus may be interpreted as a logic 0.*

Correct simulation requires partitioning of the circuit into "channel-connected components" [27, 103, 145]. A channel-connected component is an arbitrary interconnection of MOS transistors with three types of external connections: (1) inputs feeding only into gate-terminals of transistors in the component, (2) outputs feeding only into gate-terminals of transistors in other components, and (3) connections to V_{DD} *or ground. States of nodes inside a component are determined by analyzing the node capacitances and conducting paths between* V_{DD} *and ground formed by the connected channels of "on" transistors. Thus, for given states of input signals, the*