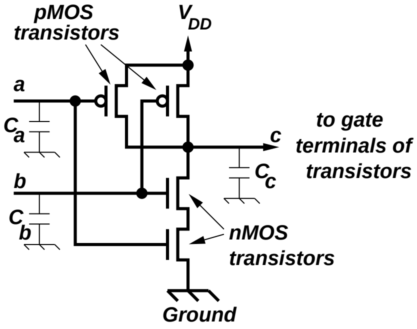
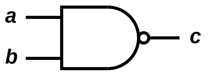


(a) Static CMOS NAND structure.



a	b	c
0	0	1
0	1	1
1	0	1
1	1	0

(b) NAND logic function.

Figure 5.5: CMOS implementation of a NAND logic gate.

Figure 5.2(a), or it may use further hierarchy. The latter case is shown in Figure 5.4, where the *FAn* is built with two half adders or *HAn*. The subnetwork *HAn* is shown in Figure 5.4(a.) Lower level subnetworks, which are frequently reused, are generally kept in *standard cell libraries*. Most HDLs [171, 667] used to describe circuits support hierarchy. Circuit connectivity description without hierarchy is usually referred to as the *flat description*. A flat description of the 32-bit ripple-carry adder of Figure 5.2(b) contains 288 logic gates.

5.3.3 Gate-level Modeling of MOS Networks

In today's semiconductor technology, digital logic functions are realized by MOS (*metal-oxide semiconductor*) transistors [718]. A MOS transistor is a three-terminal device. Two terminals, *source* and *drain*, form a semiconductor *channel*. The third terminal, *gate*, controls the conductivity of the channel. The gate is insulated from the channel and represents a capacitive load to the controlling signal source. There are two types of MOS transistors. For an nMOS device, the high state (usually, V_{DD}) of the gate makes the channel conductive, causing almost a short between source and drain. In this state, the *on-resistance* of the channel depends on the dimensions or size (length and width.) For the low state (usually, *ground*), the channel acts as an open-circuit. The pMOS device works in a complementary manner.

Figure 5.5 shows a NAND gate in the *complementary-MOS* (CMOS) design style. Signals a and b feed into high impedances since they are connected to the insulated gates of transistors. The sources of signals a and b only see equivalent capacitive loads, C_a and C_b, respectively. We assume that the output signal c feeds only to the gate terminals of some other transistors. This is modeled by the total capacitance C_c of node c. As usual, we denote the voltage level V_{DD} as logic 1 and the ground voltage as logic 0. When $a = b = 1$, the output c is grounded through the two nMOS devices. This offers a ground voltage to all gates connected to c. When either one among a or b is 0, c is isolated from ground and is connected to V_{DD} through one or both pMOS devices. Thus, the capacitor C_c is charged to V_{DD}. In either state of c, only a transient charging current flows. Once the steady state is reached,